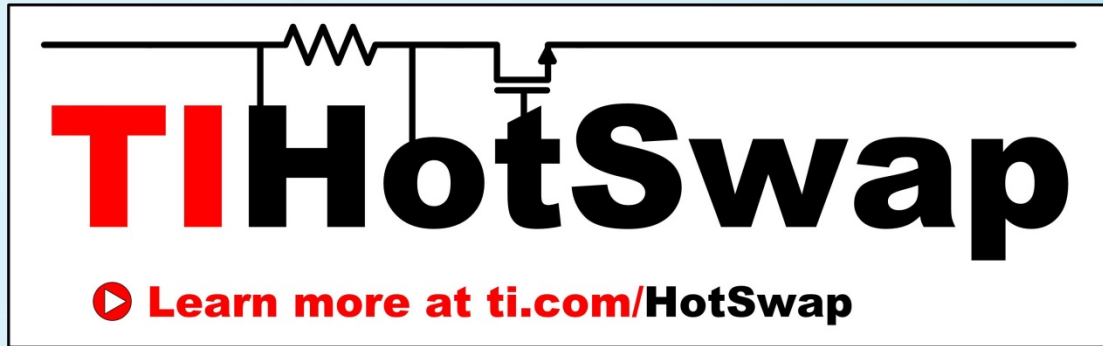


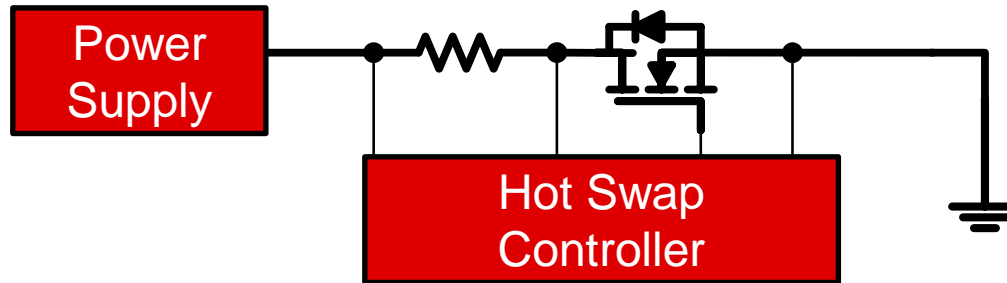
# Hot Swap Design

TI Hot Swap Team



# Stressful Hot Swap Conditions

## Start Into Short



Short means  $V_{out} = 0V$

Thus  $V_{ds}$  of the MOSFET =  $V_{in} - V_{out} = V_{in}$ .

- Worst Case  $V_{ds} = V_{in(max)}$

When considering MOSFET SOA curve, must check  $V_{ds} = V_{in(max)}$

# MOSFET Selection

## SOA

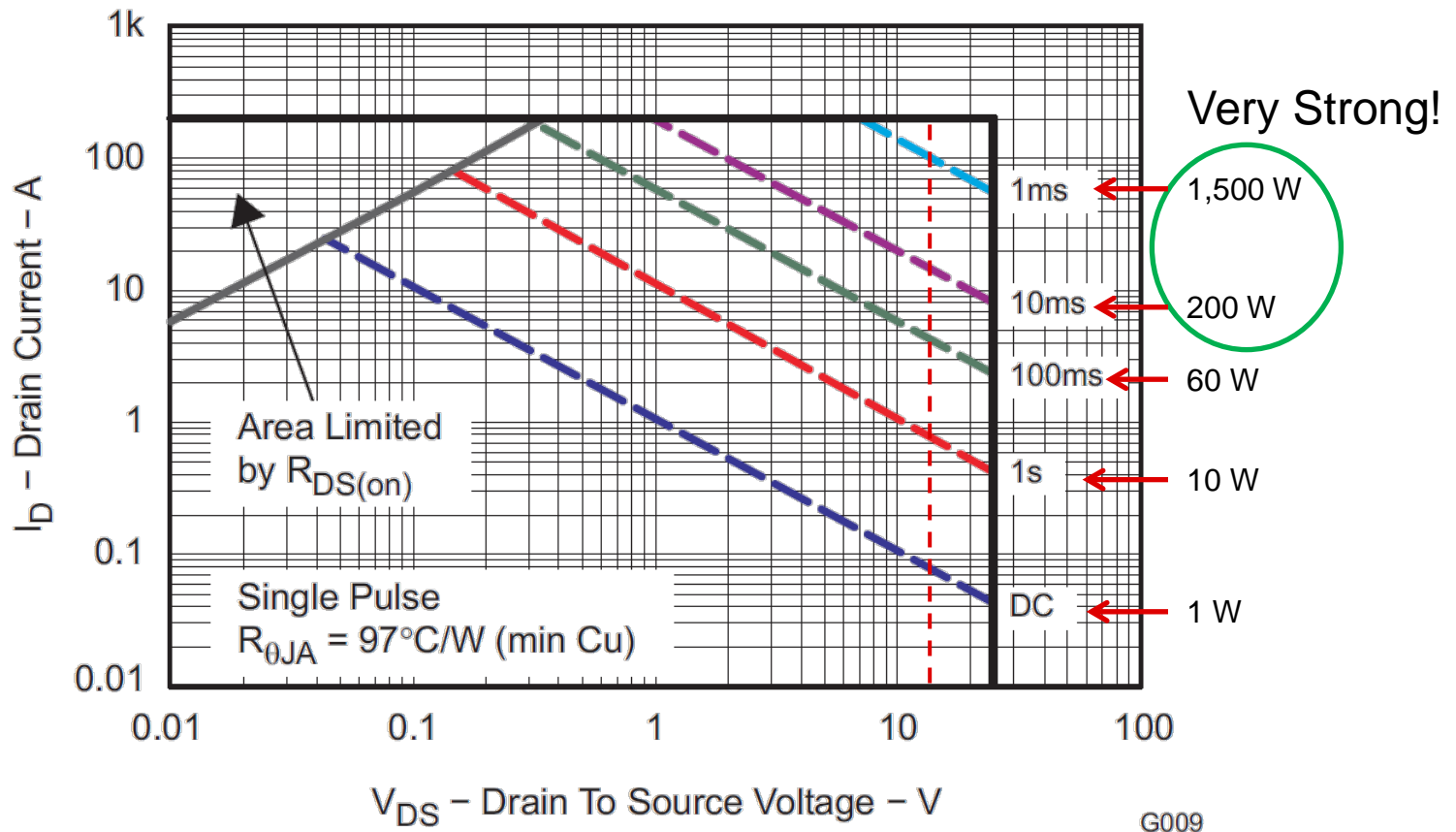


Figure 10. Maximum Safe Operating Area

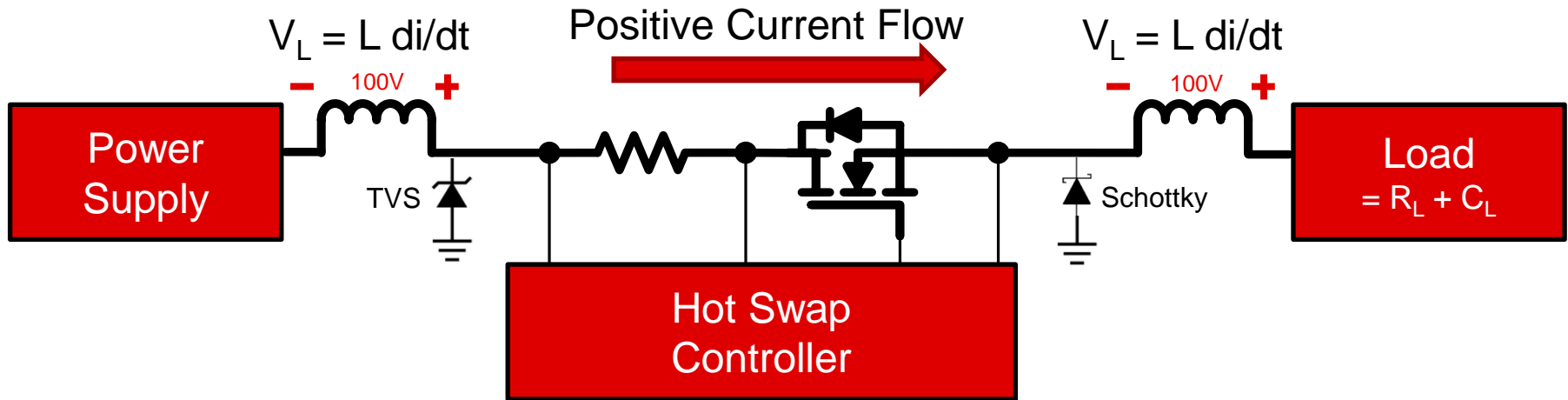
CSD16415Q5 Datasheet, Page 5

# MOSFET Selection

	V <sub>DS</sub> (V)	V <sub>GS</sub> (V)	Package	R <sub>DS(ON)</sub> (mΩ) TYP(10V)	R <sub>DS(ON)</sub> (mΩ) MAX (10V)	SOA Current Rating (A) @ 14V V <sub>ds</sub>		Qg(nC) (TYP)
						1ms Pulse	10ms Pulse	
<b>CSD16570Q5B</b>	25	+/-20	SON5x6	0.49	0.61	12	6	95
<b>CSD17570Q5B</b>	30	+/-20	SON5x6	0.56	0.69	12	6	93
<b>CSD17573Q5B</b>	30	+/-20	SON5x6	0.84	1.00	8	4.5	49
<b>CSD17575Q3</b>	30	+/-20	SON3.3x3.3	1.9	2.3	4.5	2	23
<b>CSD17576Q5B</b>	30	+/-20	SON5x6	1.7	2.0	8	4	25
<b>CSD16556Q5B</b>	25	+/-20	SON5x6	0.9	1.07	25	6	36
<b>CSD17556Q5B</b>	30	+/-20	SON5x6	1.2	1.4	35	12	30
<b>CSD17559Q5</b>	30	+/-20	SON5x6	0.95	1.15	30	14	39
<b>CSD16401Q5</b>	25	+16/-12	SON5x6	1.3	1.6	100	15	21
<b>CSD16415Q5</b>	25	+16/-12	SON5x6	0.99	1.15	100	15	21

# Stressful Hot Swap Conditions

## Hot Short / Severe Overcurrent



For Short Circuit,  $di/dt$  may be:  $(0A - 100A) / 10ns = -10^{10} A/s$

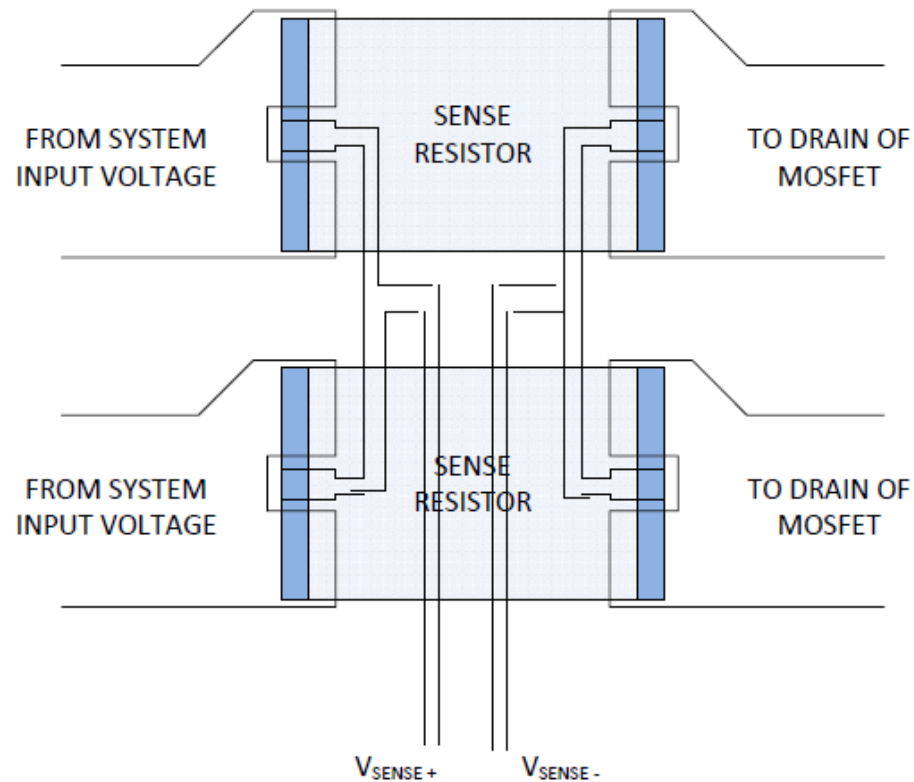
Trace inductance may be as low as 10nH.

$V_L = 10nH * -10^{10} A/s = -100V \rightarrow$  Both inductors will produce -100V.

This results in a positive voltage transient on the input and a negative transient on the output. A high power TVS on the input and Schottky on the output will clamp these voltages.

# Layout Considerations

- Multi Sense Resistor Layout

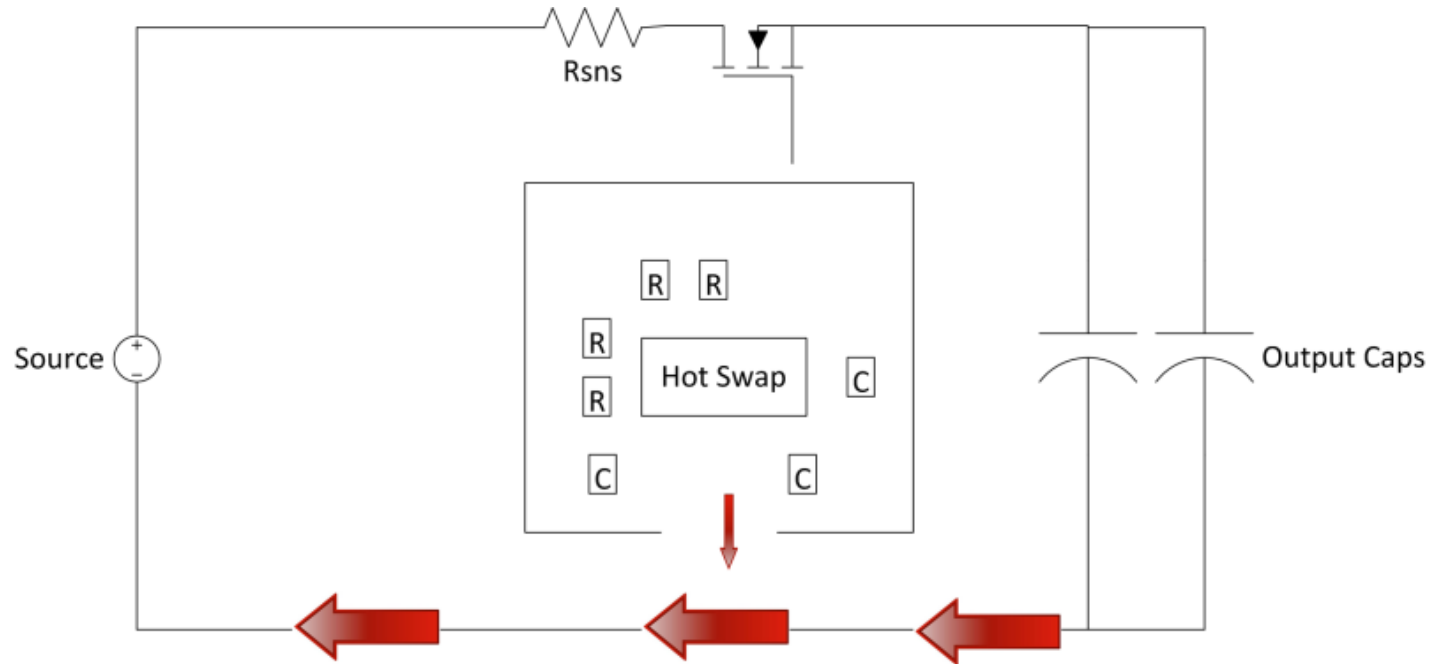


- 4-pad sensing:

- [https://e2e.ti.com/blogs\\_/b/powerhouse/archive/2014/10/30/choosing-the-right-sense-resistor-layout](https://e2e.ti.com/blogs_/b/powerhouse/archive/2014/10/30/choosing-the-right-sense-resistor-layout)

# Layout Considerations

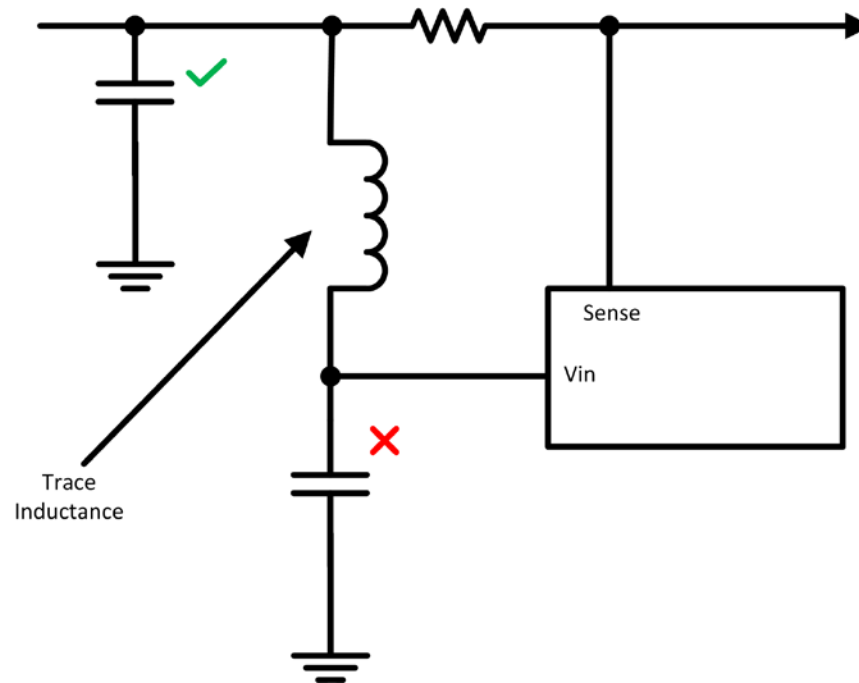
- **Ground plane cutout**



- **Prevents differential voltage from forming across the IC's ground and surrounding passive component grounds.**

# Layout Considerations (cont'd)

- Input Capacitor Placement



- Prevents differential voltage from forming across the IC's Vin and Sense pins.



# TI Solutions for 12V Hot Swap

	Telemetry	Analog
<5A	LM25066 + CSD17553 TPS2480 + CSD17553 *	TPS2590, TPS2592x (Integrated FET)
5A – 10A	LM25066 + CSD17553 TPS2480 + CSD17553*	TPS2475x (Integrated FET) * TPS24710 + CSD17553
10 A to 20A	LM25066 + CSD17573 TPS2480 + CSD17573 *	TPS24710 + CSD17573 TPS24720 + CSD17573 TPS2477x + CSD17573 (240 VA)
20-40A	LM25066 + CSD17570 * TPS2480 + CSD17570	TPS24710/20 + CSD16415 TPS2477x + CSD17570 *
>40A	LM25066 + CSD16415 * LM25066 + CSD17556 LM25066 + CSD17570 (If SC protection not req'd)	TPS2477x + CSD17570 (Low Cout) TPS2477x + CSD17556 (Med Cout) TPS2477x + CSD16415 (High Cout)

(\* ) TI Recommended

# Selection Table

	$V_{DS}$ (V)	$V_{GS}$ (V)	Package	$R_{DS(ON)}$ (m $\Omega$ ) TYP(10V)	$R_{DS(ON)}$ (m $\Omega$ ) MAX (10V)	SOA Current Rating (A) @ 14V Vds		Qg(nC) (TYP)
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<b>CSD16415Q5</b>	25	+16/-12	SON5x6	0.99	1.15	100	15	21

# Selection Table

Part number	Vin Range	Telemetry	Sense Voltage	Over Voltage Protection	FET SOA Protection	ILIM Accuracy
TPS24700/1	2.5V – 18V	No	25mV	No	No	10%
TPS24710/1/2/3	2.5V – 18V	No	25mV	No	Yes	10%
TPS24720	2.5V – 18V	Analog IMON	10 mV – 42.5 mV	Yes	Yes	10% @ 25mV
TPS2480/1	9.0V – 26V	I2C	50 mV	No	Yes	10%
TPS24770	2.5V – 18V	Analog Imon	10 mV – 200mV	Yes	Yes	5% @ 10mV
LM25061	2.9V – 17V	No	50mV	No	Yes	No
LM25069	2.9V – 17V	No	50mV	Yes	Yes	No
LM25066 family	2.9V – 17V	PMBus	26mV / 50mV	Yes	Yes	12% @ 26 mV 6% @ 50 mV