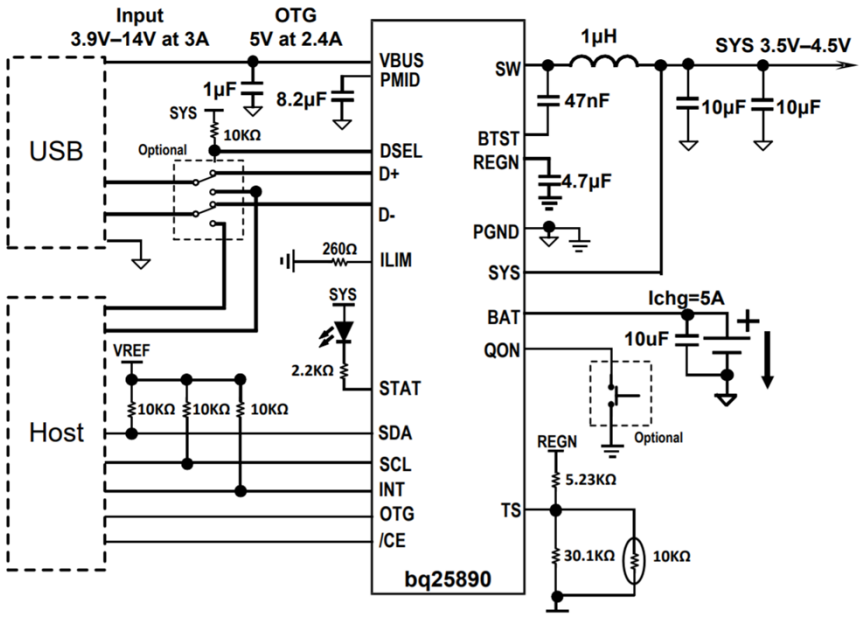
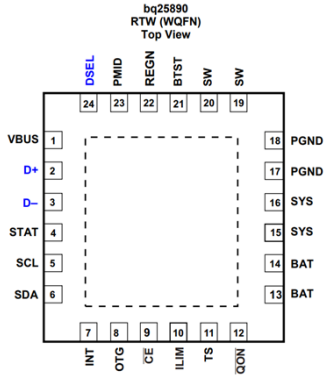
BQ25890 TYPICAL SCHEMATIC





BQ25890 SCHMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
D+/D-	2-3						USB data line pair	
		Optional					Positive line of the USB data line pair.	1. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2, and Adjustable high voltage adapter.
		Optional					Negative line of the USB data line pair.	2. If D+/D- based input current limit detection is not used, short D+/D- pins together or leave both pins open.
STAT	4						Open drain charge status output	
		Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ to 10-kΩ resistor.	1. If not used, leave it float. 2. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault condition occurs, STAT pin blinks in 1 Hz. The STAT pin function can be disabled when STAT_DIS bit is set.
SCL/SDA	5-6						I2C Interface clock and data	
		Optional	SCL resistor		10 kΩ		Connect SCL to the logic rail through a 10-kΩ resisto	If I2C communication is not used, leave it float.
		Optional	SDA resistor		10 kΩ		Connect SDA to the logic rail through a 10-kΩ resiste	If I2C communication is not used, leave it float.
INT	7						Open-drain Interrupt Output	
		Optional	INT resistor		10 kΩ		Connect the INT to a logic rail via 10-kΩ resistor.	1. If not used, leave it float. 2. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
OTG	8						Active high enable pin during boost mode.	
		Optional						1. If OTG boost mode is not used, short it to ground. 2. The boost mode is activated when OTG_CONFIG =1 and OTG pin is high
/CE	9						Active low Charge Enable pin.	
		Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when CHG_CONFIG = 1 and CE pin = Low.
ILIM	10						Input current limit Input.	
		Optional	ILIM resistor		* Ω		A resistor is connected from ILIM pin to ground to set the maximum limit as IINMAX = KILIM(390 max)/RILIM .	1. The actual input current limit is the lower limit set by ILIM pin (when EN_ILIM bit is high) or IIINLIM register bits. Input current limit of less than 500 mA is not support on ILIM pin. 2. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V. 3. If ILIM pin is short, the input current limit is set by the register. 4. The ILIM pin function can be disabled when EN_ILIM bit is 0.
TS	11						Temperature qualification voltage input.	
		Required	TS resistors and thermistor				Connect a negative temperature coefficient thermistor. Recommend 103AT-2 thermistor.	  1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
/QON	12						BATFET enable/reset control input.	
		Optional			Switch			If not used, leave it float. The pin contains an internal pull-up to maintain default high logic.
DSEL	24						Open-drain D+/D- multiplexer selection output.	
		Optional	DSEL resistor		10 kΩ		Connect DSEL to a logic rail via a 10-kΩ resistor.	1. If not used, leave it float. 2. The pin is normally float and pull-up by external resistor.
VBUS	1						Input source to the charger	
		Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
PMID	23						Actual input source to the charger	
		Required	PMID caps	8.2uF				Given the total input capacitance, put 1 µF on VBUS to PGND and the rest capacitance on PMID to PGND.
VBAT	13-14						Positive battery connection point	
		Required	VBAT caps	10uF	10uF			1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.
VSYS	15-16						System connection point.	
		Required	VSYS caps	20uF	20uF	40uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.
SW	19-20						Switching node connecting to output inductor.	
		Required	Output inductor	1uH		2.2uH		The charger device has internal loop compensator. To get good loop stability, 1-µH and minimum of 20-µF output capacitor is recommended.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required.Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	21						PWM high side driver positive supply.	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor snubbing resistor	Help with EMI performance. Recommend unpopulated footprint on new designs.
REGN	22						PWM low side driver positive supply output.	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10 V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PGND	17-18						Power ground connection for high-current power converter node.	
		Required						On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.
PowerPAD		Required						Always solder PowerPAD Pad to the board, and have vias on the PowerPAD plane star-connecting to PGND and ground plane for high-current power converter.