Current Phase Lead Compensation in Single-Phase PFC Boost Converters with a Reduced Switching Frequency to Line Frequency Ratio

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Abstract - **Traditional design of the current loop controller in a single-phase PFC boost converter is not suitable for applications with higher line frequencies (up to 800 Hz) because of the zero-crossing distortion and high harmonic content due to the current phase lead effect. Increasing the control bandwidth and switching frequency in order to avoid this effect would reduce converter efficiency and is objectionable. The paper presents the leading-phase admittance cancellation (LPAC) technique, which improves the current-shaping control structure and eliminates the current phase lead without increasing the bandwidth requirement. The LPAC method extends the allowable line frequency range from $^1/_{150}$ to $^1/_5$ of the current loop bandwidth. The LPAC method is load-invariant and superior to other previously proposed methods. The LPAC network can be added to existing designs, which would require only two passive components in the simplest case.**

I. INTRODUCTION

The boost topology is a popular choice for a single-phase ac-dc preregulator with high power factor and low harmonic distortions of the ac line current. This converter employs a two-loop control system, with an inner "current" loop shaping the sinusoidal current drawn from the line, and the outer "voltage" loop maintaining the dc output voltage at the required level [1]. The boost converter operating in continuous current conduction mode (CCM) with average current mode control (ACMC) is a preferred choice for PFC converters with higher power rating. This paper is focused on performance improvement of the current loop controller of the converter operating in CCM with ACMC. Although the PFC boost converter operating in discontinuous or critical conduction mode is easier to control, these modes are restricted to relatively low power levels because of higher than in CCM current stress on semiconductor devices, higher current ripple, and varying switching frequency.

The bandwidth of the current loop controller should be high enough to pass all significant harmonics of the rectified sine wave. For the utility line frequency (50-60 Hz), it should be around 10 kHz [1]. Because the control loop bandwidth may not be larger than $^1/_5$ of the switching frequency, this requirement further translates into a switching frequency in excess of 50 kHz, with typical values approaching 100 kHz [2, 3]. In other words, with traditional current loop design, the switching frequency to line frequency ratio should be at least 1000, or the loop crossover frequency to line frequency ratio should be at least 150. If this ratio is much smaller, a zero-crossing distortion of the line current waveform appears due to the leading phase of the current relative to the line voltage. This leading phase is a result of control action of the current loop compensation scheme [4, 5]. A PFC converter with a zero-crossing distortion of the line current may not be able to meet harmonic distortion requirements.

At the utility line frequencies (50-60 Hz) and power level less than 1 kW, these requirements for frequency ratios usually do not present a problem. In some other applications, these ratios may be impossible or impractical to realize. For example, future aircraft power systems will utilize much higher frequencies (360 Hz to 800 Hz [4-7]). Increasing the control loop bandwidth in order to avoid the zero-crossing distortion effect would require the switching frequency to be extended to hundreds of kilohertz, which would reduce converter efficiency and may be impractical. Another example is medium- and high-power (above 10 kW) single-phase PFC applications operating at the utility line frequency. These converters would greatly benefit from lower switching frequency (30 kHz or less). As a better alternative to using inefficient "brute-force" designs to comply with the above stated bandwidth requirement, this paper suggests making modifications to the standard current loop controller in order to eliminate the cause of the leading-phase distortion of the line current.

Among previously proposed methods to alleviate this problem are modification of the current reference signal [4, 5, 8], which is load-dependent and best implemented with DSP control, and various types of voltage feedforward schemes [9-12]. Some of these schemes use signal-by-signal division in the control law formula and are complicated for analog implementation [10-12]. An analog circuit based on two op-amps is suggested to implement a feedforward control law proposed in [9]. This law was shown to have some sensitivity to the boost inductance variation.

In this paper, a closed-loop dynamic model of the boost PFC converter is newly derived from first principles. The reasons for the current phase lead and possible ways to eliminate it become readily apparent from the model. The leading-phase admittance cancellation (LPAC) method allows operation without the current phase lead and the zero-crossing distortion at 360-800 Hz with a standard converter designed for 60 Hz with the switching frequency less than 50 kHz. This

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TABLE I
HARMONIC DISTORTIONS VS. CURRENT LOOP BANDWIDTH

Crossover frequency	300 Hz	600 Hz	1200 Hz	6 kHz
f_{cr} / f_g	5	**10**	20	100
THD	8.85%	**3.52%**	1.37%	0.17%
phase shift	8.4º	**4.9º**	2.7º	0.6º
displacement factor	0.989	**0.996**	0.999	1.0
distortion factor	0.996	**0.999**	1.0	1.0
power factor	0.985	**0.996**	0.999	1.0
3rd harmonic	4.41%	**1.29%**	0.35%	0.02%
5th harmonic	3.64%	**1.20%**	0.35%	0.02%
7th harmonic	2.99%	**1.10%**	0.34%	0.02%
9th harmonic	2.50%	**1.00%**	0.33%	0.02%
11th harmonic	2.13%	**0.91%**	0.31%	0.02%
13th harmonic	1.85%	**0.82%**	0.30%	0.02%

method allows simple analog implementation and can be added to existing converters without their redesign. The method is load-invariant, line voltage-invariant, and is not sensitive to the boost inductance variation.

In order to appreciate possible benefits of elimination of the current phase lead and zero-crossing distortion, consider the closed-loop line-voltage-to-current transfer function of the boost converter approximated by a first-order low-pass filter with a given cutoff frequency (equal to the open-loop crossover frequency). Table I shows harmonic characteristics of the line current at 60 Hz line frequency. The harmonics were calculated by passing rectified line voltage through the low-pass filter to obtain a rectified current waveform, then using it to reconstruct the ac current waveform. If the maximum odd harmonic limit is 4% and the THD limit is 5% (IEEE Standard 519), then current loop bandwidth of 600 Hz should provide a current waveform with acceptable quality. Consequently, the switching frequency does not have to be higher than 6 kHz. This control design corresponds to the crossover frequency to the line frequency ratio of only 10, and the switching frequency to the line frequency ratio of only 100. Although the closed-loop transfer function of the converter is not exactly a first-order low-pass filter, this example gives us an estimate of possible improvement.

II. SYSTEM MODELING

Traditional design of a PFC boost converter utilizes a two-loop control structure (Fig. 1), with an outer voltage-regulating control loop providing reference to an inner current-shaping loop [1]. In practice, the dc link capacitance C is large enough such that it could be treated as a voltage source. Under this assumption, dc voltage V_o and the voltage loop compensator output V_c are constant values. Then, the dynamic model of the converter is described by the block diagram in Fig. 2. The power stage line-to-current and control-to-current transfer functions are

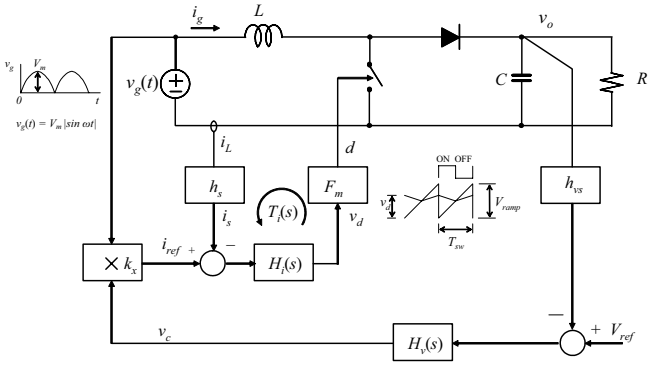


Fig. 1. PFC boost converter control diagram (H_i – current loop compensator, H_v – voltage loop compensator, F_m – modulator gain, k_x – multiplier gain, h_s – current sensor gain, h_{vs} – voltage sensor gain).

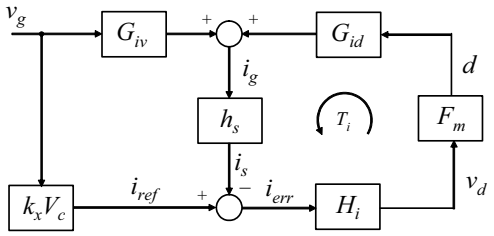


Fig. 2. PFC boost converter current loop control diagram in terms of transfer functions (G_{iv} and G_{id} – power stage transfer functions, k_xV_c – current reference gain).

$$G_{iv}(s) = \frac{1}{r + s\,L} \quad \text{and} \quad G_{id}(s) = \frac{V_o}{r + s\,L}, \tag{1}$$

where r is an equivalent resistance of the current path. This resistance does not noticeably affect closed-loop transfer functions. The compensator is a PI-type controller with the zero placed at or near the loop crossover frequency [1]:

$$H_i(s) = \frac{\omega_i\left(1 + \dfrac{s}{\omega_z}\right)}{s\left(1 + \dfrac{s}{\omega_p}\right)}. \tag{2}$$

The line voltage v_g is scaled down by the gain k_xV_c to produce current reference i_{ref} for the control loop.

From Fig. 2, it is seen by inspection that current i_g is a sum of two terms:

$$i_g(s) = \frac{G_{iv}}{1 + T_i} v_g(s) + \frac{G_{id}\,F_m\,H_i}{1 + T_i} k_x V_c\, v_g(s). \tag{3}$$

Therefore, the closed-loop input admittance transfer function (which is similar to the generic form reported in [13]) is

$$Y(s) = \frac{i_g(s)}{v_g(s)} = \frac{G_{iv}}{1 + T_i} + \frac{G_{id}\,F_m\,H_i}{1 + T_i} k_x V_c, \tag{4}$$

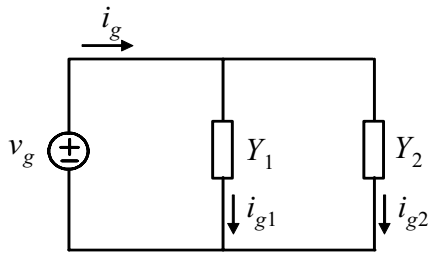


Fig. 3. Closed-loop input admittance represented by two branches.

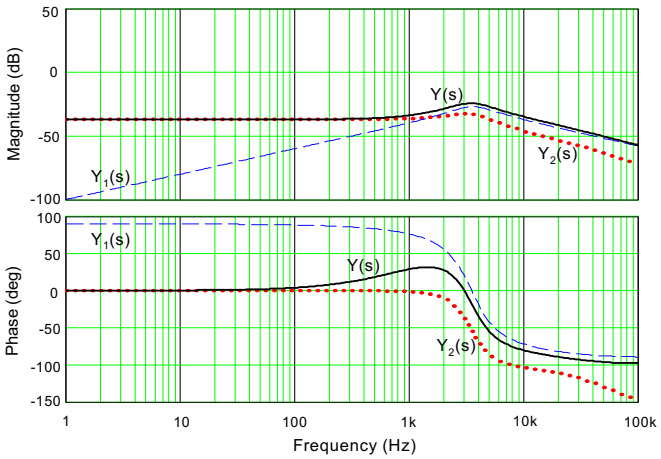


Fig. 4. Closed-loop input admittance and its components.

or
$$Y(s) = G_{ivcl} + T_{icl}\, k_x V_c, \tag{5}$$

where
$$T_i = G_{id}\, F_m\, H_i\, h_s \tag{6}$$

is the loop gain transfer function, and

$$T_{icl} = \frac{G_{id}\, F_m\, H_i}{1 + T_i} \tag{7}$$

is the closed-loop control-to-current transfer function.

We can think of admittance $Y(s)$ as consisting of two components, or two branches $Y_1(s)$ and $Y_2(s)$, each drawing its own current from the source (Fig. 3). Below the crossover frequency, neglecting r,

$$Y_1(s) = G_{ivcl} = \frac{s}{V_o\, F_m\, h_s\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)} \tag{8}$$

and

$$Y_2(s) = T_{icl}\, k_x V_c = \frac{k_x V_c}{h_s} = Y_{CL0} = \frac{I_{grms}}{V_{grms}} = \frac{P_g}{V_{grms}^{\,2}}. \tag{9}$$

Component $Y_2(s)$ is the closed-loop current-reference-to-current transfer function (current reference term), which provides desired input admittance magnitude with zero phase below crossover frequency of the loop gain T_i. This branch of the input admittance draws a current in phase with the line voltage, with the magnitude determined by V_c, which corresponds to the load power. Component $Y_1(s)$ is the closed-loop voltage-to-current transfer function (voltage term, or leading-phase admittance term), which has a 90º leading phase below the crossover frequency. This branch draws a leading-phase current, which is independent of the converter load and increases with the line frequency for a given current loop bandwidth. The magnitude of this current is low at 60 Hz but may become large enough in the frequency range of 360-800 Hz such that the phase of the total input admittance is no longer zero (Fig. 4), which is in agreement with results obtained in [8]. This is the reason why the current phase lead effect may be observed at these frequencies, which causes the zero-crossing distortion of the line current and increased harmonic content [4, 5, 8].

III. Current Phase Lead Compensation

A. Current Reference Correction

From the discussion above, it is clear that we need to compensate the effect of admittance component $Y_1(s)$ in order to eliminate the current phase lead and the resulting zero-crossing distortion. The current reference correction (CRC) method compensates for the effect of $Y_1(s)$ indirectly by using a corrective transfer function $K(s)$ in the current reference path (Fig. 5) so that

$$Y(s) = G_{ivcl} + T_{icl}\, k_x\, V_c\, K(s). \tag{10}$$

$K(s)$ is determined from the condition $Y(s) = Y_{CL0}$ below the crossover frequency. From (8) and (9),

$$Y(s) = \frac{s}{V_o\, F_m\, h_s\, \omega_i \left(1 + \dfrac{s}{\omega_z}\right)} + \frac{k_x V_c}{h_s} K(s) = Y_{CL0},$$

from which

$$K(s) = \frac{1 + \dfrac{s}{\omega_{zk}}}{1 + \dfrac{s}{\omega_z}}, \tag{11}$$

where
$$\omega_{zk} = \left(\frac{1}{\omega_z} - \frac{1}{k_x V_c V_o F_m \omega_i}\right)^{-1}.$$

In Fig. 3, this is equivalent to creating a phase lag in the current drawn by $Y_2(s)$ such that it compensates the leading-phase current drawn by $Y_1(s)$. The results in Fig. 6 show that the frequency range of undistorted current operation is drastically extended for more than a decade. The expression for $K(s)$ is load-dependent (ω_{zk} is a load-dependent zero); therefore, $K(s)$ is best implemented using digital control. Adding a corrective transfer function into the current reference path was previously proposed in [4], which also suggested a load-invariant form of $K(s)$:

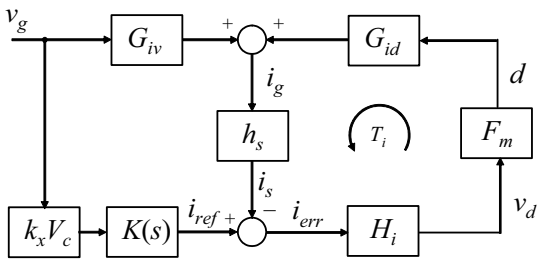


Fig. 5. Current phase lead compensation using current reference correction.

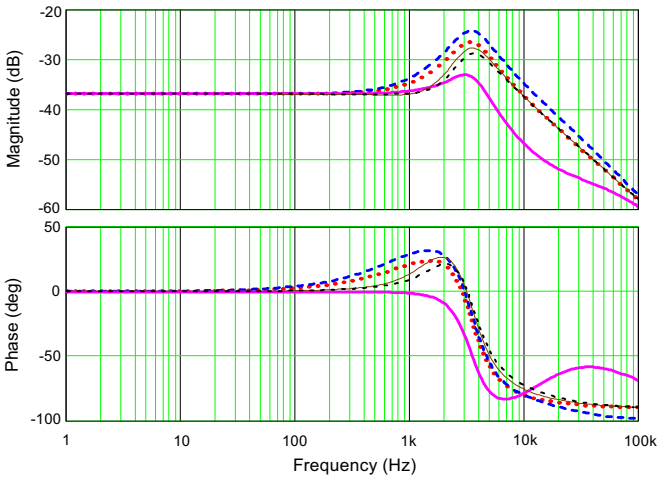


Fig. 6. Closed-loop input admittance with current reference correction: dash – uncorrected, solid thick – exact formula (11), dot – simple approximation (12), solid thin – better approximation (13), dash-dot – double-pole approximation (14).

$$K(s) = \frac{1}{1 + s/\omega_z}. \tag{12}$$

However, simply neglecting ω_{zk} yields only a marginal improvement over uncompensated $Y(s)$ for given load conditions as shown in Fig. 6 (dotted line). Location of ω_{zk} depends on the load and may be in the right- or left-half-plane, and the zero's effect may be significant. If an approximation in the form of (12) must be used, it is better to adjust location of the pole for predominant load conditions to yield the maximum benefit. Even better results can be achieved by adding a second pole or a zero. As shown in Fig. 6, better compensation is achieved using

$$K(s) = \frac{1}{1 + \dfrac{s}{0.4\,\omega_z}} \quad \text{(solid thin line)} \tag{13}$$

and

$$K(s) = \frac{1}{\left(1 + \dfrac{s}{0.8\,\omega_z}\right)^2} \quad \text{(dash-dot line).} \tag{14}$$

However, the best approach to eliminate the current phase lead and the resulting zero-crossing distortion is the load-invariant leading-phase admittance cancellation method described next.

B. Leading-Phase Admittance Cancellation

The two-component structure of the input admittance (4) suggests a natural way to eliminate phase lead in $Y(s)$ by adding a third component that cancels the effect of the first one. The leading-phase admittance cancellation (LPAC) method uses an additional term $Y_3(s)$ in the admittance equation to cancel the leading-phase term $Y_1(s)$. Then, the current reference term is left as the only one that determines the magnitude and phase of the line current. A new input from v_g with a transfer function $H_c(s)$ is introduced at the summing junction in order to cancel the undesired voltage term in (4) as shown in Fig. 7 (solid line). This approach has an advantage of using the existing error amplifier input for LPAC implementation. Then,

$$Y(s) = G_{ivcl}(s) + T_{icl}(s)\,k_x V_c + T_{icl}(s)\,H_c(s). \tag{15}$$

$H_c(s)$ is determined from the condition $Y(s) = Y_{CL0}$ below the crossover frequency. Using (8) and (9),

$$H_c(s) = -\frac{1}{V_o F_m H_i(s)} = -\frac{s}{V_o F_m \omega_i \left(1 + \dfrac{s}{\omega_z}\right)}. \tag{16}$$

As an alternative, the new input can be introduced into the loop after $H_i(s)$ as shown in Fig. 7 (dash line):

$$Y(s) = G_{ivcl}(s) + T_{icl}(s)\,k_x V_c + \frac{G_{id}(s)\,F_m}{1 + T_i(s)}\,H_{c1}(s), \tag{17}$$

from which

$$H_{c1}(s) = -\frac{1}{V_o F_m}, \tag{18}$$

approximated as a static gain below the crossover frequency.

As shown in Fig. 8, addition of $H_c(s)$ or $H_{c1}(s)$ is equivalent to adding a new branch $Y_3(s)$, which draws a current opposite to the current of $Y_1(s)$ and, thus, cancels its effect at frequencies within the current loop bandwidth. The results in Fig. 9 demonstrate that the frequency range of undistorted current operation is drastically extended for more than a decade. At 800 Hz, which is $^1/_5$ of the crossover frequency (4 kHz), the phase shift is less than 1°. Unlike $K(s)$ in the CRC method, $H_c(s)$ and $H_{c1}(s)$ are independent of load power.

C. Implementation of the LPAC

A generic implementation of the LPAC in a standard PFC control system is shown in Fig. 10. $H_c(s)$ is part of the compensator circuit; it is added to the system by means of an R_c-C_c network from the rectified line voltage to the negative input of the current loop amplifier. Assume for generality that the R_c-C_c circuit is connected to v_g through a gain h_c. Then,

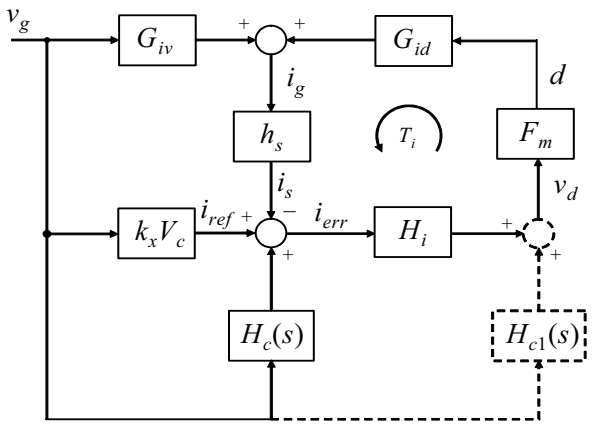


Fig. 7. Two ways of implementing the leading-phase admittance cancellation for current phase lead compensation.

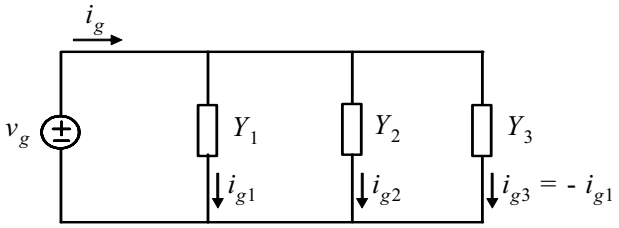


Fig. 8. Elimination of the current phase lead by canceling the current in the leading-phase admittance branch.

$$H_c(s)\,H_i(s) = \frac{v_d(s)}{v_g(s)} = -\frac{h_c\left(R_f + \dfrac{1}{s\,C_{fz}}\right) \| \dfrac{1}{s\,C_{fp}}}{R_c + \dfrac{1}{s\,C_c}}, \qquad (19)$$

$$H_c(s) = -\frac{C_c\,h_c}{C_{fp} + C_{fz}} \frac{s}{\omega_i\left(1 + \dfrac{s}{\omega_c}\right)}, \qquad (20)$$

where

$$\omega_c = \frac{1}{C_c\,R_c}. \qquad (21)$$

Comparing (20) with (16), we obtain

$$\omega_c = \omega_z, \qquad C_c = \frac{C_{fp} + C_{fz}}{V_o\,F_m\,h_c}, \text{ and } \qquad R_c = \frac{1}{C_c\,\omega_z}. \qquad (22)$$

The R_c-C_c circuit can be added to an existing converter without its redesign. In the simplest case, only two components (R_c and C_c) are needed. Fig. 10 shows how the LPAC can be implemented in a controller made of general-purpose components. A controller based on the UC3854 chip [14] would use the same way of connecting the LPAC network (Fig. 11). Another IC, UCC3817 [15], uses an additional inversion in the current loop and will require an inverted v_g signal to be applied to the R_c-C_c circuit (Fig. 12). Then, h_c is equal to the inverting amplifier gain. The inverting amplifier will need a negative supply voltage, which may be an undesirable requirement. An LPAC implementation shown

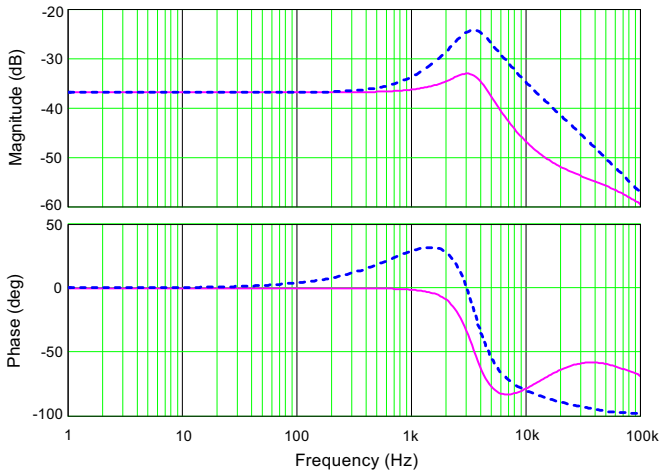


Fig. 9. Closed-loop input admittance with leading-phase admittance cancellation: dash – uncompensated, solid – LPAC-compensated.

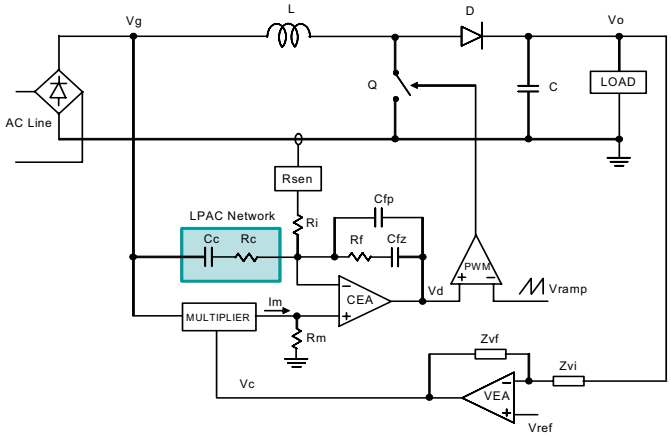


Fig. 10. Generic implementation of the LPAC as part of the current loop compensator circuit.

in Fig. 13 does not require a negative supply voltage while preserving advantages of the UCC3817 such as the leading-edge modulation and higher noise immunity of the current amplifier. This circuit is based on using $H_{c1}(s)$ as shown in Fig. 7 (dash line) and requires breaking the connection between the error amplifier and the comparator. A new control IC with included LPAC functionality could possibly be created, which would integrate amplifiers A_1 and A_2 in the chip. The scaling factor of the voltage divider R_1-R_2 is determined by (18).

Single-phase PFC converters are usually designed with a universal "worldwide" voltage input. In order to maintain the same power drawn from the line regardless of the line voltage, the current reference is scaled down as the line voltage increases. This feature does not affect the LPAC design. The LPAC network is used to cancel the leading-phase current component, which does not depend on the load power. From Fig. 8, it is obvious that, as i_{g1} would change following a v_g change, so should i_{g3}. While i_{g2}, which represents the real power, has to be adjusted for a v_g change, i_{g3} does not.

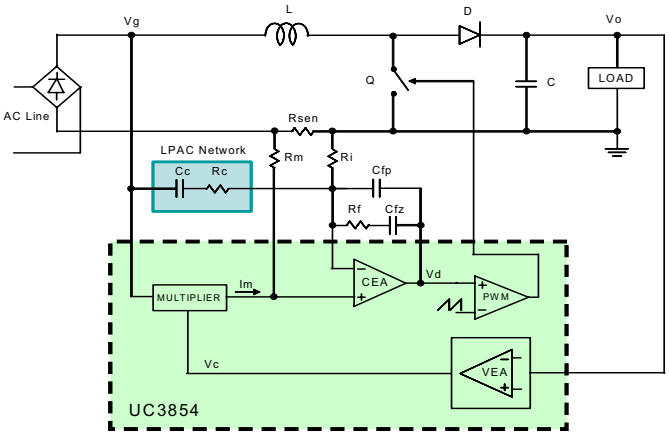


Fig. 11. The LPAC implementation in the UC3854-based controller.

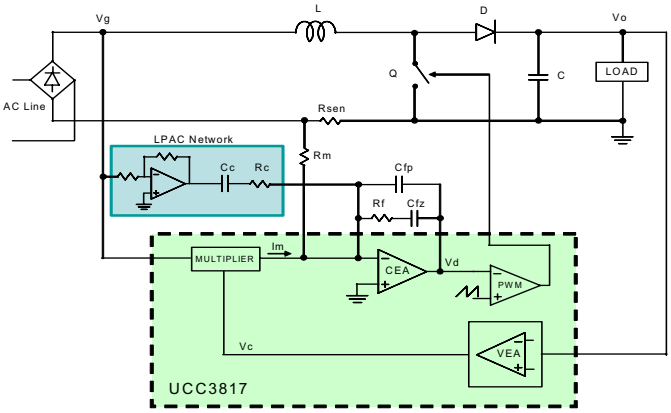


Fig. 12. The LPAC implementation in the UCC3817-based controller.

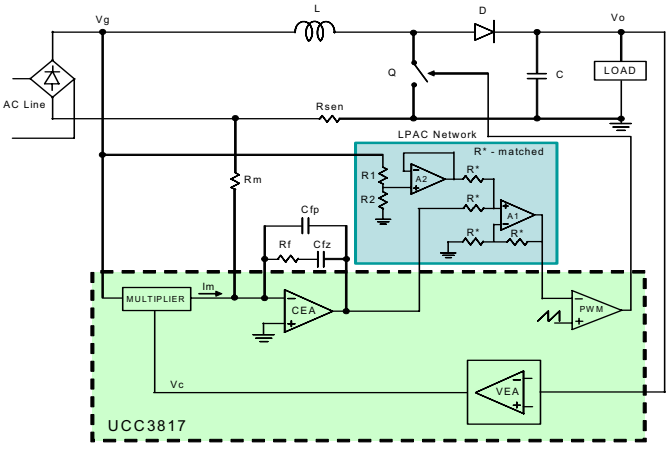


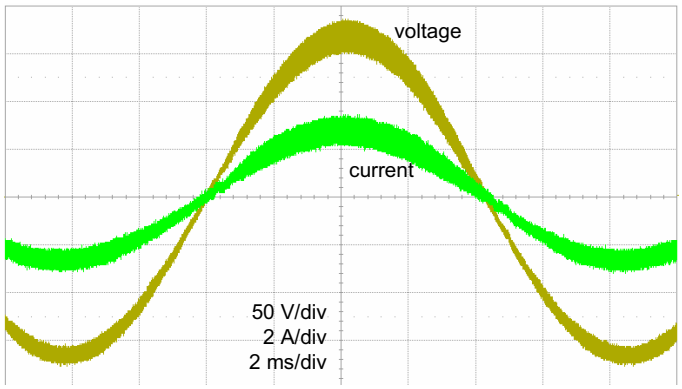
Fig. 13. The LPAC implementation in the UCC3817-based controller without using a negative supply voltage.

IV. Experimental Results

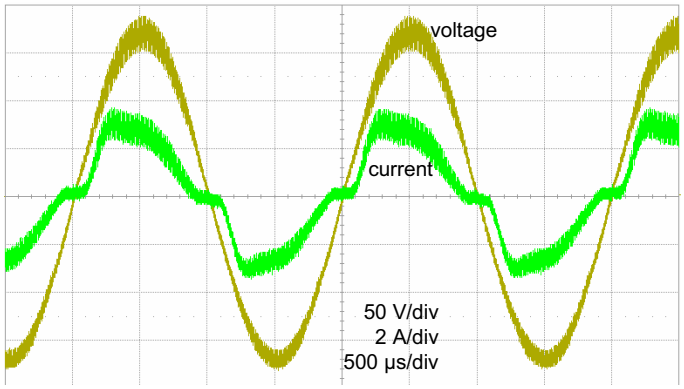
A PFC boost converter based on the UCC3817 Power Factor Preregulator IC was used to verify the LPAC method. The current loop was designed with 4 kHz bandwidth. At 500 Hz line frequency, the phase lead and the zero-crossing distortion of the line current are observed, but they completely disappear when the LPAC circuit is enabled. The circuit was tested with different switching frequencies down to 35 kHz. At 60 Hz, there is no leading-phase distortion (Fig. 14 (a)), and the LPAC does not have any effect on the current. However, at higher line frequencies, the distortion becomes severe. Fig. 14 (b) and Fig. 14 (d) show the line current distortion when the frequency is increased to 500 Hz. The current phase lead does not depend on the switching frequency, and a higher switching frequency by itself does not alleviate the distortion. Fig. 14 (c) and Fig. 14 (e) indicate that the sinusoidal current shape with zero phase shift at 500 Hz is completely restored when the LPAC network is enabled, which is in agreement with the Bode plots in Fig. 9. While the converter was not tested at 800 Hz because of the ac source limitations, the Bode plots show that this design can operate up to 800 Hz without distortion when the LPAC is enabled. The experiment proved that it is possible to build a PFC converter for the future aircraft line frequency range (360-800 Hz) with a relatively low switching frequency and a high quality line current waveform.

V. Conclusion

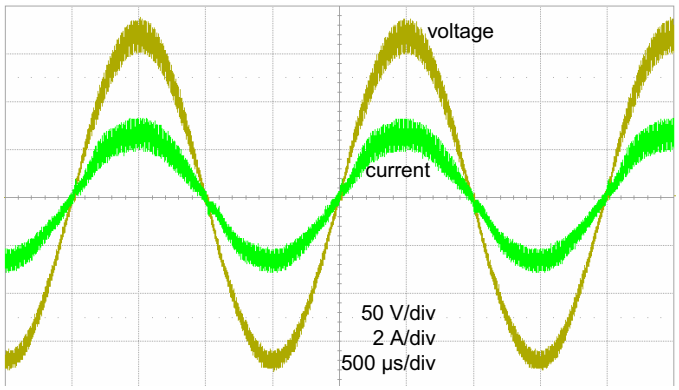
The leading-phase admittance cancellation (LPAC) method has been proposed and developed for the single-phase PFC boost converter in order to eliminate the leading-phase distortion of the line current at higher line frequencies. This technique extends the allowable range of line frequencies from about $^{1}/_{150}$ of the current loop bandwidth with traditional design to about $^{1}/_{5}$ with the LPAC. This method can be used with any PFC boost converter but is especially useful in applications with higher line frequencies such as aircraft power system (360-800 Hz) and in medium- and high-power (above 10 kW) single-phase PFC applications operating at the utility line frequency, which would benefit from a lower switching frequency (30 kHz or less). Unlike methods proposed in the past, the cancellation circuit added to the standard converter control system is load-invariant, line-voltage-invariant, and is not sensitive to the boost inductance variation. The LPAC method can be realized easily with only two passive components in the simplest case and can be applied to existing designs to extend their operating range of line frequencies or to lower their switching frequency in current operating conditions, thus improving the converter efficiency. The newly developed dynamic model of the system was used to determine component values of the LPAC network. Experimental results showed good agreement with simulation waveforms and confirmed effectiveness of the LPAC. It was shown theoretically and demonstrated experimentally that it is possible to build a PFC boost converter for the 360-800 Hz line frequency range with a relatively low switching frequency and high quality of the line current waveform. The principle of leading-phase admittance cancellation may also be applied to other PFC converter configurations.



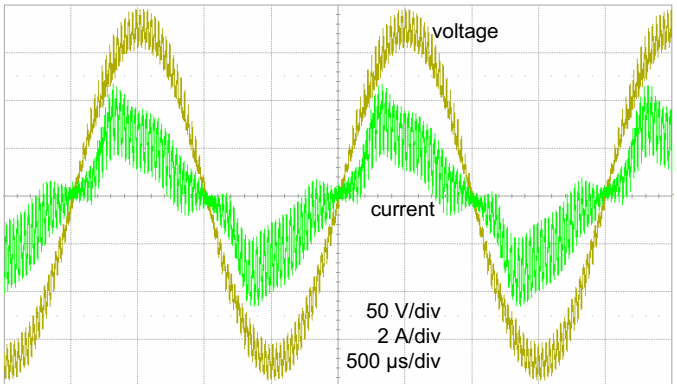
(a)



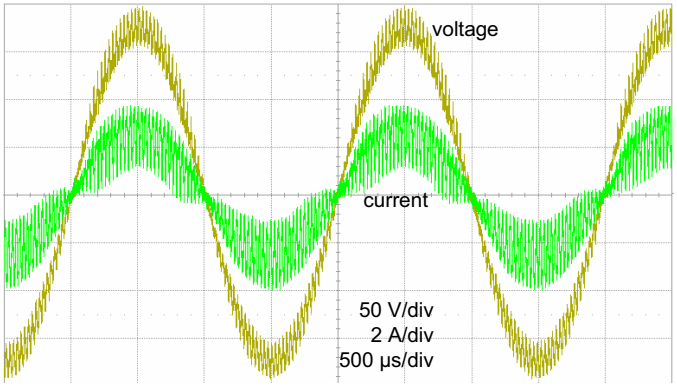
(b)



(c)



(d)



(e)

Fig. 14. (a) f_{line} = 60 Hz, f_{sw} = 90 kHz, standard controller, (b) f_{line} = 500 Hz, f_{sw} = 90 kHz, standard controller, (c) f_{line} = 500 Hz, f_{sw} = 90 kHz, with LPAC, (d) f_{line} = 500 Hz, f_{sw} = 35 kHz, standard controller, (e) f_{line} = 500 Hz, f_{sw} = 35 kHz, with LPAC.

APPENDIX

Converter parameters: L = 1 mH, R_{sen} = 0.33 Ω, F_m = 0.25, $R_m = R_i$ = 4 kΩ, R_{fz} = 3.3 kΩ, C_{fp} = 820 pF, C_{fz} = 12 nF, C_c = 2.7 nF, R_c = 20 kΩ, h_c = 0.054, V_o = 385 V.

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