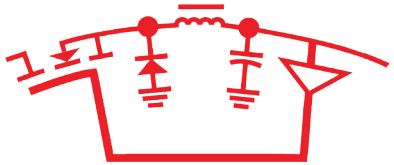

Power Supply Design Seminar

# Common Mistakes in DC/DC Converters and How to Fix Them

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Texas Instruments

# Common Mistakes in DC/DC Converters and How to Fix Them

**Pradeep Shenoy**

**Anthony Fagnani**



Texas Instruments

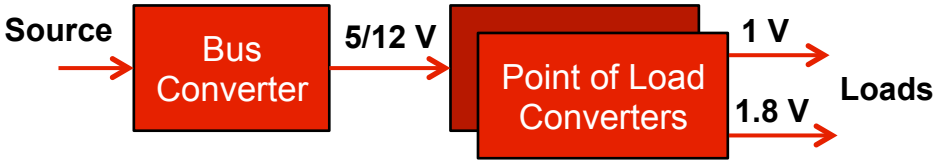
# Agenda

- Quick review
- 10 common mistakes and how to fix them
  - Converter capabilities and part selection
  - Component selection
  - Feature settings
  - Board layout
  - Measurement techniques
- Summary

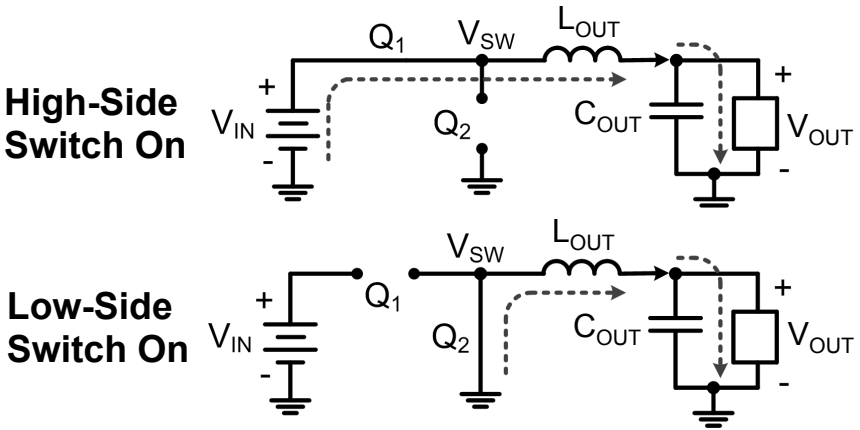
> *"Learn from the mistakes of others. You can't live long enough to make them all yourself."*
> - Unknown

# Quick Review

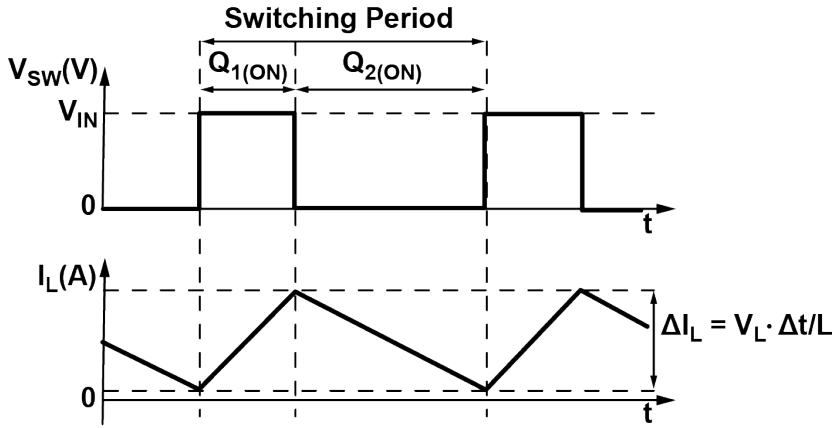
- DC/DC converters used as point-of-load voltage regulators
- Buck converter is most common topology




## Buck Converter Switching States



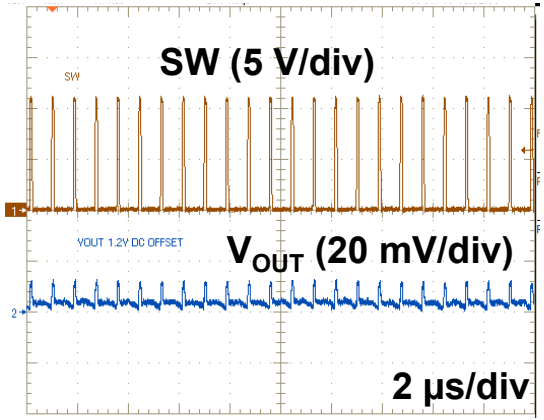

## Steady State Waveforms



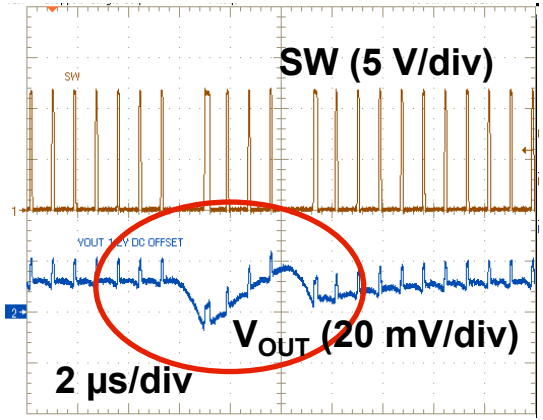
# 1) Why Are There Jumps in the Output Voltage?

Conditions: 1.2 V/0 A output, switching frequency ($f_{SW}$) = 1.2 MHz,
Forced continuous conduction mode (FCCM)

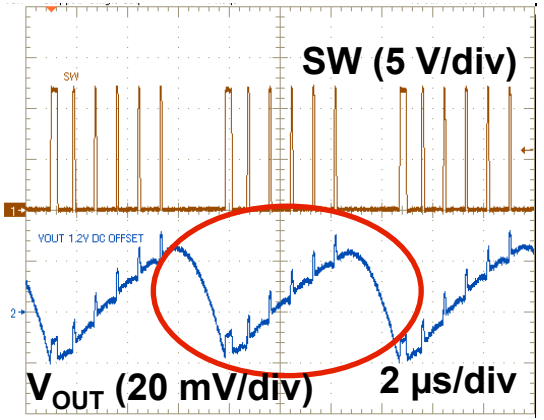
**11 V Input**




**11.7 V Input**




**12 V Input**




High-side switch **minimum on-time ($t_{ON}$) violation**
cannot output narrow enough SW node pulses

$$t_{ON} = \frac{1}{f_{SW}} \cdot \frac{V_{OUT}}{V_{IN}}$$

$$t_{ON} = 83\ ns$$

# 1) Duty-Cycle Limits Considerations

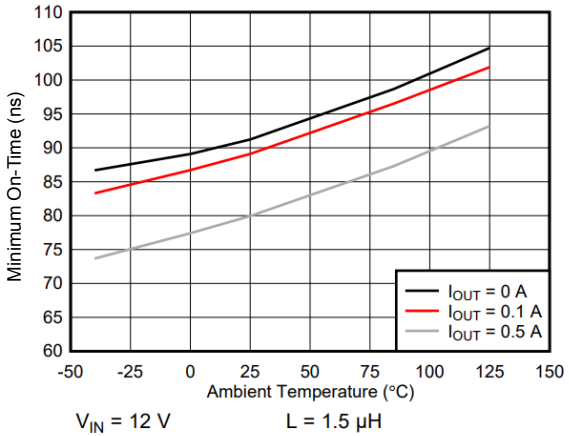
- Select switching frequency ($f_{SW}$) based on:
  - Maximum minimum on-time
  - Maximum input voltage

$$f_{SW} \le \frac{1}{t_{ON(MIN)}} \cdot \frac{V_{OUT}}{V_{I(MAX)}}$$

- If min on-time is violated converters will either:
  - Skip pulses
  - Change switching frequency
  - Output will become unregulated

- Minimum on-time varies with temperature, with load and from part to part

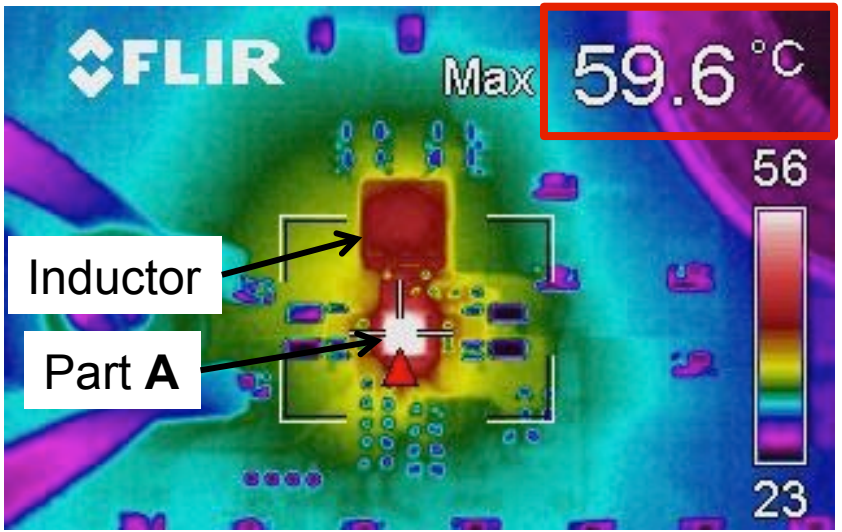
| MIN | TYP | MAX | UNIT |
|---|---|---|---|
| | 90 | 130 | ns |

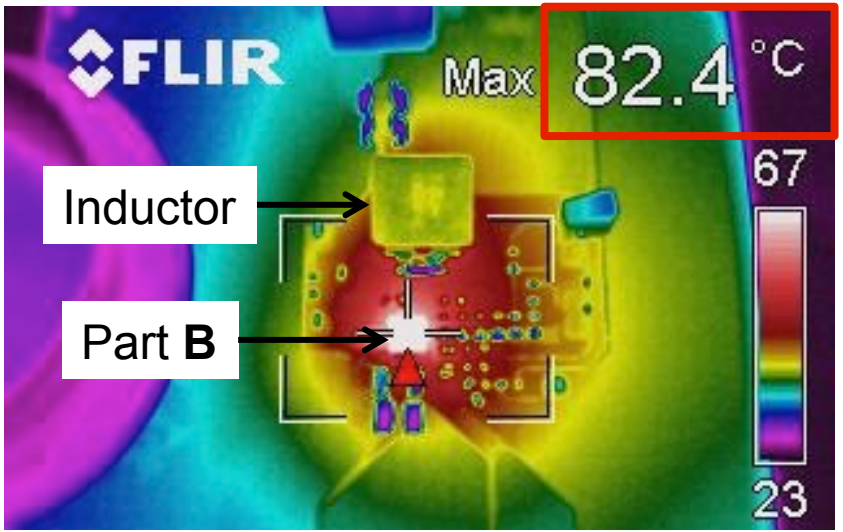


# 2) Which Part Is Rated for 8 A?

Conditions: 12 V, 1.8 V at 8 A, 700 kHz

**Both are 8 A parts!**



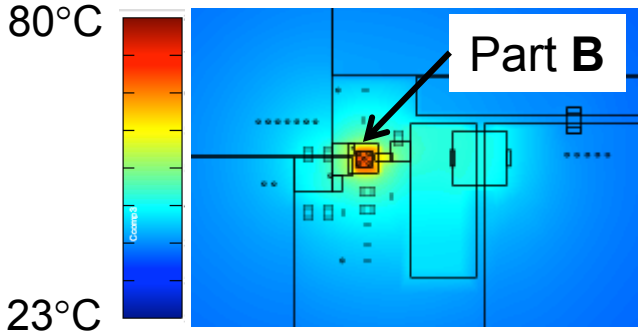




Part B gets **over 20°C hotter** and has a **larger thermal footprint**
Part B has **little margin** if 85°C ambient temperature due to 60°C temperature rise

# 2) Thermal Derating - Part Comparison

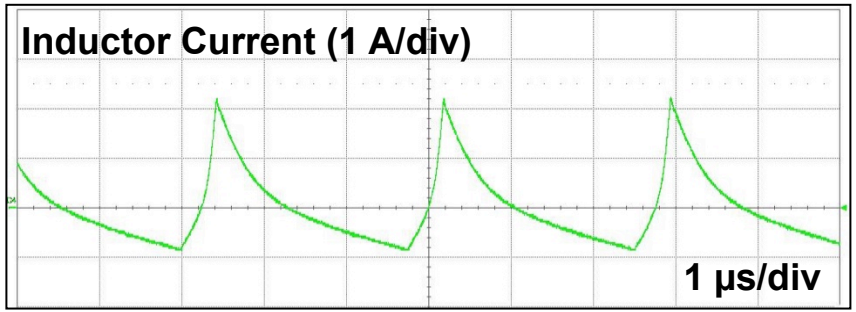
| Spec | Part A (TPS54824) | Part B (TPS54821) |
|---|---|---|
| $V_{IN}$ range | 4.5 – 17 V | 4.5 – 17 V |
| Current | 8 A | 8 A |
| Size | 3.5 x 3.5 mm | 3.5 x 3.5 mm |
| $R_{DS(ON)}$ | 14/6 mΩ | 26/19 mΩ |
| Modeled $P_{LOSS}$ | 1.69 W | 2.38 W |
| Simulated die temp | 64 °C | 81 °C |
| Price | $$ | $ |

- Part B can be used if 8 A is a short transient condition or low ambient temp
- Consider **average** current for thermals
- TI's WebTHERM™ online tool estimates thermal performance on EVMs

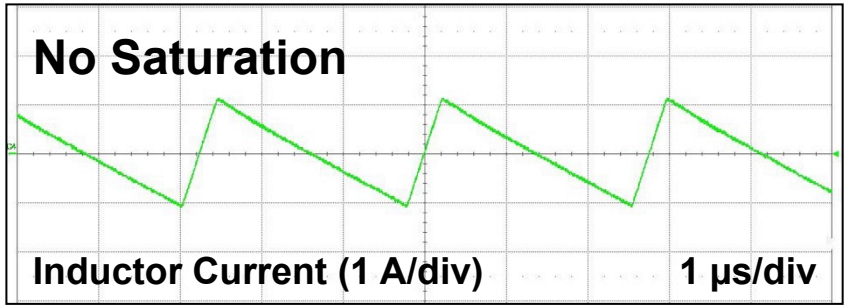



Part B Thermal Simulation Result

# 3A) What's Wrong with the Inductor Current?

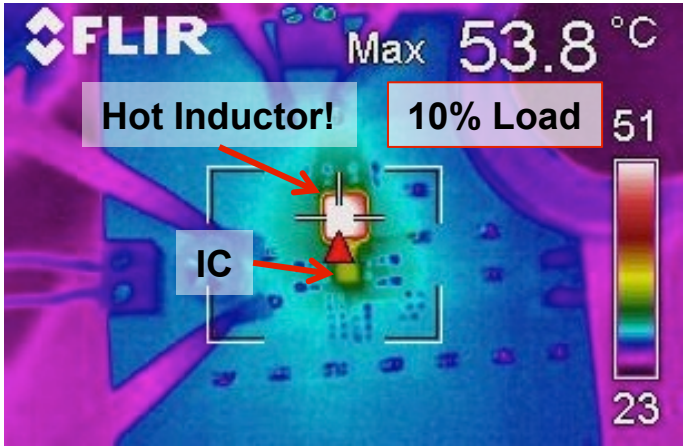



**Inductor Current Saturation!**

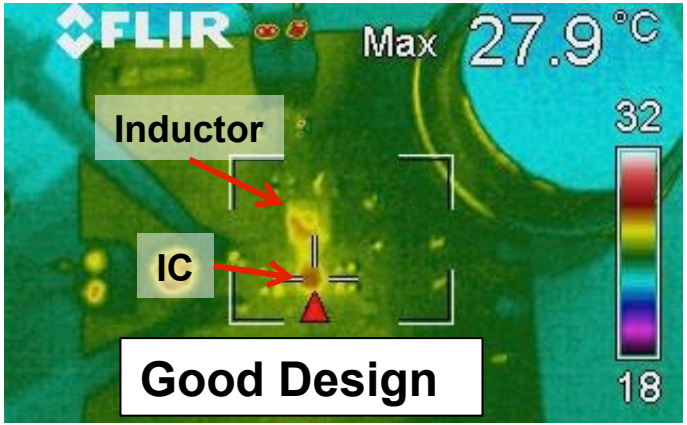



- Inductor current slope sharply increases when core saturates
  - Saturation → low core permeability
  - Causes peaking in current waveform of hard saturating cores
- Saturation can cause problems
  - Can **damage** converter
  - Leads to **premature overcurrent protection**
  - **Limits** converter output current
- Consider using an inductor with a **soft saturating** core

# 3B) Why Is the Inductor so Hot?




L = 240 nH → large inductor current ripple ($\Delta I_L$)! (over 100%)

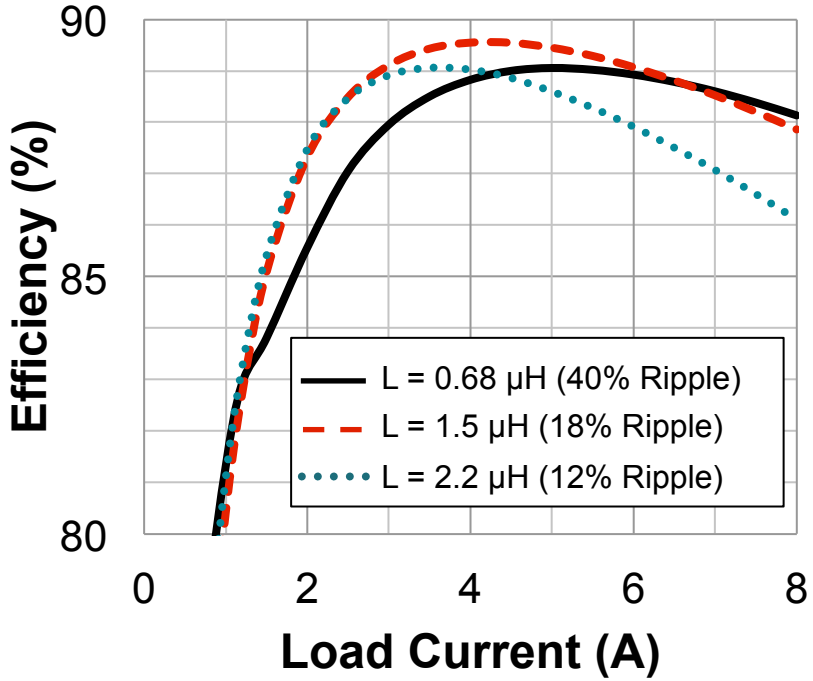



L = 1 µH, has ~30% ripple

$$P_{CORE} \approx k_0 f_{SW} B_{PK}^2 \propto k_0 f_{SW} \Delta I_L^2$$

**High core loss due to low inductance and high current ripple**

# 3) Inductor Selection Guidelines




*All inductors: same size, same vendor

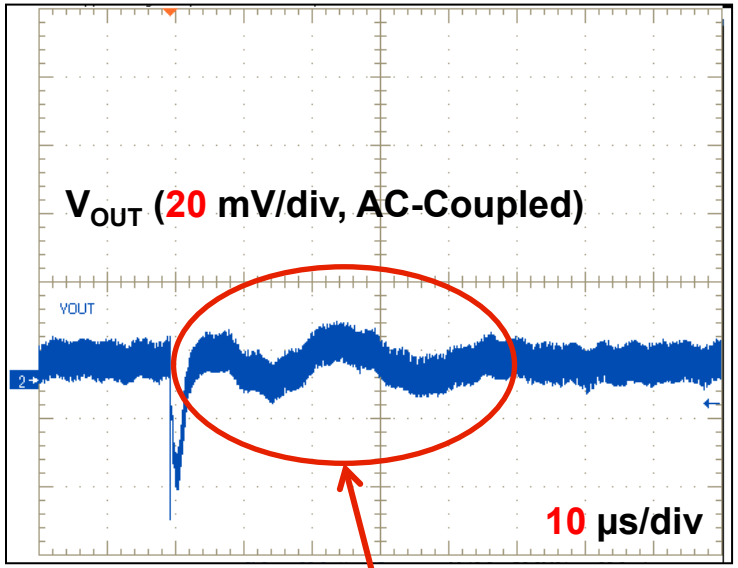
- Rule of thumb: current ripple between 15% and 40% of **max** load current

$$L = \left( \frac{V_{IN(MAX)} - V_{OUT}}{K \cdot I_{OUT}} \right) \left( \frac{V_{OUT}}{V_{IN(MAX)} \cdot f_{SW}} \right)$$

  - For **converters**, use **rated** load current of device
- Higher inductance tends to increase **peak efficiency**
  - Lower core loss/RMS currents
  - Slower transient response
- Lower inductance has higher **full load efficiency**
  - Lower winding resistance

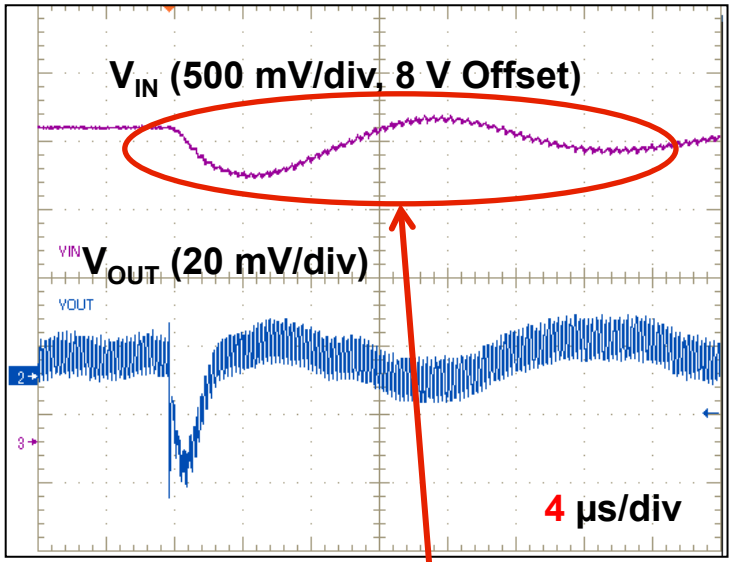
# 4A) What's Causing the Output Oscillation?

**10 V input**, 1.2 V output, 8 A load step-up




**Output oscillating after a load transient**

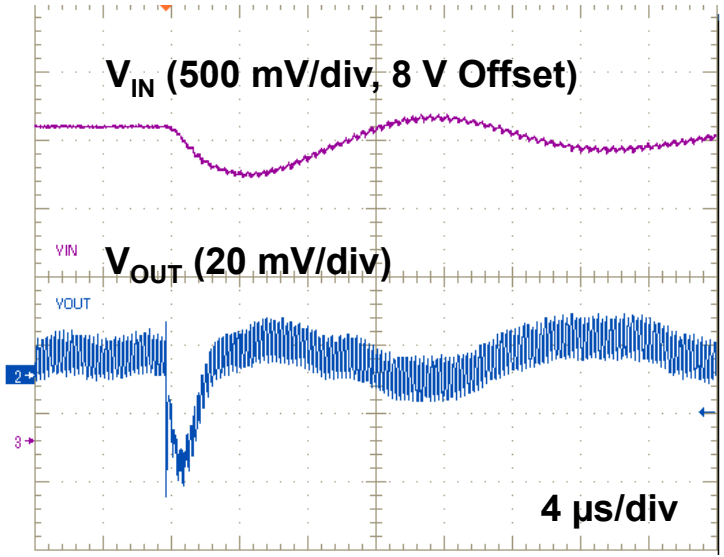
**Insufficient input decoupling capacitance!**



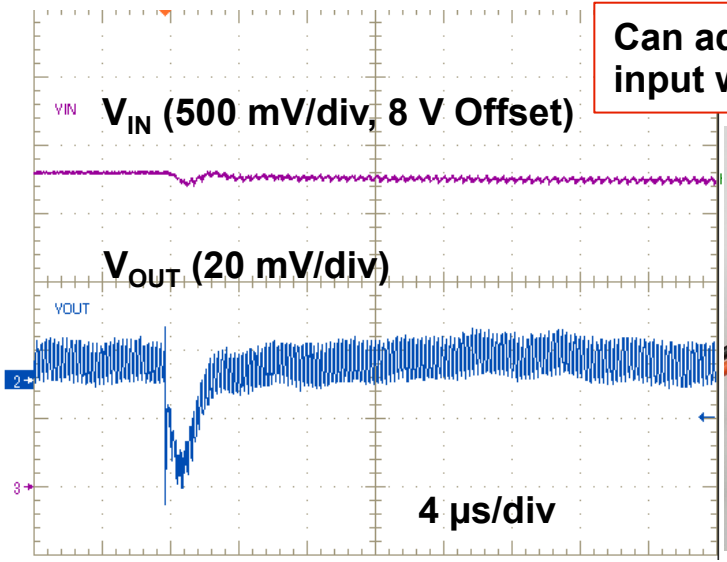

**Input voltage perturbations**

# 4A) Input Capacitance Comparison

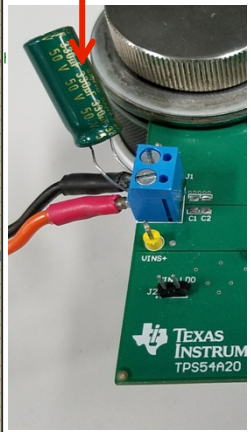
10 V input, 8 A load step-up
**No bulk decoupling input capacitance**




10 V input, 8 A load step-up
**With bulk decoupling input capacitance**




**Can add a bulk cap to input when testing**

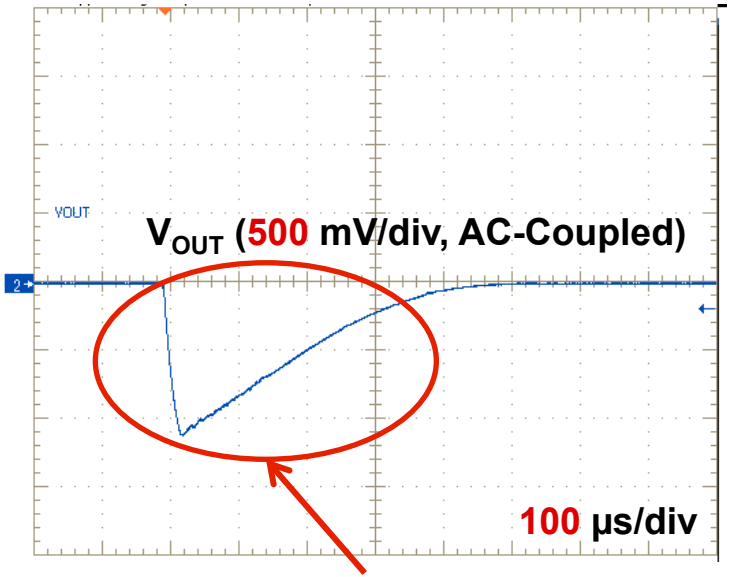



**Ensure bus converter is designed correctly to handle large load transients**

# 4B) Why Does the Output Voltage Collapse?

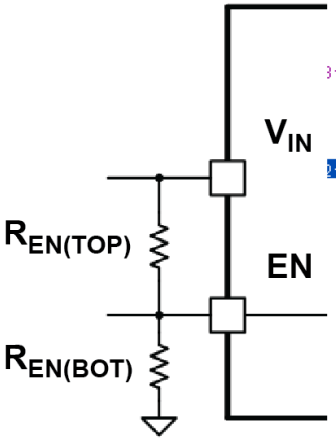
**Tripping undervoltage lockout (UVLO)!**

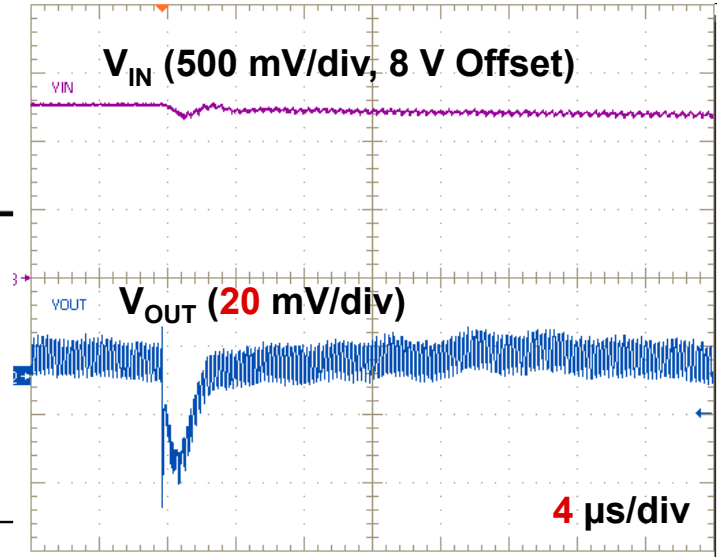
**9 V input**, 1.2 V output, 8 A load step-up




**Output collapses after a load transient**

EN falling threshold crossed when $V_{IN}$ dips



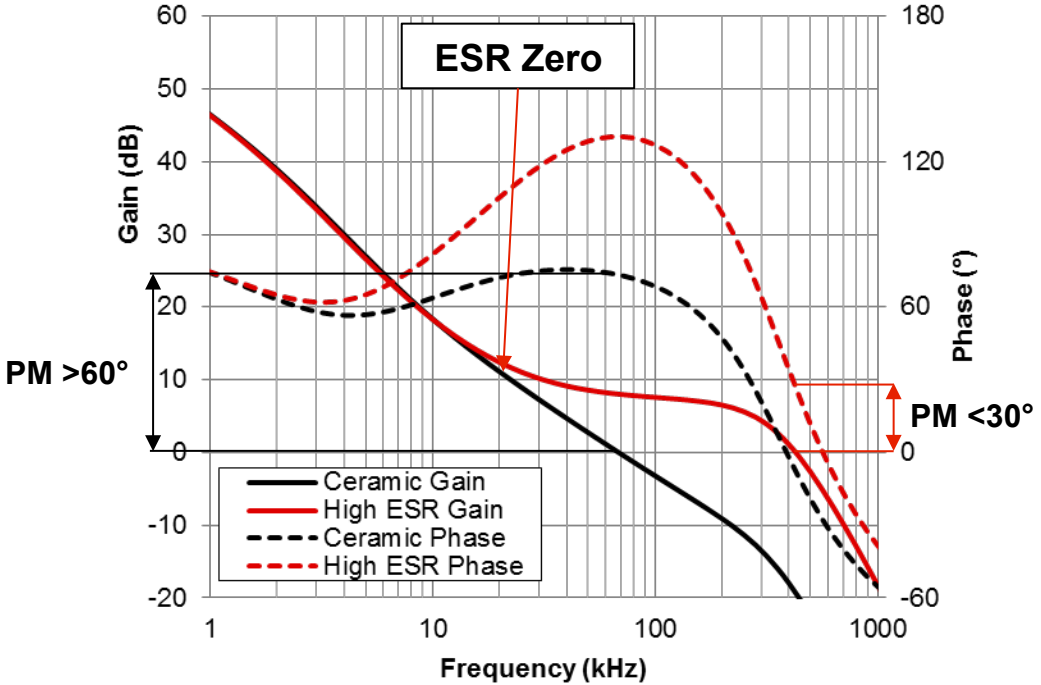




9 V input, 8 A load step-up

**With bulk decoupling input capacitance**

# 4) Input/Output Capacitor Guidelines

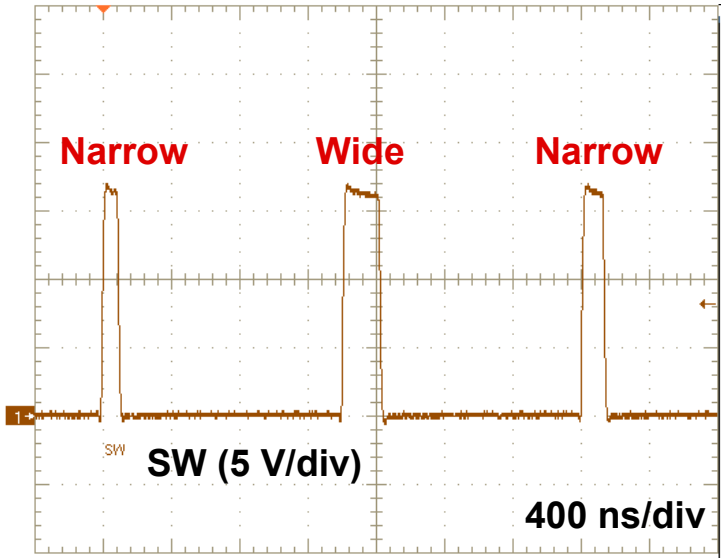
- Ensure sufficient decoupling capacitance
- Don’t replace a low ESR cap with a “cheap” high ESR cap
  - Can cause instability!
  - ESR increases by factor 4 to 15 at -40 °C!
- Select output capacitance with load transient requirements accounted for
- Check RMS current rating



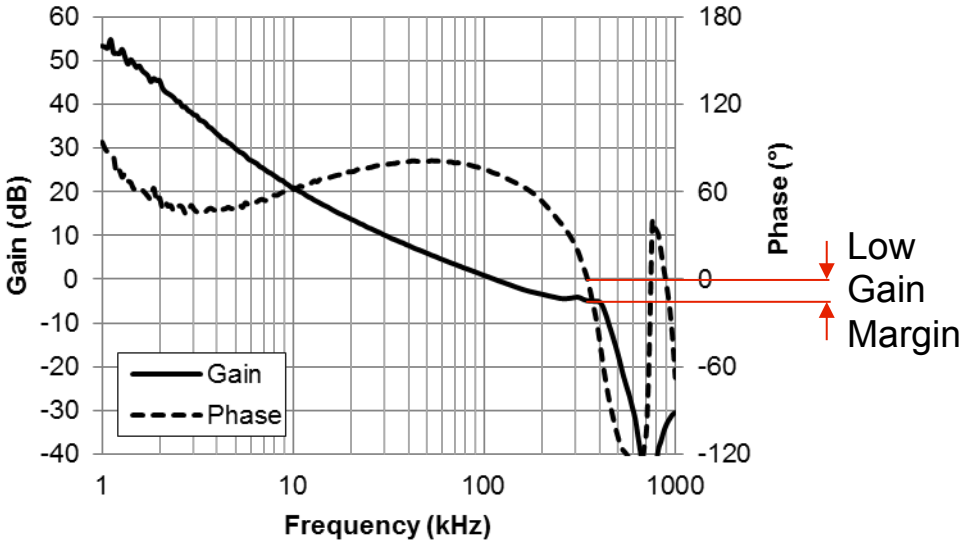

**Different compensation is needed!**

# 5A) What Caused Wide/Narrow SW Node Pulses?

$V_{IN}$ = 17 V, $V_{OUT}$ = 1.8 V, D = 11%



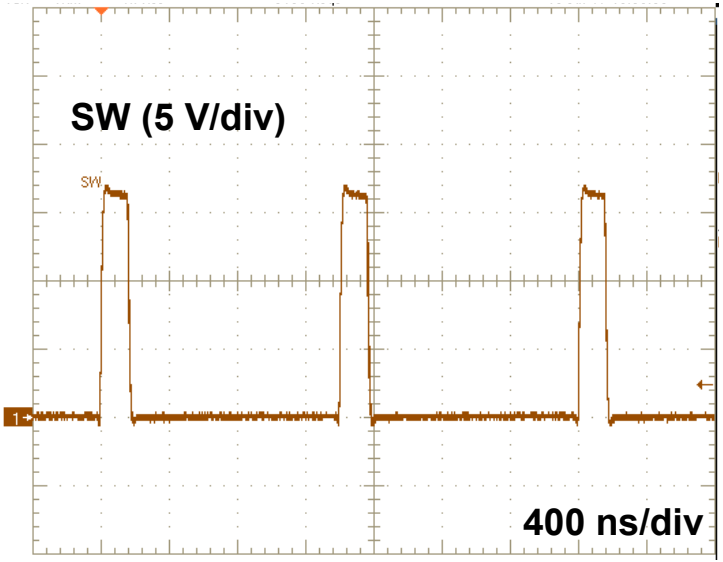

**Poorly compensated design**



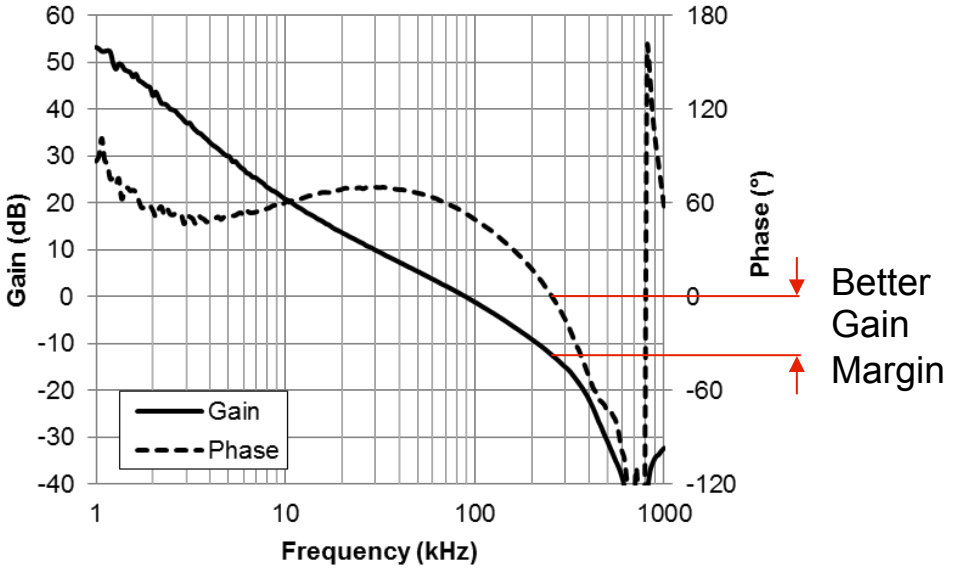

**Low gain margin! <5 dB!**
(Gain when phase crosses 0)

# 5A) Design for More Gain Margin

SW Node Is Stable

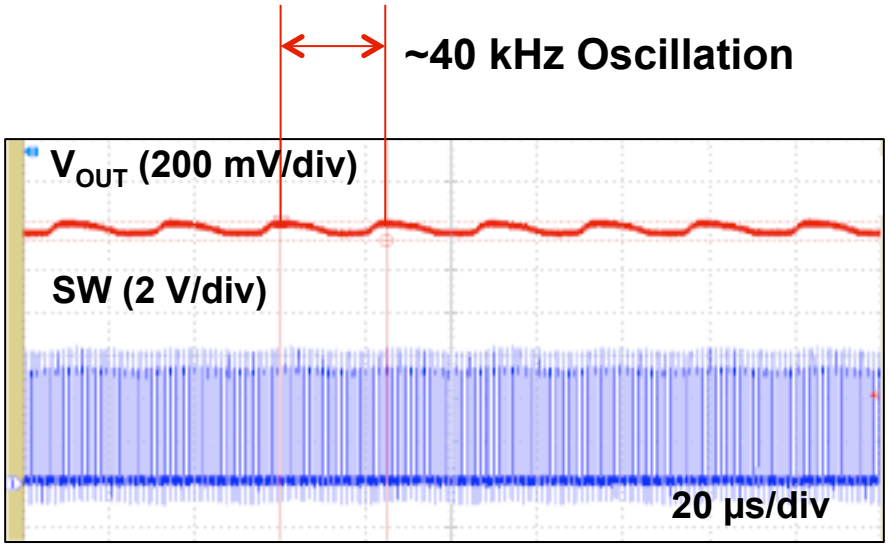



**13 dB** Gain Margin



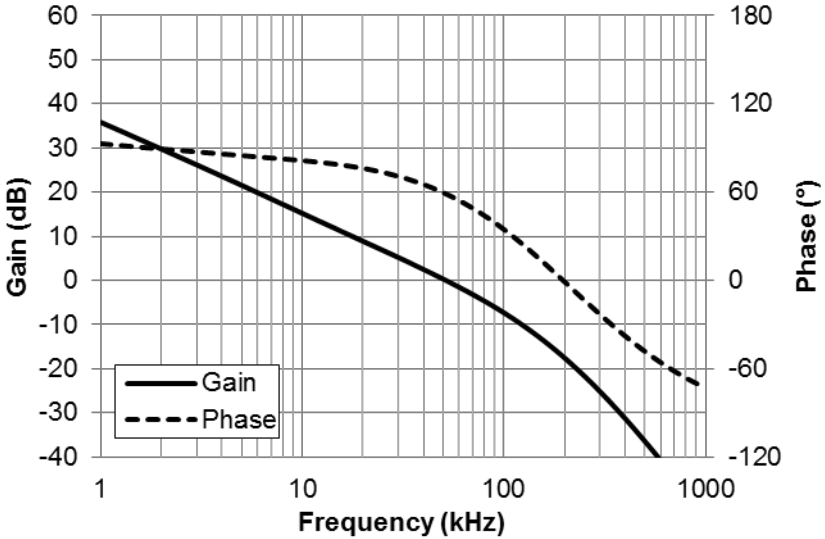

Design rule of thumb: **>10 dB** gain margin
(across ALL operating conditions)

# 5B) Why Is the Output Oscillating?



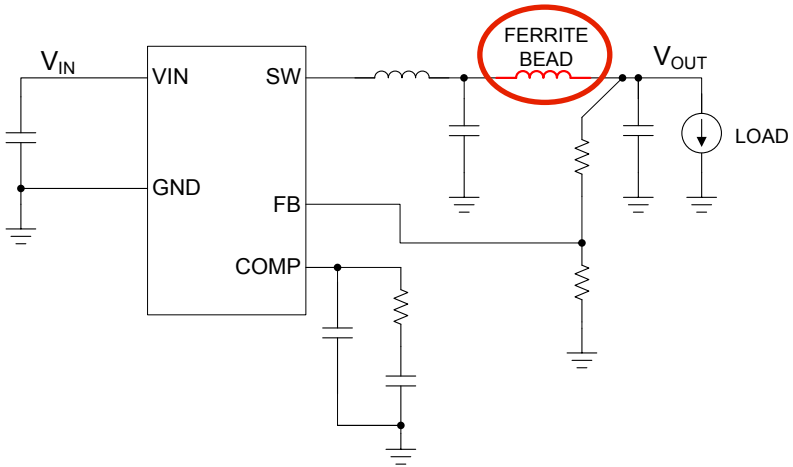

Design is stable on an EVM but output oscillates in real application

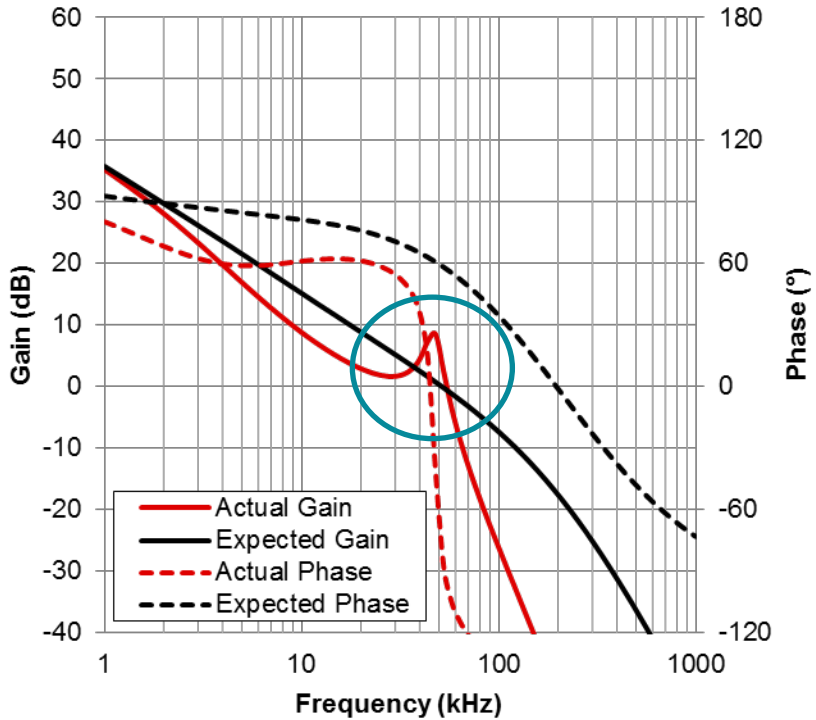
**Phase Margin: 60°**
**Gain Margin: 16.7 dB**




Simulation shows sufficient phase margin and gain margin

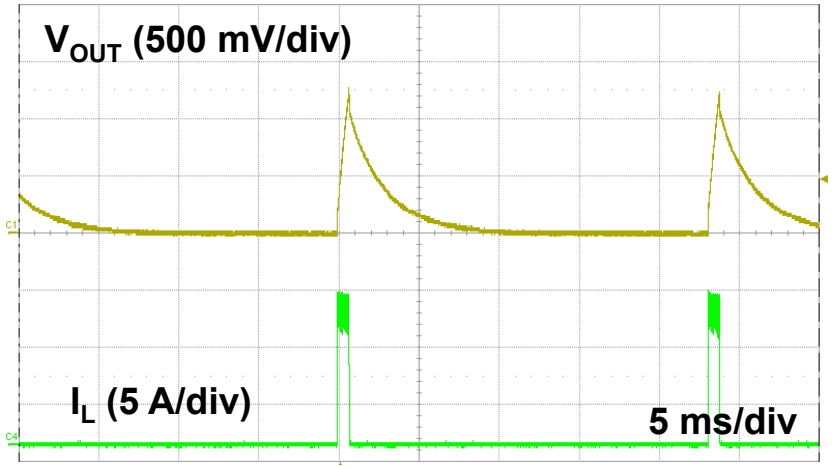
# 5B) Compensate for System Level Output Filter




- **Second stage LC filter** not included in original design and causes instability!
  - Resonance frequency is ~40 kHz
  - Same frequency as oscillation
- Design compensation for the actual output filter

# 6) Why Doesn’t the Converter Start Up?




A very **large output capacitance** is causing the converter to hit its **overcurrent limit** during startup. The hiccup auto-restart process continues indefinitely.

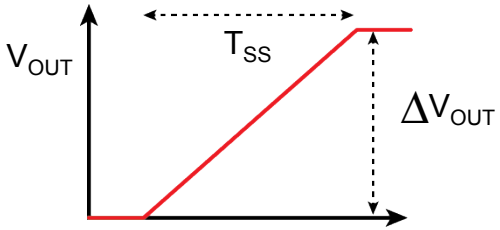
# 6) Pick an Appropriate Soft Start Time

- Avoid input voltage sag due to inrush current
- Estimate converter input and output current

$$I_C = C\frac{\Delta V}{\Delta T}$$

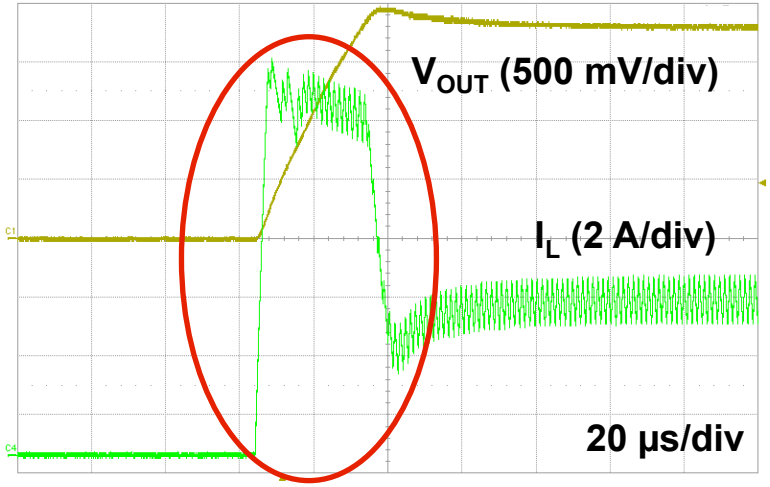
$$I_L = I_{LOAD} + I_C$$

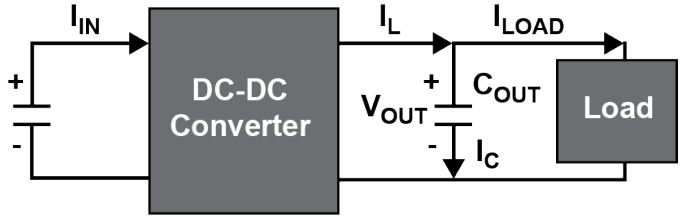
$$I_{IN} \approx D(I_{LOAD} + I_C)$$



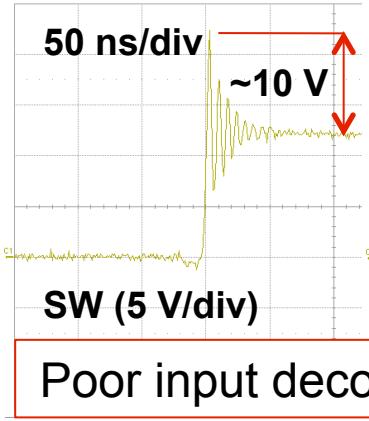

- Avoid overcurrent protection limit
- **Sequence** startup of supply rails

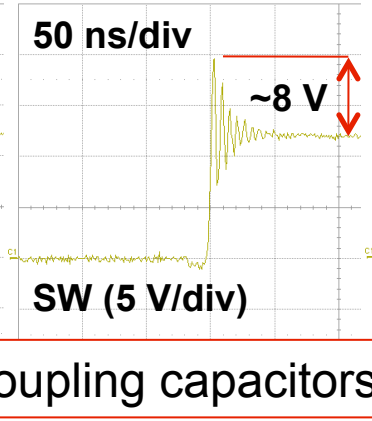
Current surge: startup time is too short

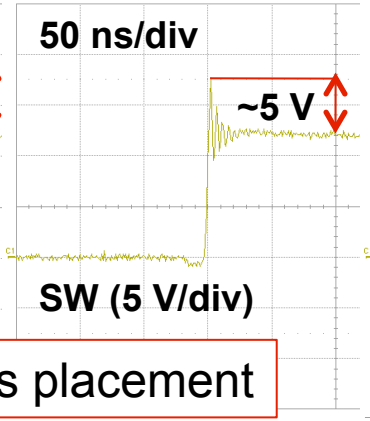


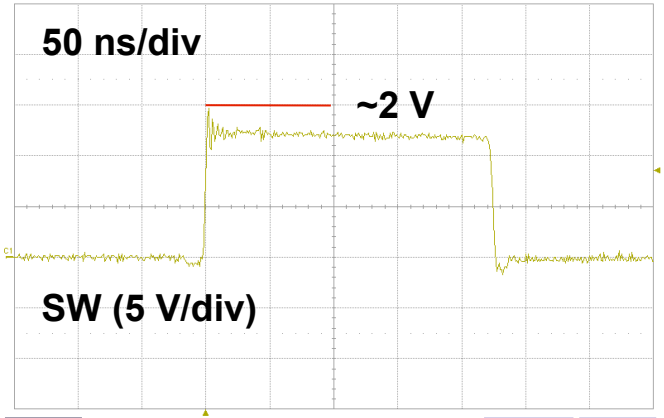



# 7) Why Is There Large SW Node Ringing?



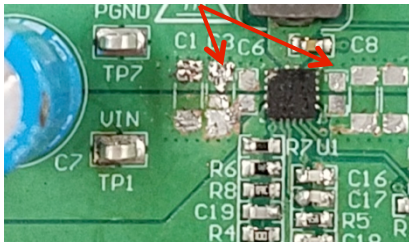



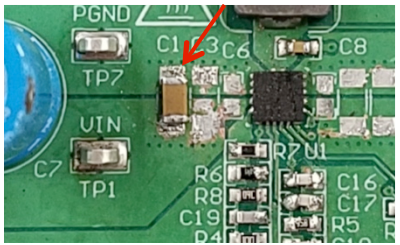




Poor input decoupling capacitors placement

**No nearby input caps**

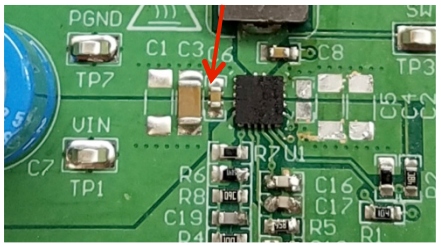



**One far input cap**



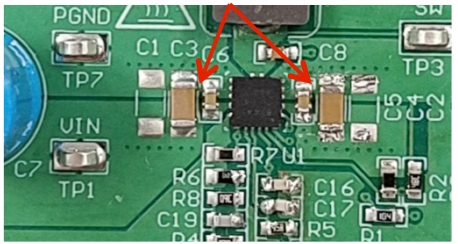

10 µF, 1206

**Two close caps**




10 µF, 1206
0.1 µF, 0603

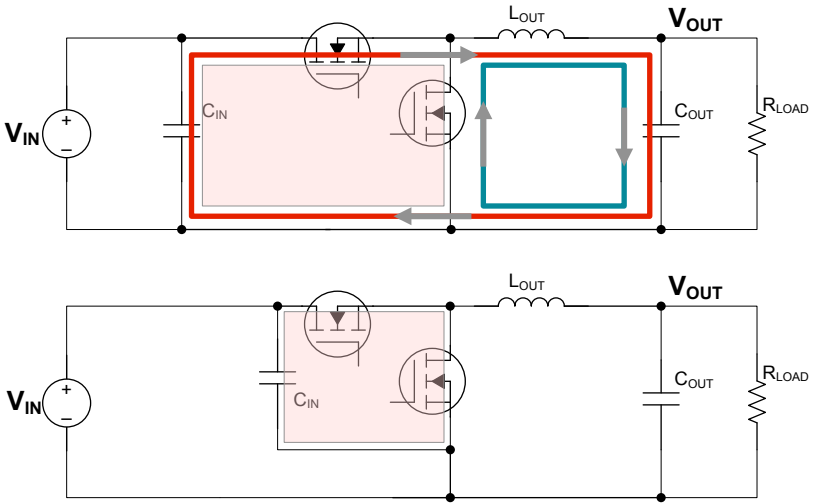
**Two-sided, close caps**




2 x 10 µF, 1206
2 x 0.1 µF, 0603

# 7) Understand Layout Parasitics

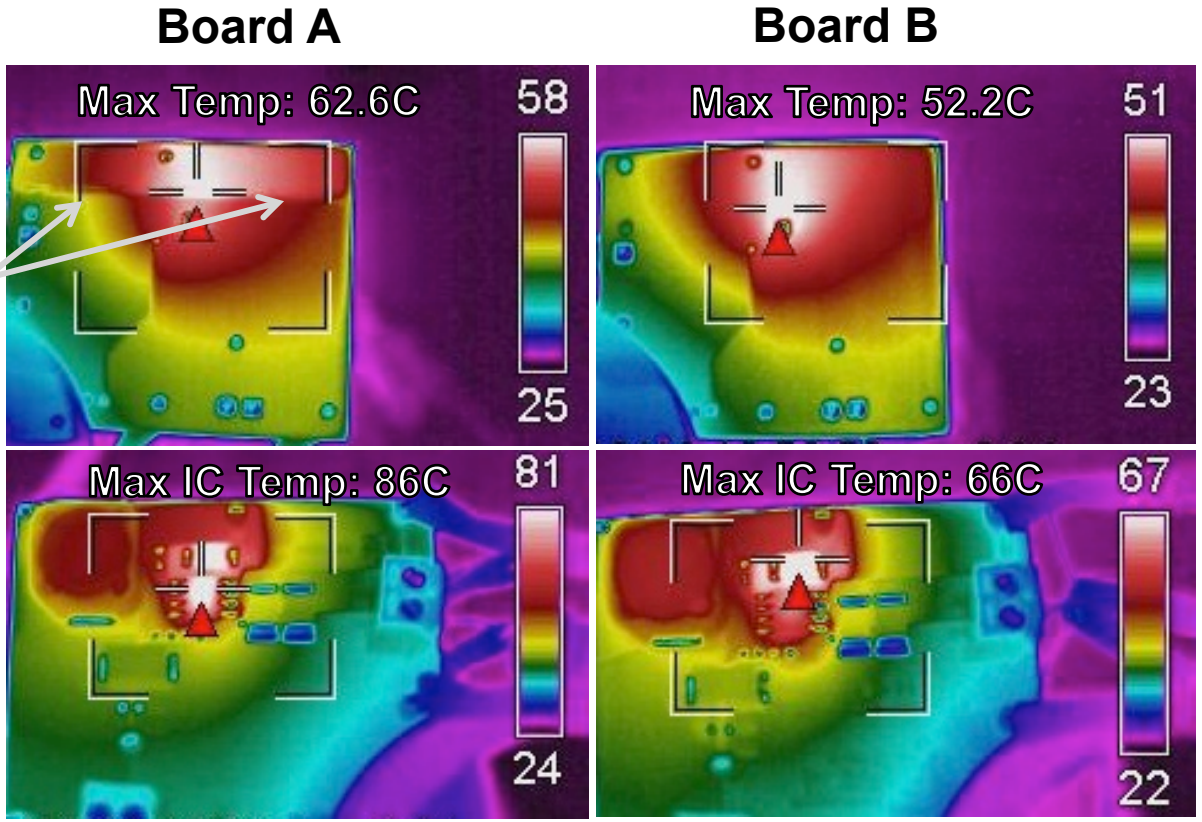
- Minimize loop area and keep components close
- Optimize grounding/return paths
- Avoid large SW node → EMI
- Keep noise sensitive analog pins/ traces (e.g. FB, COMP) **away from** noisy power pins/traces (e.g. SW, BOOT)
- Can add a snubber or a boot resistor to control/slow down SW node slew rate



# 8) Why Is Board A 10°C Hotter Than B?

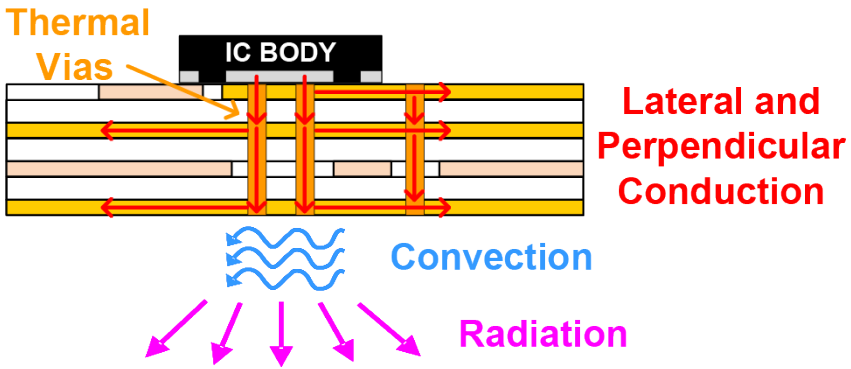
**Traces cutting through the ground plane**

- Traces on the bottom layer **prevent heat from spreading** effectively
- **Removing horizontal trace** for a more solid bottom layer reduces IC temp on Board B
- Hottest component on B is the catch diode



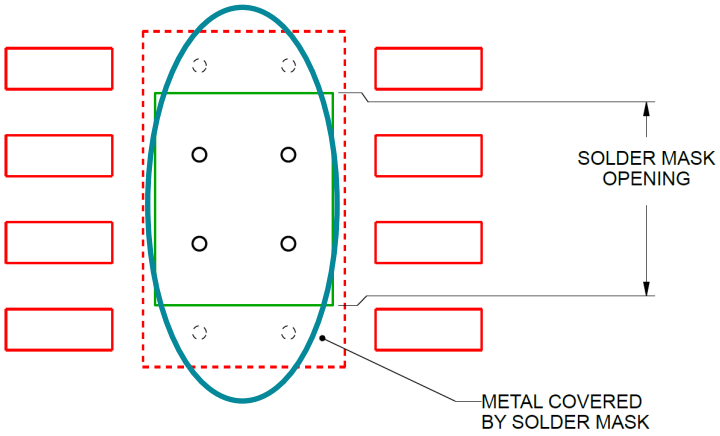
# 8) Layout PCB Considering Thermals

- Have **solid ground planes** to better spread heat across the layer
- Use **thermal vias** to spread heat to other layers



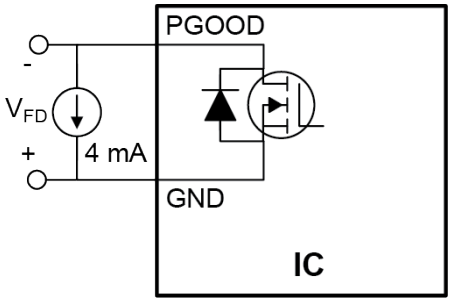

- **Thermal pads** help to get the heat out of the IC into the PCB

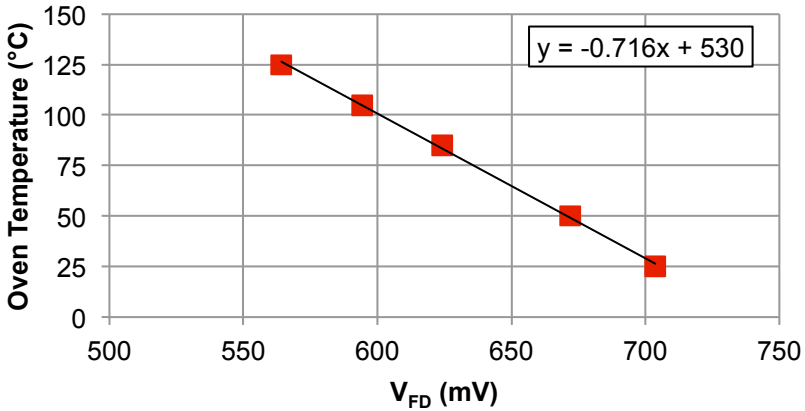
**Footprint with Thermal Via Pattern**



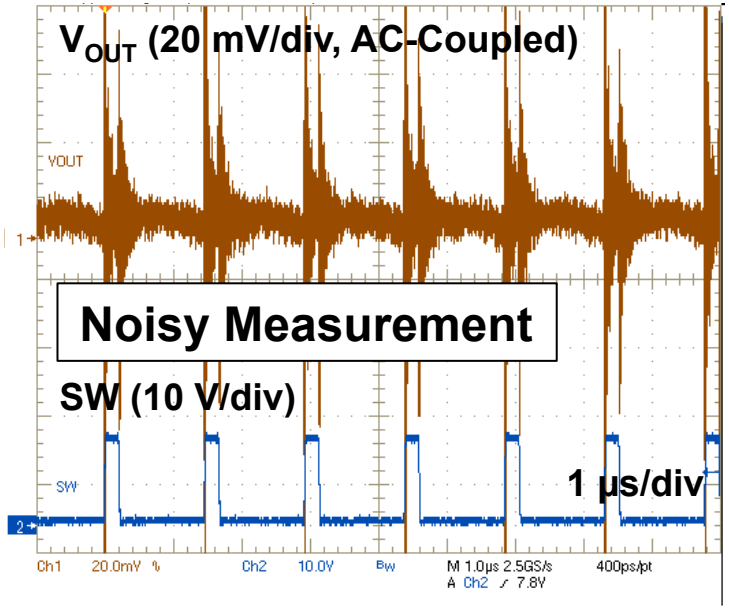
# 8) In Situ Junction Temperature Measurement

- Common question: How much thermal margin is there in my design?
- Difficult to accurately measure IC junction temp in operation
- One option: Use the **internal diode on PGOOD** or similar pin
  - First **characterize** diode voltage versus temperature
  - Measure diode voltage in operation
  - View app note slva397 for more details

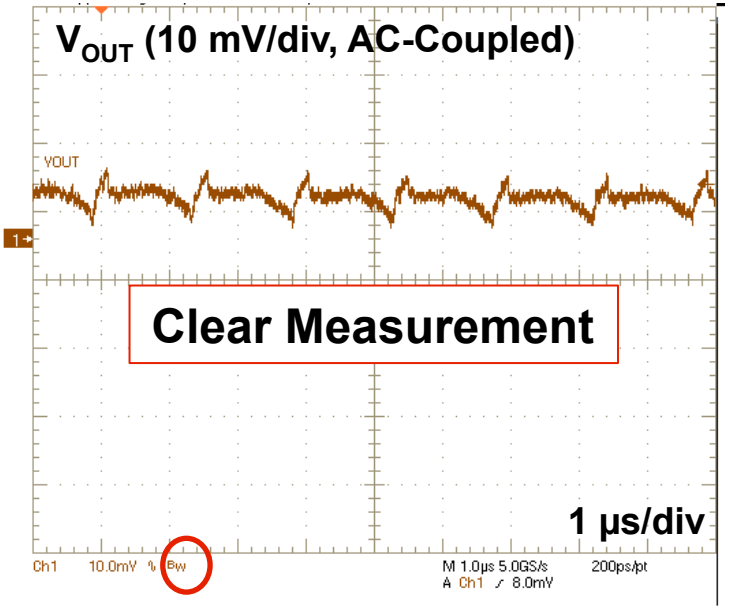


# 9) Which Output Measurement Is Right?




- Switching noise picked up from channel 2
- No bandwidth limiting



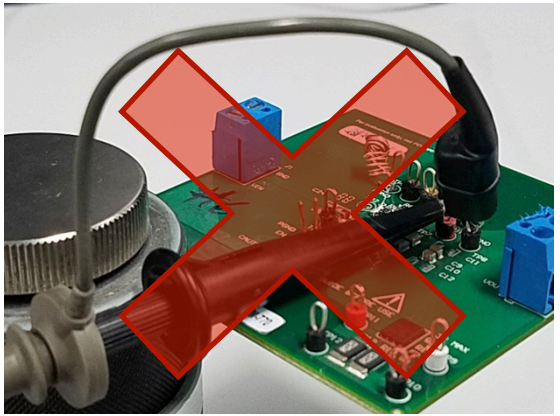

- 20 MHz bandwidth limiting
- Switch node probe removed

# 9) Correct Measurement Techniques

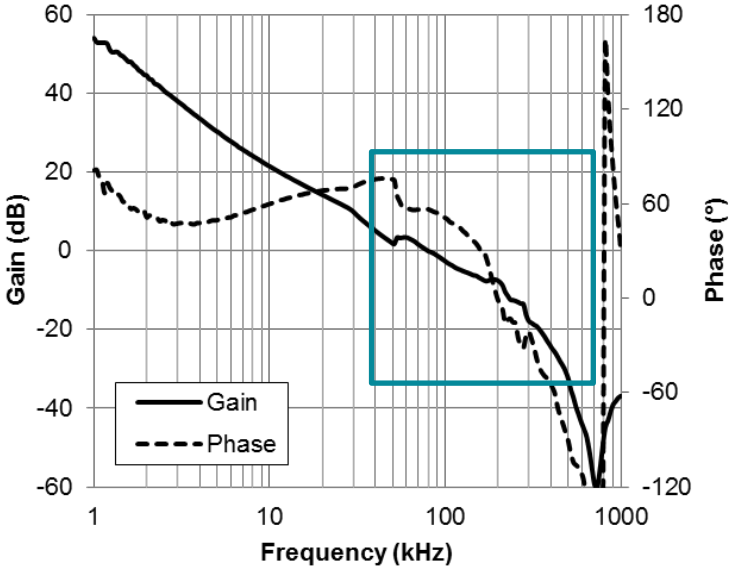
- Measure right across the output capacitor
  - Use a “tip and barrel” approach
  - Probe sockets for prototypes
  - Don’t have a flying ground lead
- Limit the bandwidth 20 MHz
- Use scope full Y-axis scale
- Consider 1:1 probes or active probes

**“Tip and Barrel”**

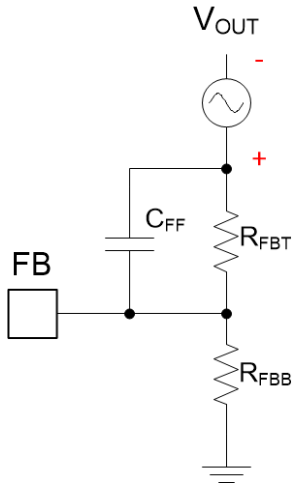

**Flying Ground Lead**

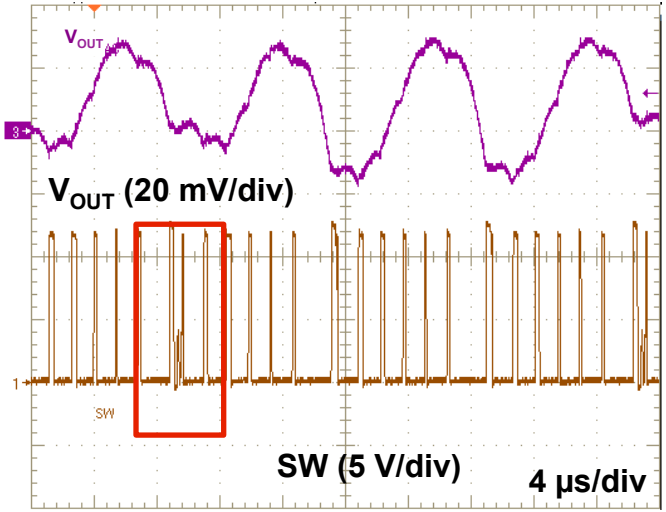


# 10A) Why Is the Bode Plot Not Smooth?



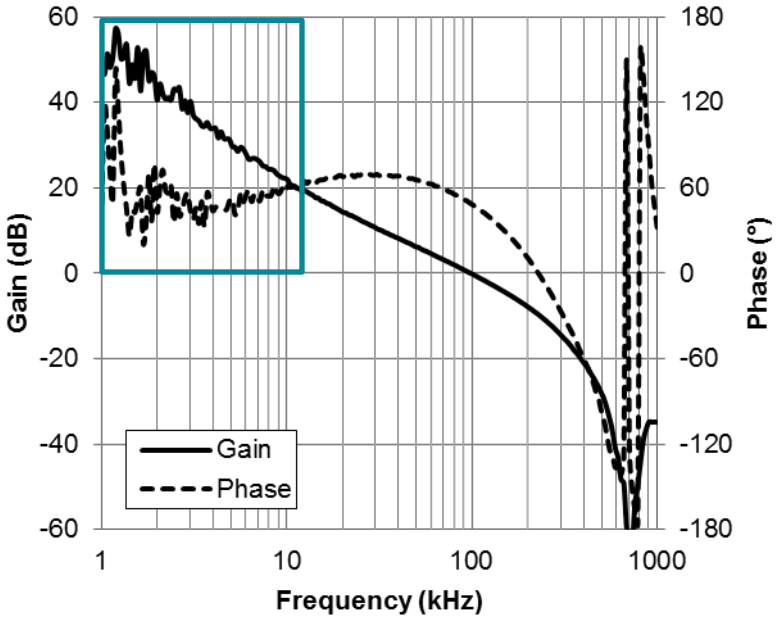

Large injected signal results in pulse-skipping at SW




**Signal injection too large**

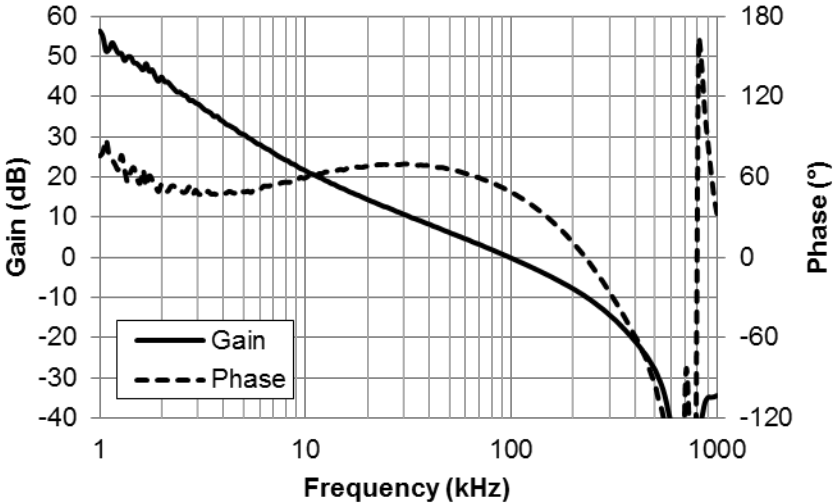
# 10B) Why Is the Bode Plot Not Smooth?



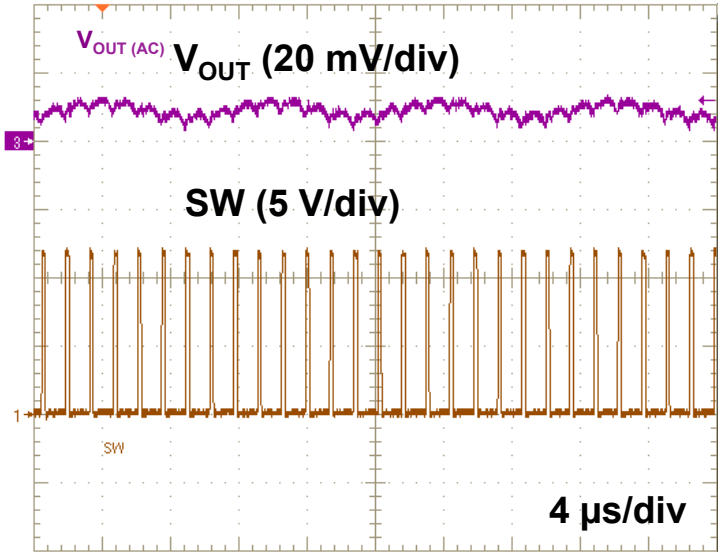

- **Signal-to-noise ratio** is too low to make an accurate measurement
- At low frequencies, gain of loop **attenuates** injected signal
- Increasing **integration time** or using lower frequency IF bandwidth helps to filter noise

**Signal injection too small**

# 10) Optimal Small Signal Injection




- Too large → glitches at higher frequency
- Too small → inaccurate measurement
- Shape injected signal amplitude vs frequency




Good measurement: visible oscillation on $V_{OUT}$ and SW waveform is stable

# Summary

- Reviewed **common mistakes** in point of load DC/DC converters
  - Minimum on-time limitation and converter ratings
  - Inductor and capacitor selection
  - Compensation and startup
  - Converter PCB layout to minimize parasitics and improve thermal dissipation
  - Output voltage and bode plot measurement techniques
- Explained why these mistakes occur and **how to avoid them**
- Use this presentation as a reference when debugging and working on new designs

# References

- Switch-mode power converter compensation made easy
  https://www.ti.com/seclit/ml/slup340/slup340.pdf
- Power Tips: Designing a two-stage LC filter
  https://e2e.ti.com/blogs_/b/powerhouse/archive/2015/02/24/power-tips-designing-a-two-stage-lc-filter
- Junction temperature measurement
  http://www.ti.com/lit/an/slva397/slva397.pdf
- Parts used in presentation
  - http://www.ti.com/product/TPS54824
  - http://www.ti.com/product/TPS54a20
  - http://www.ti.com/product/TPS54821

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