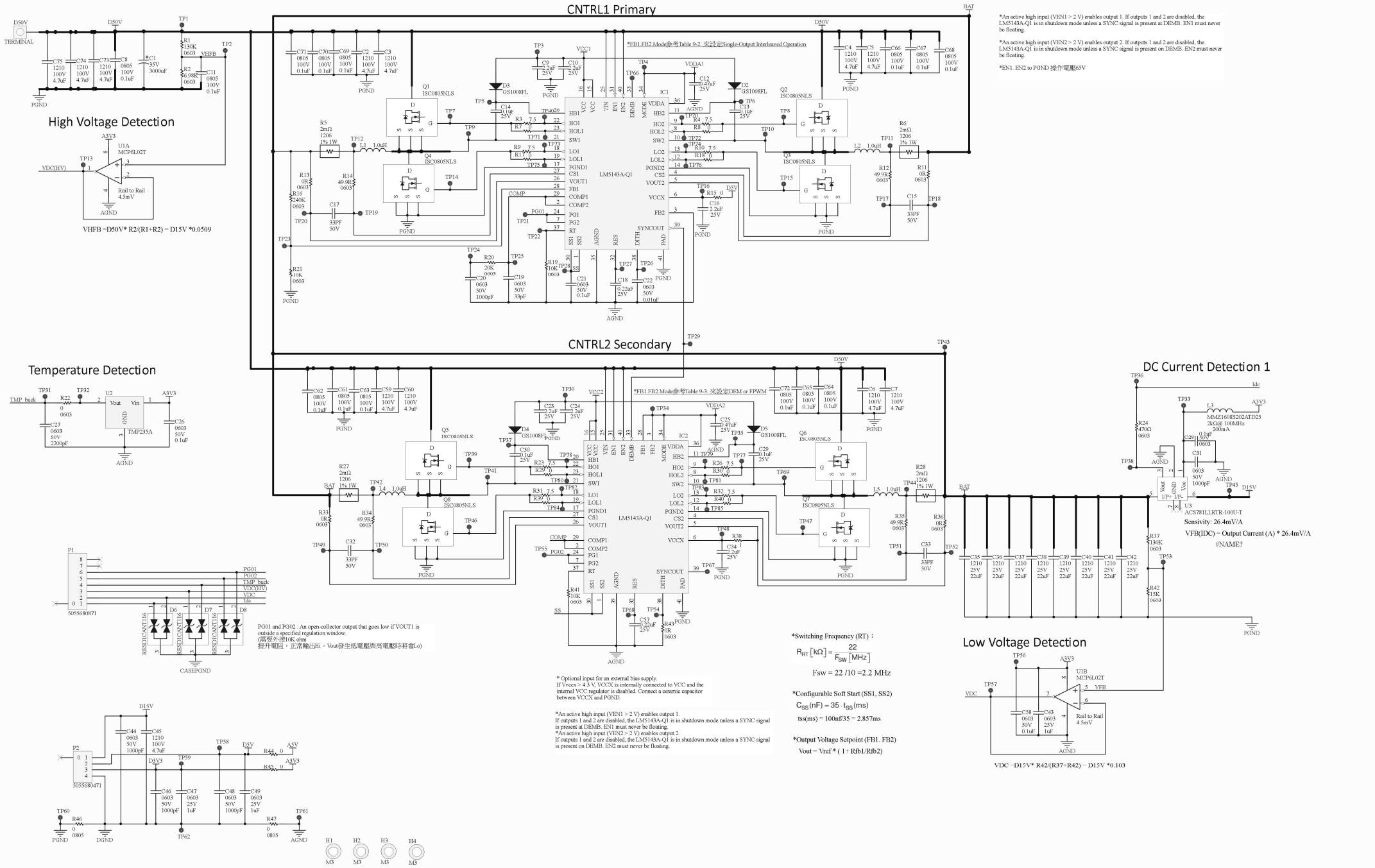
CNTRL1 Primary
CNTRL2 Secondary
High Voltage Detection
Temperature Detection
DC Current Detection 1
Low Voltage Detection
LM5143A-Q1
VHFB =D50V* R2/(R1+R2) − D15V *0.0509
*FB1.FB2.Mode參考Table 9-2. 求設定Single-Output Interleaved Operation
*FB1.FB2.Mode參考Table 9-3. 求設定DEM or FPWM
*An active high input (VEN1 > 2 V) enables output 1. If outputs 1 and 2 are disabled, the LM5143A-Q1 is in shutdown mode unless a SYNC signal is present at DEMB. EN1 must never be floating.
*An active high input (VEN2 > 2 V) enables output 2. If outputs 1 and 2 are disabled, the LM5143A-Q1 is in shutdown mode unless a SYNC signal is present on DEMB. EN2 must never be floating.
*EN1. EN2 to PGND 操作電壓65V
PG01 and PG02 : An open-collector output that goes low if VOUT1 is outside a specified regulation window.
(當要外接10K ohm
提升電阻，正常輸出Hi，Vout發生低電壓與高電壓時將會Lo)
* Optional input for an external bias supply.
If Vvccx > 4.3 V, VCCX is internally connected to VCC and the internal VCC regulator is disabled. Connect a ceramic capacitor between VCCX and PGND.
*An active high input (VEN1 > 2 V) enables output 1.
If outputs 1 and 2 are disabled, the LM5143A-Q1 is in shutdown mode unless a SYNC signal is present at DEMB. EN1 must never be floating.
*An active high input (VEN2 > 2 V) enables output 2.
If outputs 1 and 2 are disabled, the LM5143A-Q1 is in shutdown mode unless a SYNC signal is present on DEMB. EN2 must never be floating.
*Switching Frequency (RT) :
$R_{RT}[k\Omega] = \frac{22}{F_{SW}[MHz]}$
Fsw = 22 /10 =2.2 MHz
*Configurable Soft Start (SS1, SS2)
$C_{SS}(nF) = 35 \cdot t_{SS}(ms)$
tss(ms) = 100nf/35 = 2.857ms
*Output Voltage Setpoint (FB1. FB2)
Vout = Vref * (1+ Rfb1/Rfb2)
Sensivity: 26.4mV/A
VFB(IDC) = Output Current (A) * 26.4mV/A
#NAME?
VDC −D15V* R42/(R37+R42) − D15V *0.103
*Please refer to the Layout Guide in SNVSCC1,page 54.
Title
Size
A2
Number
Revision
Date: 2025/8/20
Sheet of
File: D:\研究\..\1. BUCK Converter_R01.SchDoc
Drawn By: