TPS65218xx Silicon Revision History

#	Name	Description	Issue Occurrence	System Impact	Status			
					-B1	-D0	Conditions of occurrence	Workaround with -B1 silicon
1	DCDC4 startup issue (Cold Temp, High VIN)	Depending on the temperature, VIN voltage, output capacitance, and the quality of the layout, DCDC4 could have issues starting up	High	High	Present	Fixed	1) VIN > 4.8V, worsens with higher voltage 2) TEMP < 25C, worsens with lower temperature 3) Worsen with poor layout 4) COUT > 80uF, worsens with larger COUT	**Recommended workaround:** 1) Place schottky diode from GND to L4A 2) Place at minimum 25 vias on the power pad 3) Place DCDC4 output capacitor on the same PCB layer as PMIC
2	DCDC4 startup issue (Hot Temp, Low VIN)	DCDC4 is unable to start at low VIN due to insufficient current sensor sampling time	Low	High	Present (Documented in datasheet)	Fixed	1) TEMP > 55C, worsens with lower temperature	Behavior is documented in the -B1 datasheet: Input voltage soft-start range - VIN_DCDC4 > 3.4V from -40C to 55C - VIN_DCDC4 > 3.8V from -40C to 105C
3	DCDC4 instability (Cold Temp, High VIN, High Load)	At high load and high VIN, DCDC4 is unstable, particularly worse at cold temp	None	High	Present (Documented in datasheet)	Fixed	1) VIN > 4.5V, worsens with higher voltage 2) TEMP < 25C, worsens with lower temperature 3) Worsens with poor layout 4) Is worse on the EVM then validation board	**Recommended workaround:** 1) Place schottky diode from GND to L4A 2) Place at minimum 25 vias on the power pad 3) Place DCDC4 output capacitor on the same PCB layer as PMIC
4	DCDC4 instability (Hot Temp, Low VIN, High Load)	DCDC4 oscillates when a load transient of 300mA or more is applied near the current limit in boost mode; this behavior occurs at low VIN and high temperature	None	High	Present (Documented in datasheet)	Fixed	1) VIN < 3.3V, worsens with lower voltage 2) VOUT > 1.8V, worsens with higher output voltage 3) TEMP > 85C, worsens with higher temp 4) COUT < 100uF, worsens with lower COUT 5) > 300mA transient step (700mA --> 1000mA) Worsens with a larger transient step near current limit	**Reccomended workaround:** 1) Increase the output capacitance on DCDC4
5	DCDC4 increased output ripple (Cold Temp, High VIN, High Load)	DCDC4 will have large ripple when the device is transitioning from PFM mode to PWM mode when the device is configured in Auto PFM mode (i.e. Power saving mode)	Low	Low	Present (Documented in datasheet)	Fixed	1) VIN > 4.5V, worsens with higher voltage 2) TEMP < 25C, worsens with lower temperature 3) 300mA < LOAD < 500mA 4) Worsens with lower COUT 5) More prevalent on the EVM	**Recommended workaround:** 1) Place DCDC4 into forced PWM mode
6	DCDC5/6 Voltage Droop	When FSEAL=1 and there is a slow voltage decay on IN_BIAS when the main supply is lost, the internal EEPROM may be latched to the incorrect values causing the bandgap voltage for DCDC5/6 to have the incorrect value which in turn causes DCDC5/6 to regulate low on when on coincell	High	Low	Present (Documented in datasheet)	Fixed	1) FSEAL = 1 and CC voltage present 2) IN_BIAS slew rate < 150V/s	Behavior is documented in the -B1 datasheet: Documented in DC accuracy spec for DCDC5 - DC accuracy +/-1.5% when IN_BIAS decaying slew rate > 150V/s - DC accuracy +5/-10% when IN_BIAS decaying slew rate < 150V/s Documented in DC accuracy spec for DCDC6 - DC accuracy +/-1.5% when IN_BIAS decaying slew rate > 150V/s - DC accuracy +/-5% when IN_BIAS decaying slew rate < 150V/s **Recommended workaround:** - Ensure the IN_BIAS decay > 150V/s from 2.5V --> 1.8V - Place a PFET and resistor combination to decay the slew rate faster than 150V/s - use the PGOOD signal of the pre-reg/charger No workaround required for -B1 silicon in systems with a 1S battery.
7	I2C minimum 40% duty cycle (f_{SCL} = 400kHz)	There is an duty cycle limitation for the I2C communication of TPS65218 when in 400kHz mode. The duty cycle must be greater than 40% to operate correctly in 400kHz mode	Low	High	Present (Documented in datasheet)	Present (Documented in datasheet)	1) In 400kHz when the ON duty cycle < 40%	**Recommended workaround:** - Operate I2C in 100kHz mode or ensure 400kHz mode is above 40% duty cycle Behavior documented in the -B1 and -D0 datasheets: 1) Spec'ed in the datasheet the "> 40%" requirement for ON time
8	LS3 1A ILIM (VIN_LS3 = 1.8V)	For LS3, when the VIN Voltage is 1.8V, the current limit is out of spec	None	Low	Present (Documented in datasheet)	Present (Documented in datasheet)	1) VIN < 2.3V, worsens with lower VIN voltage 2) Current limit setting [0x3h] 3) Worsens with higher temperature	Behavior documented in the -B1 and -D0 datasheets: - 900mA is the lower limit for the current limit setting [0x3h] - the other current limit settings have been modified as well to account for current limit variation
9	DCDC5/6 Overshoot/Inrush (at startup)	When TPS65218 starts up at high VIN, DCDC5 and DCDC6 will overshoot above their regulation targest (~200mV overshoot at worst case)	None	Low	Present (Documented in datasheet)	**Fixed**	1) VIN > 4.5V 2) COUT < 20uF 3) occurs the across the entire temperature range, worsens with lower temperature	**Recommended workaround:** - Add more capacitance to the output of DCDC5/6, add 47uF
10	DCDC5 Does Not Regulate (High Temp, Low Load Leakage)	DCDC5 erroneously switches due to leakage inside the device, at low output loads the output load is not larger enough to counteract the internal leakage in the device and DCDC5 will float up due to the errooneous switching.	Low	Low	Present (Documented in datasheet)	**Fixed**	1) Entire VIN range, worsens with lower voltage (CC or IN_BU) 2) Occurs on all material, worsens with HL skew material (strong NMOS / weak PMOS) 3) TEMP > 65C, worsens with higher temperature 4) worsens with smaller output loads	Behavior documented in the -B1 datasheet: - split up the spec based on temperature and load levels for those temps - see B1 datasheet online for the specification
11	IN_BIAS UVLO Hysteresis slew rate	TPS65218 will start up at V_UVLO (incorrect) or V_UVLO + V_HYST (correct) depending on the rising IN_BIAS slew rate	Low	Low	Present (Documented in datasheet)	**Fixed**	1) IN_BIAS slew rate > 30V/s from IN_BIAS=2.5V --> 2.75V	Behavior documented in the -B1 datasheet: IN_BIAS slew rate requirement is documented in the datasheet, see the spec to the right and in the B1 datasheet online
12	No deglitch filters present on I2C pins	No deglitch filter is present on SDA or SCL, there should be some deglitch according to the designers	None	Low	Present	**Fixed**	1) If an erroneous glitch occurs	Fix has been implemented in -D0 and is working correctly. *Not documented in the -B1 datasheet:
13	LDO1 instability (Cold Temp, High Load)	At high load and low temperature LDO1 oscillates at low COUT	None	Medium	Present (Documented in datasheet)	Present (Documented in datasheet)	1) TEMP < -20C, worsens with lower temperature 2) effective COUT capacitance < 10uF	Requirement has been updated in the -B1 and -D0 datasheets: Increase the output effective output capacitance to 10uF or greater across the entire temperature range
14	INT_LDO hold time (Cold Temp)	At -40C, the hold up time specification is able to be sastified	None	Low	Present (Documented in datasheet)	Present (Documented in datasheet)	1) At low C_INT_LDO < 1uF, 2) C_IN_BIAS <= 4.7uF 3) -40C temperature	Behavior documented in the -B1 and -D0 datasheets (update to test conditions in the specification): - IN_BIAS is tied to IN_DCDC1-4, IN_LDO1 - decay rate modification.. IN_BIAS decay rate > 5us