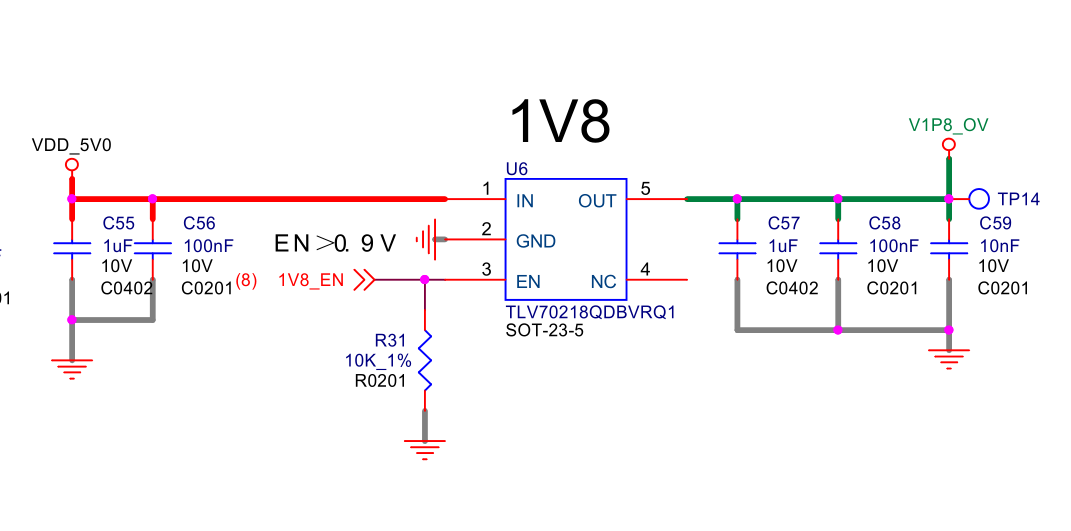
**JLR requirements**:

Control loops (e.g. Op-Amp circuits, power regulators) shall be designed with a minimum phase margin of 45 degrees and a minimum gain margin of 10 dB. Where electrolytic capacitors are used the minimum phase margin shall be increased to 60 degrees.

**Our design**

1、

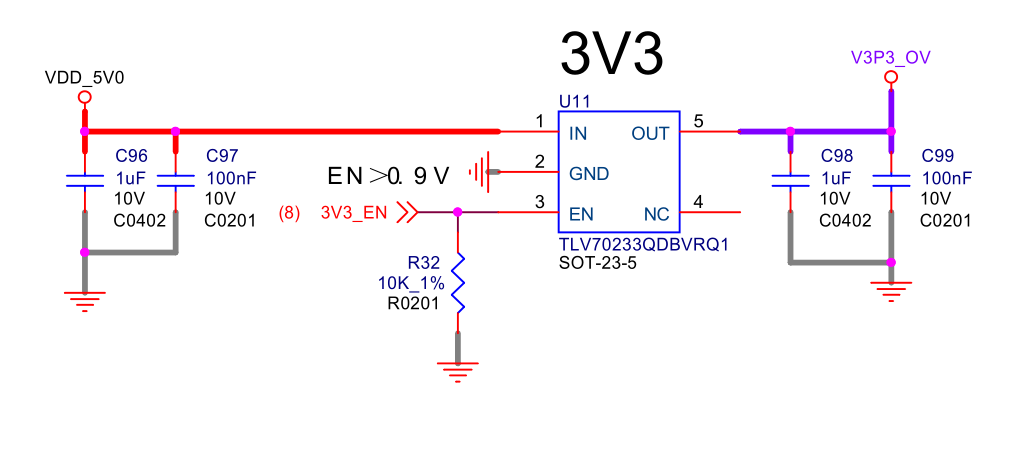


|  |  |  |
| --- | --- | --- |
| ①Requirements：max load | | |
| item | Value | Unit |
| VIN | 4.9-5.1 | V |
| VOUT | 1.8 | V |
| VOUT1 Ripple | ±150 | mV |
| IOUT | 180 | mA |

Cin：1uF/10V+100nF/10V

Cout：1uF/10V+100nF/10V+10Nf/10V

2、



|  |  |  |
| --- | --- | --- |
| ①Requirements：max load | | |
| item | Value | Unit |
| VIN | 4.9-5.1 | V |
| VOUT | 3.3 | V |
| VOUT1 Ripple | ±300 | mV |
| IOUT | 60 | mA |

Cin：1uF/10V+100nF/10V

Cout：1uF/10V+100nF/10V