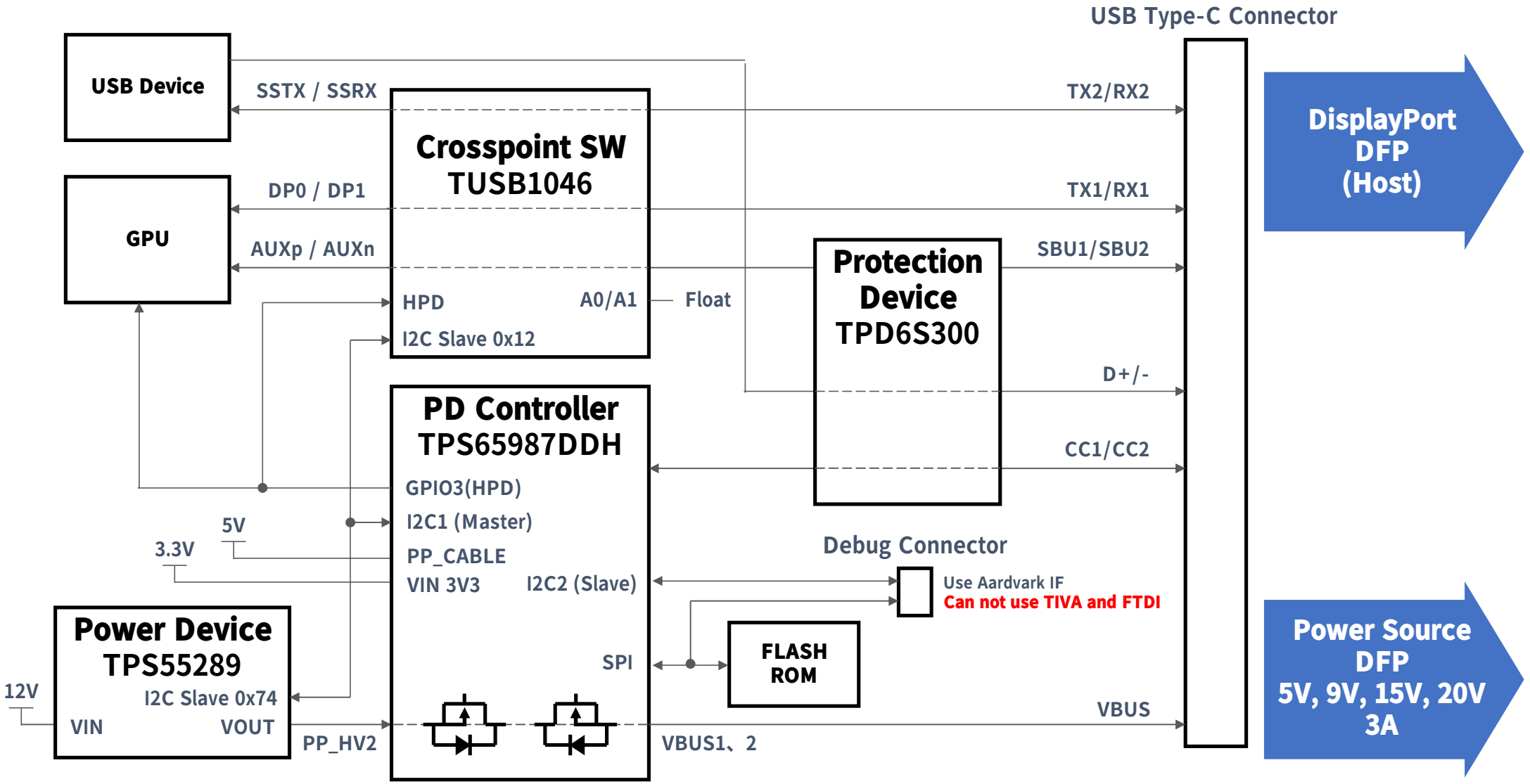
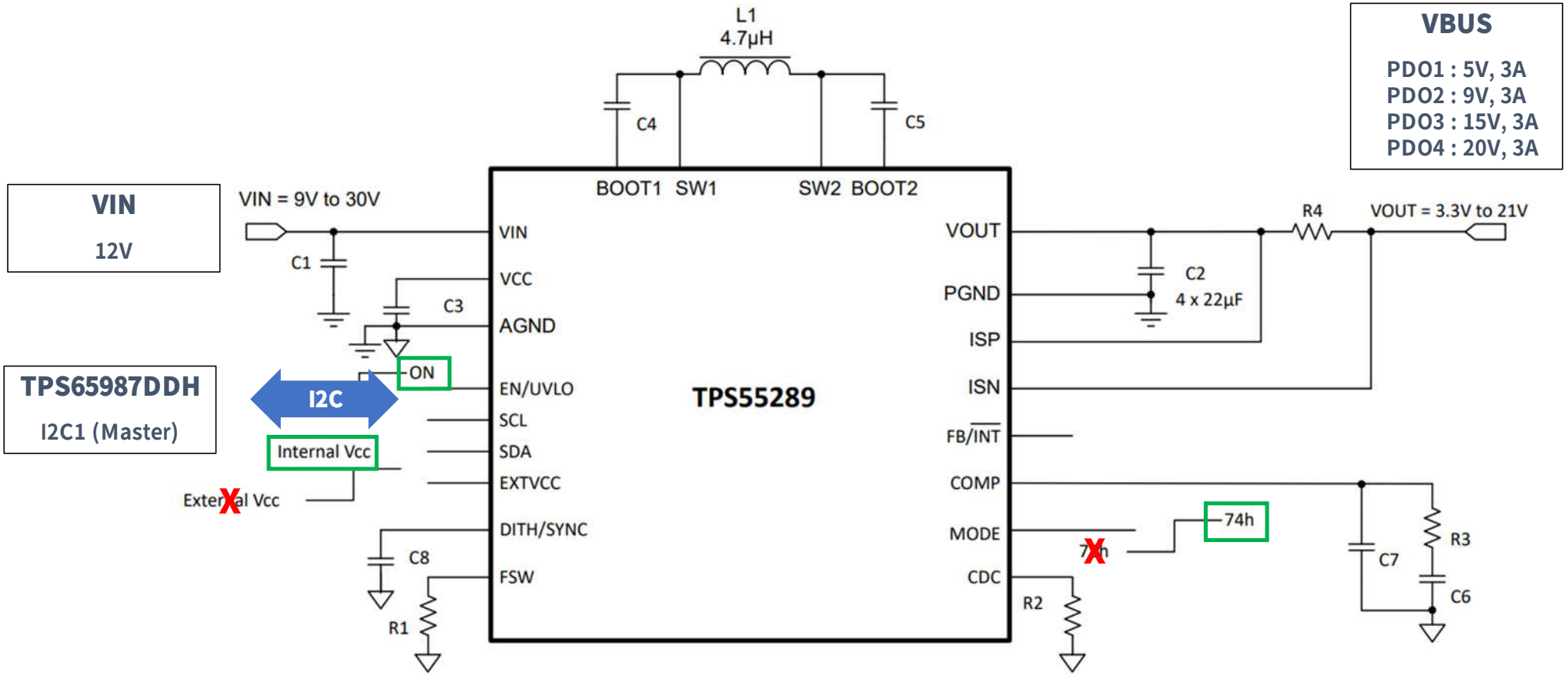
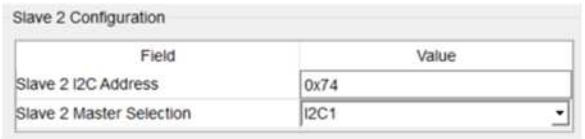
Block Diagram



TPS55289 circuit



< I2C Master Configuration (0x64) of TPS65987DDH >



TPS55289 Register settings – POR

1. VREF 7.6.1 REF Register (Address = 0h, 1h)

Figure 7-15. REF_LSB

7	6	5	4	3	2	1	0
VREF							

Figure 7-16. REF_MSB

15	14	13	12	11	10	9	8
Reserved					VREF		

Table 7-4. REF Register Field Descriptions

Bit	Field	Type	Reset	Description
15-11	Reserved	R/W	000000b	Reserved
10-0	VREF	R/W	001 10100100b	Sets the internal reference voltage 000 00000000b = 45-mV reference voltage 000 00000001b = 45.5645-mV reference voltage 000 00000010b = 46.129-mV reference voltage ..... = ... 001 10100100b = 282-mV reference voltage ..... = ... 011 00110100b = 508-mV reference voltage ..... = ... 101 10001100b = 846-mV reference voltage ..... = ... 111 10000000b = 1129-mV reference voltage ..... = ... 111 11111110b = 1200-mV reference voltage

= 0x1a4

= 282mV

2. INTFB 7.6.4 VOUT_FS Register (Address = 4h) [reset = 00000011h]

Figure 7-19. VOUT_FS Register

7	6	5	4	3	2	1	0
FB	RESERVED					INTFB	
R/W-0b	R/W-00000b					R/W-11b	

Table 7-7. VOUT_FS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FB	R/W	0b	Output feedback voltage 0b = Use internal output voltage feedback. The FB/INT pin is the indicator for output short circuit protection, overcurrent status, and overvoltage status (Default). 1b = Use external output voltage feedback. The FB/INT pin is the feedback input of the output voltage.
6-2	RESERVED	R	00000b	Reserved
1-0	INTFB	R/W	11b	Internal feedback ratio 00b = Set internal feedback ratio to 0.2256 01b = Set internal feedback ratio to 0.1128 10b = Set internal feedback ratio to 0.0752 11b = Set internal feedback ratio to 0.0564 (Default)

= 0x03

= 0.0564

< Record Index 1 of TPS65987DDH >

Record index 1 (0x1)

Field	Value
Trigger Event	Power On Reset
Data Length	3
Slave Address Index	1
Data	0x1a400

Data : 0x 1 a 4 0 0

Register address 00h

'3 'Byte of 'Data Length ", Set '0x1a4 "

< Record Index 2 of TPS65987DDH >

Record index 2 (0x2)

Field	Value
Trigger Event	Power On Reset
Data Length	2
Slave Address Index	1
Data	0x0304

$$V_{OUT} = \frac{V_{REF}}{INTFB}$$ = 282mV / 0.0564 = 5.0V

TPS55289 Register settings — POR

3. Output enable 7.6.6 MODE Register (Address = 6h) [reset = 00100000h]

Figure 7-21. MODE Register

7	6	5	4	3	2	1	0
OE	FSW	HICCUP	DISCHG	Reserved	Reserved	FPWM	Reserved
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Table 7-10. MODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OE	R/W	0b	Output enable 0b = Output disabled (Default) 1b = Output enable
6	FSWDBL	R/W	0b	Switching frequency doubling in buck-boost mode TI does not recommend using double frequency function at switching frequency above 1.6 MHz. 0b = Keep the switching frequency unchanged during buck-boost mode (Default) 1b = Double the switching frequency during buck-boost mode
5	HICCUP	R/W	1b	Hiccup mode 0b = Disable the hiccup during output short circuit protection. 1b = Enable the hiccup during output short circuit protection (Default)
4	DISCHG	R/W	0b	Output discharge 0b = Disabled VOUT discharge when the device is in shutdown mode (Default) 1b = Enable VOUT discharge. VOUT is discharged to ground by an internal 100-mA current sink
3	RESERVED	R	0b	Reserved
2	RESERVED	R	0b	Reserved
1	FPWM	R/W	0b	Select operating mode at light load condition 0b = PFM operating mode at light load condition (Default) 1b = FPWM operating mode at light load condition
0	RESERVED	R	0b	Reserved

= 0xa0

< Record Index 3 of TPS65987DDH >

Record index 3 (0x3)

Field	Value
Trigger Event	Power On Reset
Data Length	2
Slave Address Index	1
Data	0xa006

TPS55289 Register settings — PDO x

4. PDO 1 (5V)

$$V_{OUT} = \frac{V_{REF}}{INTFB} = 282mV / 0.0564 = 5.0V$$

5. PDO2 (9V)

$$V_{OUT} = \frac{V_{REF}}{INTFB} = 508mV / 0.0564 = 9.0V$$

011 00110100b = 508-mV reference voltage

= 0x334

6. PDO3 (15V)

$$V_{OUT} = \frac{V_{REF}}{INTFB} = 846mV / 0.0564 = 15V$$

101 10001100b = 846-mV reference voltage

= 0x58c

7. PDO4 (20V)

$$V_{OUT} = \frac{V_{REF}}{INTFB} = 1128mV / 0.0564 = 20V$$

111 10000000b = 1129-mV reference voltage

= 0x130c

< Record Index 4 of TPS65987DDH >

Record index 4 (0x4)

Field	Value
Trigger Event	Source PDO 1 Negotiated
Data Length	3
Slave Address Index	1
Data	0x1a400

< Record Index 5 of TPS65987DDH >

Record index 5 (0x5)

Field	Value
Trigger Event	Source PDO 2 Negotiated
Data Length	3
Slave Address Index	1
Data	0x33400

< Record Index 6 of TPS65987DDH >

Record index 6 (0x6)

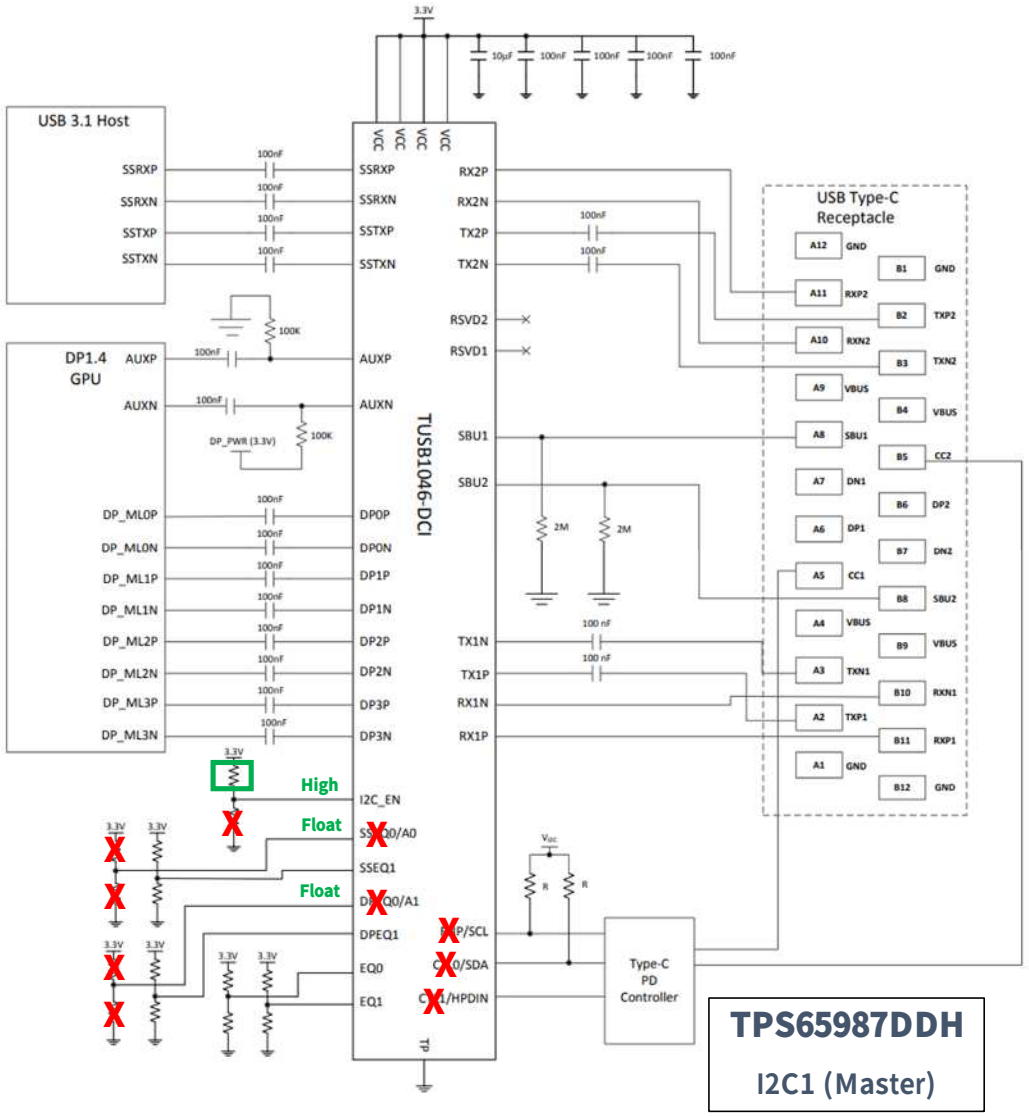
Field	Value
Trigger Event	Source PDO 3 Negotiated
Data Length	3
Slave Address Index	1
Data	0x58c00

< Record Index 7 of TPS65987DDH >

Record index 7 (0x7)

Field	Value
Trigger Event	Source PDO 4 Negotiated
Data Length	3
Slave Address Index	1
Data	0x130b0

TUSB1046 circuit



I2C_EN pin = I2C mode

I2C_EN	17	4 Level I	I²C Programming Mode or GPIO Programming Select. I2C is only disabled when this pin is '0'. 0 = GPIO mode (I²C disabled) R = TI Test Mode (I²C enabled at 3.3 V) F = I²C enabled at 1.8 V 1 = I²C enabled at 3.3 V.

I2C Slave Address = 0x12

Table 7-9. TUSB1046-DCI I²C Target Address

DPEQ0/A1 PIN LEVEL	SSEQ0/A0 PIN LEVEL	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
0	0	1	0	0	0	1	0	0
0	R	1	0	0	0	1	0	1
0	F	1	0	0	0	1	1	0
0	1	1	0	0	0	1	1	1
R	0	0	1	0	0	0	0	0
R	R	0	1	0	0	0	0	1
R	F	0	1	0	0	0	1	0
R	1	0	1	0	0	0	1	1
F	0	0	0	1	0	0	0	0
F	R	0	0	1	0	0	0	1
F	F	0	0	1	0	0	1	0
F	1	0	0	1	0	0	1	1
1	0	0	0	0	1	1	0	0
1	R	0	0	0	1	1	0	1
1	F	0	0	0	1	1	1	0
1	1	0	0	0	1	1	1	1

< I2C Master Configuration (0x64) of TPS65987DDH >

Slave 1 Configuration

Field	Value
Slave 1 I2C Address	0x12
Slave 1 Master Selection	I2C1

TUSB1046 Register settings — POR

8. REG0x0A initialize

7.6.1 General Register (address = 0x0A) [reset = 00000001]

Figure 7-2. General Registers

7	6	5	4	3	2	1	0
Reserved		SWAP_HPDIN	EQ_OVERRIDE	HPDIN_OVRRIDE	FLIPSEL	CTLSEL[1:0]	
R		R/W	R/W	R/W	R/W	R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-11. General Registers

Bit	Field	Type	Reset	Description
7:6	Reserved.	R	00	Reserved.
5	SWAP_HPDIN	R/W	0	0 – HPDIN is in default location (Default) 1 – HPDIN location is swapped (PIN 23 to PIN 32, or PIN 32 to PIN23).
4	EQ_OVERRIDE	R/W	0	Setting of this field will allow software to use EQ settings from registers instead of value sample from pins. 0 – EQ settings based on sampled state of the EQ pins (SSEQ[1:0], EQ[1:0], and DPEQ[1:0]). 1 – EQ settings based on programmed value of each of the EQ registers
3	HPDIN_OVRRIDE	R/W	0	0 – HPD IN based on state of HPD_IN pin (Default) 1 – HPD_IN high.
2	FLIPSEL	R/W	0	FLIPSEL. Refer to Table 7-5 and Table 7-6 for this field functionality.
1:0	CTLSEL[1:0]	R/W	01	00 – Disabled. All RX and TX for USB3 and DisplayPort are disabled. 01 – USB3.1 only enabled. (Default) 10 – Four DisplayPort lanes enabled. 11 – Two DisplayPort lanes and one USB3.1

< Record Index 8 of TPS65987DDH >

Record index 8 (0x8)

Field	Value
Trigger Event	Power On Reset
Data Length	2
Slave Address Index	0
Data	0xa

9. REG0x13 initialize

7.6.5 DisplayPort Control/Status Registers (address = 0x13) [reset = 00000000]

Figure 7-6. DisplayPort Control/Status Registers (0x13)

7	6	5	4	3	2	1	0
AUX_SNOOP_DISABLE	Reserved	AUX_SBU_OVR		DP3_DISABLE	DP2_DISABLE	DP1_DISABLE	DP0_DISABLE
R/W	R	R/W		R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 7-15. DisplayPort Control/Status Registers (0x13)

Bit	Field	Type	Reset	Description
7	AUX_SNOOP_DISABLE	R/W	0	0 – AUX snoop enabled. (Default) 1 – AUX snoop disabled.
6	Reserved	R	0	Reserved
5:4	AUX_SBU_OVR	R/W	00	This field overrides the AUXp or AUXn to SBU1 or SBU2 connect and disconnect based on CTL1 and FLIP. Changing this field to 1'b1 will allow traffic to pass through AUX to SBU regardless of the state of CTLSEL1 and FLIPSEL register 00 – AUX to SBU connect/disconnect determined by CTLSEL1 and FLIPSEL (Default) 01 – AUXp -> SBU1 and AUXn -> SBU2 connection always enabled. 10 – AUXp -> SBU2 and AUXn -> SBU1 connection always enabled. 11 = AUX to SBU open.
3	DP3_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 3. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 3 functionality. 0 – DP Lane 3 Enabled (default) 1 – DP Lane 3 Disabled.
2	DP2_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 2. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 2 functionality 0 – DP Lane 2 Enabled (default) 1 – DP Lane 2 Disabled.
1	DP1_DISABLE	R/W	0	When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 1. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 1 functionality 0 – DP Lane 1 Enabled (default) 1 – DP Lane 1 Disabled.
0	DP0_DISABLE	R/W	0	DISABLE. When AUX_SNOOP_DISABLE = 1'b1, this field can be used to enable or disable DP lane 0. When AUX_SNOOP_DISABLE = 1'b0, changes to this field will have no effect on lane 0 functionality. 0 – DP Lane 0 Enabled (default) 1 – DP Lane 0 Disabled.

< Record Index 9 of TPS65987DDH >

Record index 9 (0x9)

Field	Value
Trigger Event	Power On Reset
Data Length	2
Slave Address Index	0
Data	0x8013

Application report SLVAEM6

	Trigger Event	Register	Value
Index1	Power On Reset	A	0
Index2	Power On Reset	13	80

TUSB1046 Register settings — Cable Attach

10. REG0x0A : EQ_OVERRIDE ON, USB3.1 only enabled
11. REG0x0A : EQ_OVERRIDE ON, USB3.1 only enabled, FLIPSEL

< Record Index 10 of TPS65987DDH >

Record index 10 (0xa)

Field	Value
Trigger Event	Cable Attach CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x110a

< Record Index 11 of TPS65987DDH >

Record index 11 (0xb)

Field	Value
Trigger Event	Cable Attach CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x150a

12. REG0x13 : AUX_SNOOP_DISABLE
13. REG0x13 : AUX_SNOOP_DISABLE

< Record Index 12 of TPS65987DDH >

Record index 12 (0xc)

Field	Value
Trigger Event	Cable Attach CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x8013

< Record Index 13 of TPS65987DDH

Record index 13 (0xd)

Field	Value
Trigger Event	Cable Attach CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x8013

Application report SLVAEM6

Index3	Cable Attach CC_1 PD	0A	11
Index4	Cable Attach CC_2_PD	0A	15
Index5	Cable Attach CC_1 PD	13	80
Index6	Cable Attach CC_2_PD	13	80

TUSB1046 Register settings — DisplayPort Pin Config A,C or E

14. REG0x0A : EQ_OVERRIDE ON, **4 DP lanes enabled**
16. REG0x0A : EQ_OVERRIDE ON, **4 DP lanes enabled**, FLIPSEL

< Record Index 14 of TPS65987DDH >

Record index 14 (0xe)

Field	Value
Trigger Event	Displayport Pin Config A,C or E CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x120a

< Record Index 16 of TPS65987DDH >

Record index 16 (0x10)

Field	Value
Trigger Event	Displayport Pin Config A,C or E CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x160a

15. REG0x13 : AUX_SNOOP_DISABLE
17. REG0x13 : AUX_SNOOP_DISABLE

< Record Index 15 of TPS65987DDH >

Record index 15 (0xf)

Field	Value
Trigger Event	Displayport Pin Config A,C or E CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x8013

< Record Index 17 of TPS65987DDH

Record index 17 (0x11)

Field	Value
Trigger Event	Displayport Pin Config A,C or E CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x8013

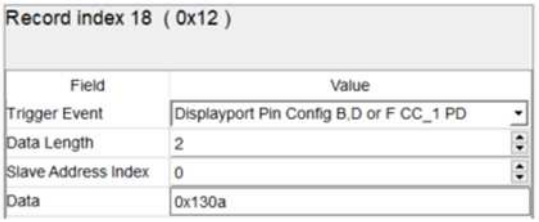
Application report SLVAEM6

Index7	DisplayPort Pin Config A, C or E CC_1 PD	0A	12
Index8	DisplayPort Pin Config A, C or E CC_1 PD	13	80
Index9	DisplayPort Pin Config A, C or E CC_2 PD	0A	16
Index10	DisplayPort Pin Config A, C or E CC_2 PD	13	80

TUSB1046 Register settings – DisplayPort Pin Config B,D or F

18. REG0x0A : EQ_OVERRIDE ON, **2 DP lanes enabled**
20. REG0x0A : EQ_OVERRIDE ON, **2 DP lanes enabled**, FLIPSEL

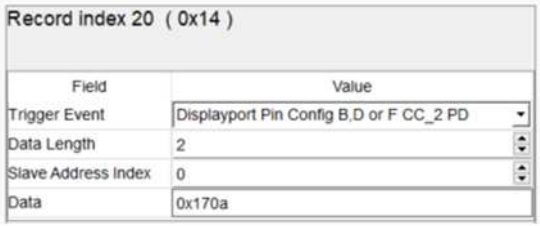
< Record Index 18 of TPS65987DDH >



Record index 18 (0x12)

Field	Value
Trigger Event	Displayport Pin Config B,D or F CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x130a

< Record Index 20 of TPS65987DDH >

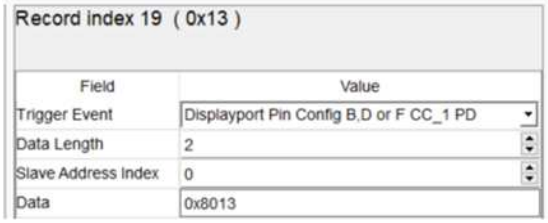


Record index 20 (0x14)

Field	Value
Trigger Event	Displayport Pin Config B,D or F CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x170a

19. REG0x13 : AUX_SNOOP_DISABLE
21. REG0x13 : AUX_SNOOP_DISABLE

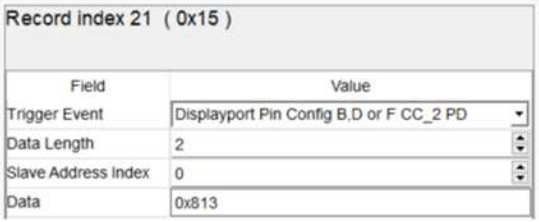
< Record Index 19 of TPS65987DDH >



Record index 19 (0x13)

Field	Value
Trigger Event	Displayport Pin Config B,D or F CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x8013

< Record Index 21 of TPS65987DDH



Record index 21 (0x15)

Field	Value
Trigger Event	Displayport Pin Config B,D or F CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x813

Application report SLVAEM6

Index11	DisplayPort Pin Config B, D or F CC_1 PD	0A	13
Index12	DisplayPort Pin Config B, D or F CC_1 PD	13	80
Index13	DisplayPort Pin Config B, D or F CC_2PD	0A	17
Index14	DisplayPort Pin Config B, D or F CC_2PD	13	80

TUSB1046 Register settings — DisplayPort Exited

22. REG0x0A : EQ_OVERRIDE ON, USB3.1 only enabled
24. REG0x0A : EQ_OVERRIDE ON, USB3.1 only enabled, FLIPSEL

< Record Index 22 of TPS65987DDH >

Record index 22 (0x16)

Field	Value
Trigger Event	Displayport Exited CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x110a

< Record Index 24 of TPS65987DDH >

Record index 24 (0x18)

Field	Value
Trigger Event	Displayport Exited CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x150a

23. REG0x13 : AUX_SNOOP_DISABLE
25. REG0x13 : AUX_SNOOP_DISABLE

< Record Index 23 of TPS65987DDH >

Record index 23 (0x17)

Field	Value
Trigger Event	Displayport Exited CC_1 PD
Data Length	2
Slave Address Index	0
Data	0x8013

< Record Index 25 of TPS65987DDH

Record index 25 (0x19)

Field	Value
Trigger Event	Displayport Exited CC_2 PD
Data Length	2
Slave Address Index	0
Data	0x8013

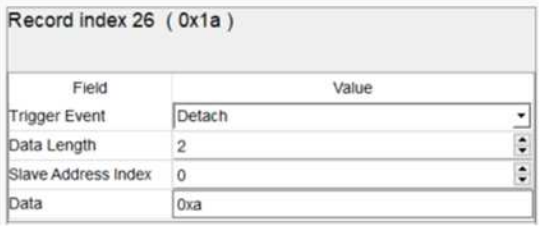
Application report SLVAEM6

Index15	DisplayPort Exited C CC_1 PD	0A	11
Index16	DisplayPort Exited C CC_1 PD	13	80
Index17	DisplayPort Exited C CC_2 PD	0A	15
Index18	DisplayPort Exited C CC_2 PD	13	80

TUSB1046 Register settings — Detach

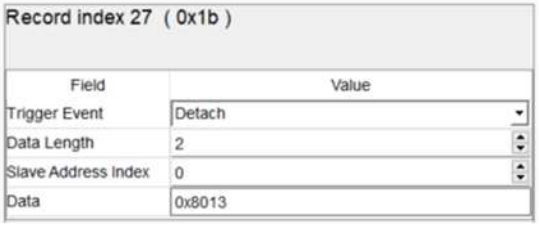
26. REG0x0A initialize

< Record Index 26 of TPS65987DDH >



27. REG0x13 initialize

< Record Index 27 of TPS65987DDH >



Application report SLVAEM6

Index19	Detach	A	0
Index20	Detach	13	80

App Config Binary Data Indices (0x62)

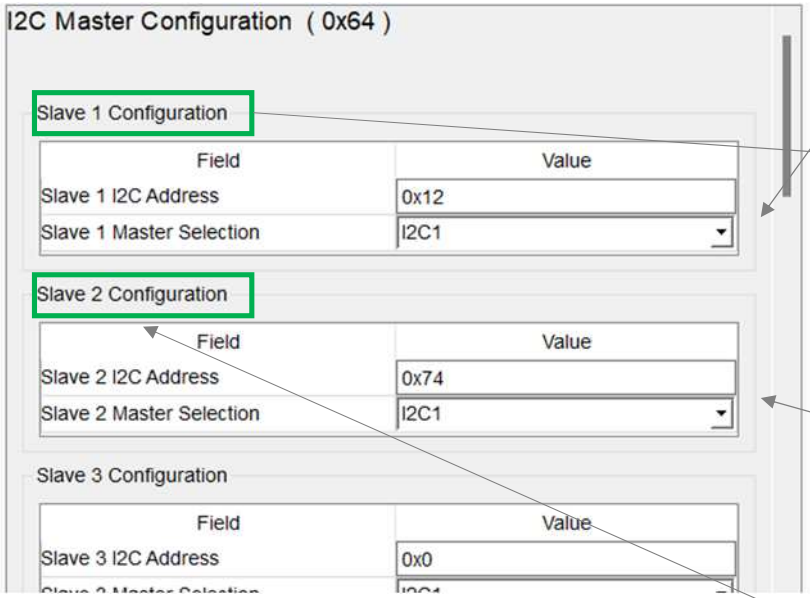
App Config Binary Data Indices (0x62)

Field	Value
Country Codes Start Index	0
Country Codes Number of Indices	0
Common I2C Record Start Index	0
Common I2C Record Number of Indices	0
Port 1 I2C Record Start Index	1
Port 1 I2C Record Number of Indices	27
Port 2 I2C Record Start Index	0
Port 2 I2C Record Number of Indices	0

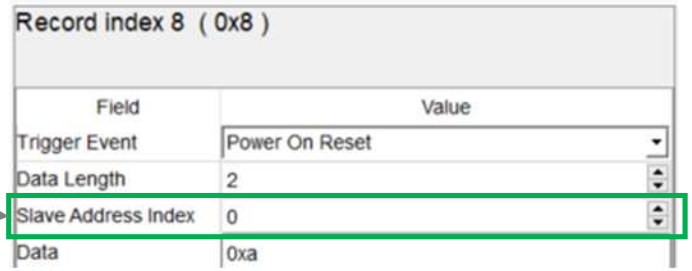
Index 1 to Index 27 of I2C Controller Evens.

‘Port 1 ”and ‘Port 2 ”means USB Port.
TPS65987 is single, Port 1 only.
TPS65988 is dual, use Port1 and Port2.

I2C Master Configuration (0x64)

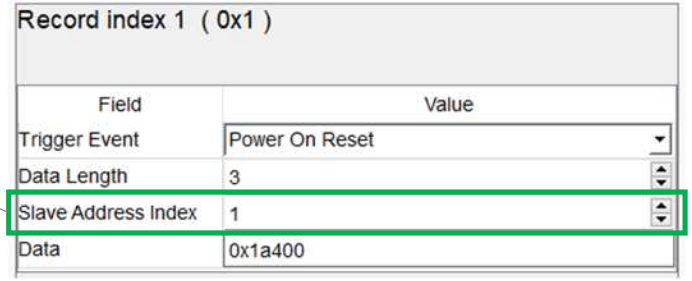


TUSB1046 I2C Slave address 0x12



‘Slave Address Index 0 ”of I2C Controller Evens means first ‘Slave 1 configuration ”

TPS55289 I2C Slave address 0x74



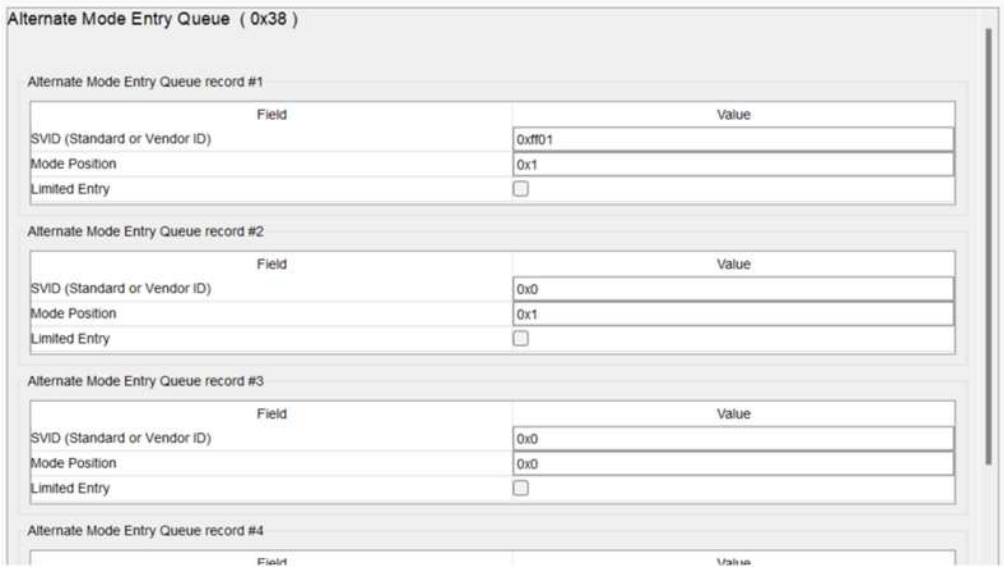
Next ‘Slave 2 configuration ”; ‘Slave Address Index 1 ”

Display Port Capabilities (0x51)

DisplayPort Alternate Mode Capabilities Host Interface Registers

The following configuration registers affect the negotiation and behavior of the DisplayPort alternate mode on TPS65981, TPS65982, TPS65986, TPS65987D and TPS65988 devices:

- 0x38, Alternate Mode entry sequence
- 0x47, TX identity data objects
- 0x51, DisplayPort capabilities
- 0x5C, GPIO event map



Application report SLVUBH2B

0x38	Alternate Mode Entry Sequence	RW	16	Allows for selection of up to four alternate modes along with their sequence for auto entry attempt. A single mode will be entered automatically if valid. See Table 3-33. Initialized by Application Customization.

3.17 0x38 Alternate Mode Entry Sequence

Table 3-33. 0x38 Alternate Mode Entry Sequence Register

Address	Name	Access	Length	Power-Up Default
0x38	Alternate Mode Entry Sequence	Read/Write	16	0 (Initialized by Application Customization)

Table 3-34. 0x38 Alternate Mode Entry Sequence Register Bit Field Definitions

Bits	Name	Description
Bytes 13-16:SVID/Mode 4		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for fourth mode for entry attempt
Bytes 9-12:SVID/Mode 3		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for third mode for entry attempt
Bytes 5-8:SVID/Mode 2		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for second mode for entry attempt
Bytes 1-4:SVID/Mode 1		
31:25	Reserved	Reserved.
24	LimitedEntry	When set, entry to this mode is only possible if no other port has currently entered this mode. This bit is only applicable when GlobalSystemConfig.MultiPortAMpolicy = 01b, otherwise is a do not care.
23:16	ModeIndex(1)	Mode index.
15:0	SVID(1)	SVID for first mode for entry attempt

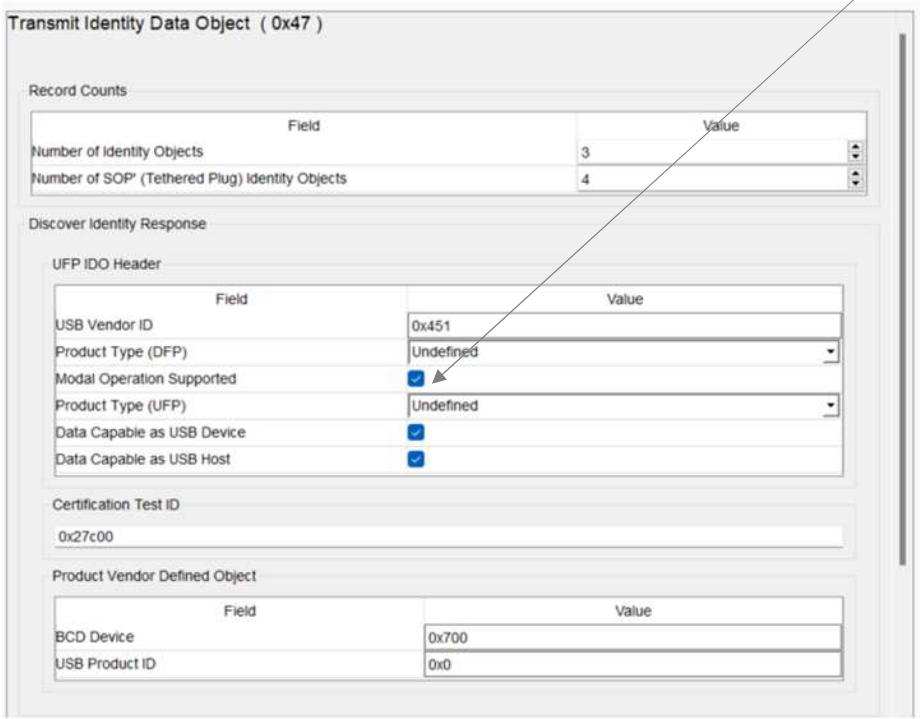
Display Port Capabilities (0x51)

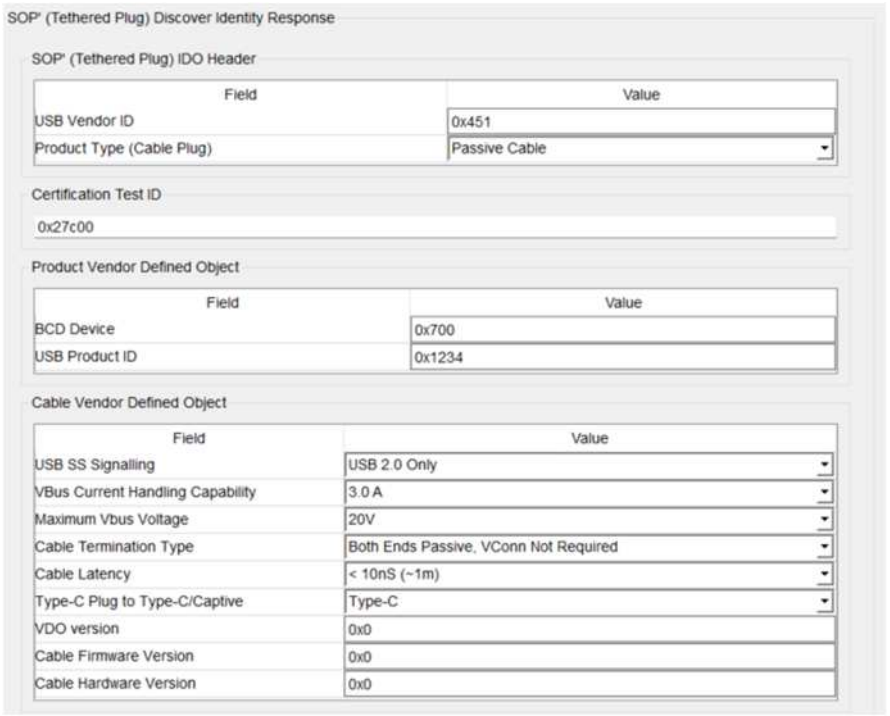
DisplayPort Alternate Mode Capabilities Host Interface Registers

The following configuration registers affect the negotiation and behavior of the DisplayPort alternate mode on TPS65981, TPS65982, TPS65986, TPS65987D and TPS65988 devices:

- 0x38, Alternate Mode entry sequence
- 0x47, TX identity data objects
- 0x51, DisplayPort capabilities
- 0x5C, GPIO event map

Confirm ‘Modal Operation Supported ”





Display Port Capabilities (0x51)

DisplayPort Alternate Mode Capabilities Host Interface Registers

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- 0x38, Alternate Mode entry sequence
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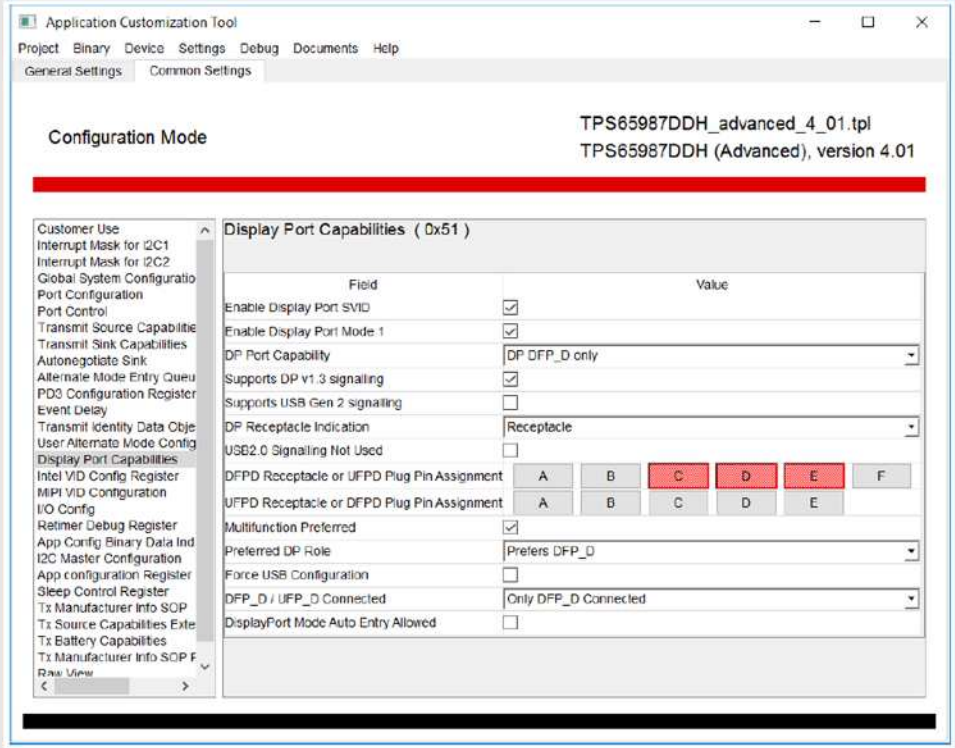
- 0x51, DisplayPort capabilities
- 0x5C, GPIO event map

Display Port Capabilities (0x51)

Field	Value
Enable Display Port SVID	☑
Enable Display Port Mode 1	☑
DP Port Capability	DP DFP_D only
Supports DP v1.3 signalling	☑
Supports USB Gen 2 signalling	☐
DP Receptacle Indication	Receptacle
USB2.0 Signalling Not Used	☐
DFPD Receptacle or UFPD Plug Pin Assignment	A B C D E F
UFPD Receptacle or DFPD Plug Pin Assignment	A B C D E
Multifunction Preferred	☑
Preferred DP Role	Prefers DFP_D
DFP_D / UFP_D Connected	Only DFP_D Connected
DisplayPort Mode Auto Entry Allowed	☐

Application report SLVA884B

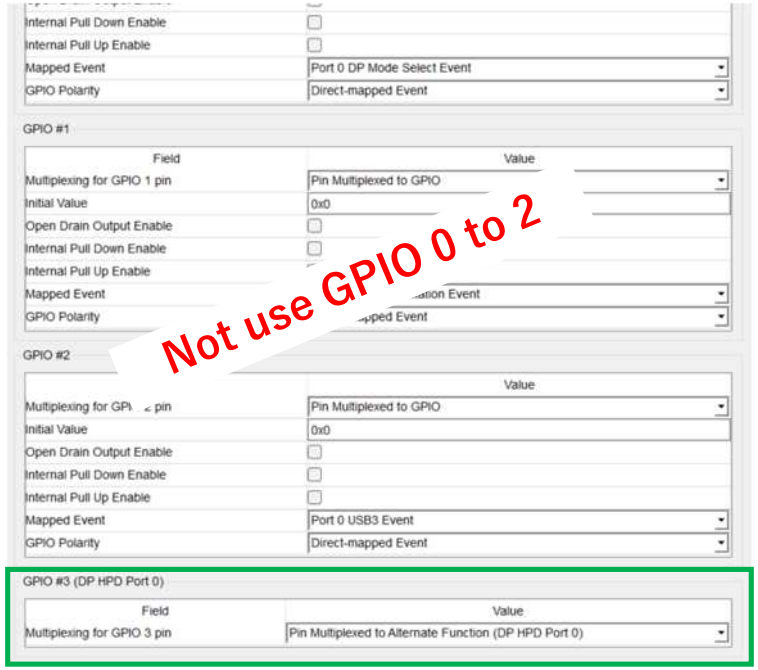


Display Port Capabilities (0x51)

DisplayPort Alternate Mode Capabilities Host Interface Registers

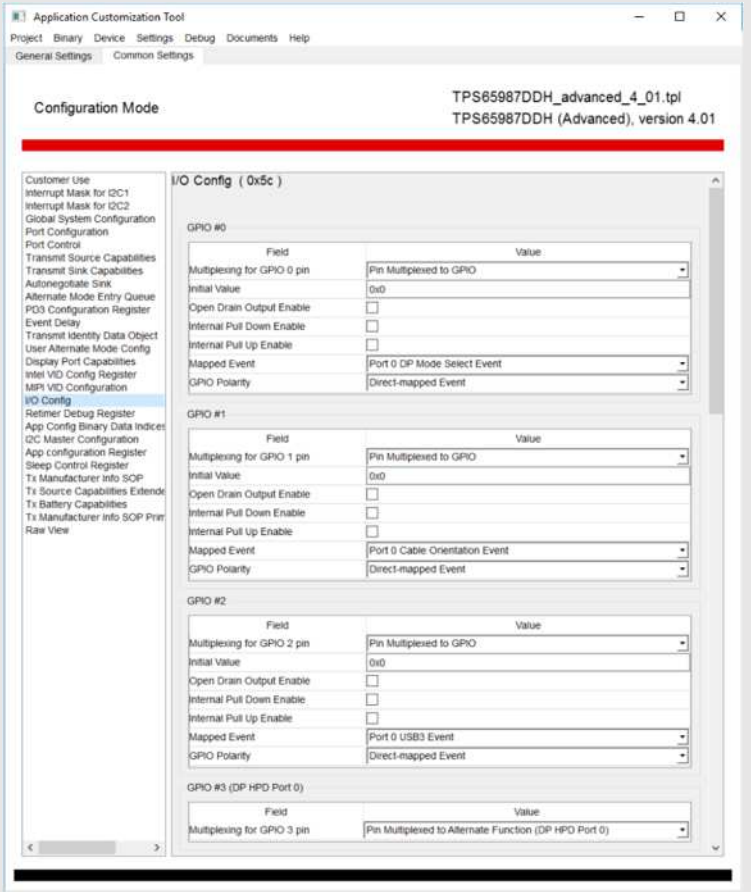
The following configuration registers affect the negotiation and behavior of the DisplayPort alternate mode on TPS65981, TPS65982, TPS65986, TPS65987D and TPS65988 devices:

- 0x38, Alternate Mode entry sequence
- 0x47, TX identity data objects
- 0x51, DisplayPort capabilities
- 0x5C, GPIO event map

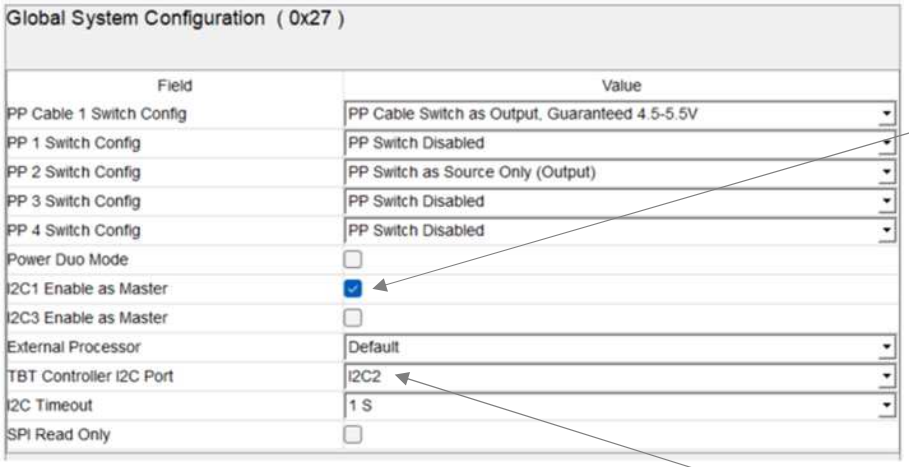


Confirm for GPIO3(HPD), Because only I2C mode.

Application report SLVA884B



Global System Configuration (0x27)



Check I2C1 Enable as Master

Select I2C2 of TBT Controller I2C Port (Not use TBT)