TPS2662x 60-V, 800-mA Industrial eFuse with integrated input and output reverse polarity protection

1 Features

- 4.5 V to 57 V Operating Voltage, 60-V Absolute Maximum
- Integrated Reverse Input Polarity Protection to –60 V
- Integrated Reverse Output Polarity Protection to –(60 – V_{IN}) (TPS26624 and TPS26625 Only)
- Integrated Back to Back MOSFETs With 478-mΩ Total RON
- 25 mA to 880 mA Adjustable Current Limit (±5% accuracy at 880 mA)
- Load Protection During Surge (IEC 61000-4-5) With Minimum External Components
- Electrical Fast Transients Immunity According to IEC 61000-4-4
- Fast Reverse Current Blocking Response (0.3 µs)
- Adjustable UVLO, OVP Cut Off, Output Slew Rate Control for Inrush Current Limiting
- Fixed 38-V Over Voltage Clamp (TPS26622 and TPS26623 only)
- Low Quiescent Current, 340 µA in Operating, 12 µA in Shutdown
- Small Foot Print - 10L (3 mm × 3 mm) VSON
- UL 2367 Recognition Pending

2 Applications

- PLC I/O Modules
- AC and Servo Drives
- Sensor and Controls
- Thermostat
- PoE Highside Protection

3 Description

The TPS2662x family are compact, feature rich high voltage eFuses with a full suite of protection features. The wide supply input range of 4.5 V to 57 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from positive and negative supply voltages up to ±60 V. The TPS26624 and TPS26625 devices support both input as well as output reverse polarity protection feature. Integrated back to back FETs provide reverse current blocking feature making the device suitable for systems with output voltage holdup requirements during power fail and brownout conditions. Load, source and device protection are provided with many adjustable features including overcurrent, output slew rate and overvoltage, undervoltage thresholds. The internal robust protection control blocks along with the high voltage rating of the TPS2662x family helps to simplify the system designs for Surge protection.

The TPS26620, TPS26622 and TPS26624 feature Latch off and TPS26621, TPS26623 and TPS26625 feature Auto-Retry functionality are the over temperature and over current fault events.

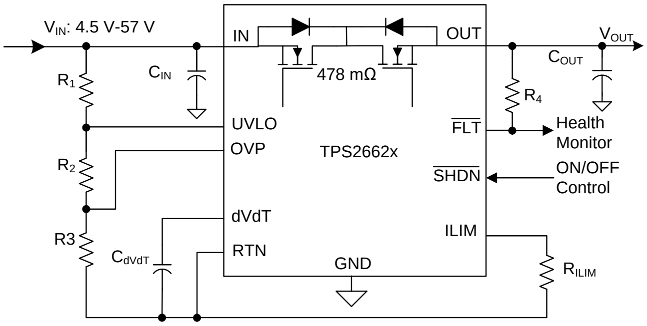
The devices are available in a 3 mm × 3 mm 10-pin SON package and are specified over a –40°C to +125°C temperature range.

Device Information[(1)]

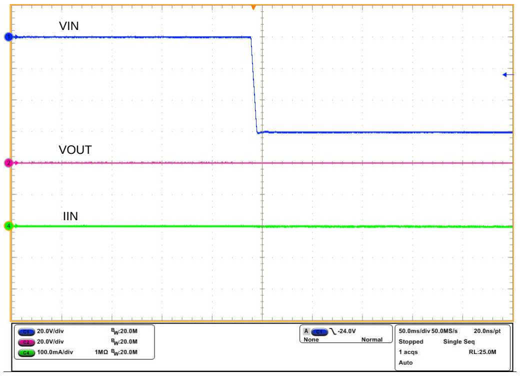
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS26620 TPS26621 TPS26622 TPS26623 TPS26624 TPS26625	SON (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Reverse Input Polarity Protection at –60-V Supply



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4 Revision History

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• Changed SHDN pin voltage from 4 V to 6 V in the *Recommended Operating Conditions* table in the Specifications section	5

Changes from Revision B (April 2018) to Revision C	Page
• Changed status from Advanced Information to Production Data	1

Changes from Revision A (March 2018) to Revision B	Page
• Changed Repinse to Response in the *Device Comparison* table header	3

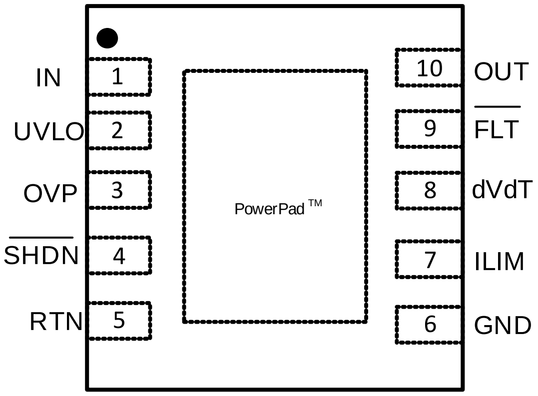
Changes from Original (October 2017) to Revision A	Page
• Changed from one page to full data sheet	1

5 Device Comparison Table

PART NUMBER	OVERVOLTAGE PROTECTION	OVERLOAD and THERMAL FAULT RESPONSE	REVERSE POLARITY PROTECTION
TPS26620	Overvoltage cut-off, adjustable	Latch Off	Input side
TPS26621	Overvoltage cut-off, adjustable	Auto-Retry	Input side
TPS26622	Overvoltage clamp, fixed (38 V)	Latch Off	Input side
TPS26623	Overvoltage clamp, fixed (38 V)	Auto-Retry	Input side
TPS26624	Overvoltage cut-off, adjustable	Latch Off	Input and Output side
TPS26625	Overvoltage cut-off, adjustable	Auto-Retry	Input and Output side

6 Pin Configuration and Functions

DRC Package
10-Pin VSON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	IN	Power	Input supply voltage.
2	UVLO	I	Resistor programmable undervoltage lockout threshold setting input. An undervoltage event will open the internal FET. If the Undervoltage Lock Out function is not needed, the UVLO terminal must be connected to the IN terminal with atleast 1 MΩ resistor. UVLO pin is 5 V rated and this resistor limits the UVLO pin current to < 60 µA
3	OVP	I	Resistor programmable overvoltage protection threshold. An overvoltage event will open internal FET. In TPS26620, TPS26621, TPS26624, TPS26625 devices if over voltage protection feature is not to be used then connect OVP terminal to RTN. For overvoltage clamp response (TPS26622 and TPS26623 Only) connect OVP to RTN externally.
4	$\overline{\text{SHDN}}$	I	Shutdown PIN. Pulling it low makes the device to enter into low power shutdown mode. Cycling $\overline{\text{SHDN}}$ low and then back high resets the device that has latched off (TPS26620, TPS26622, TPS26623 only) due to a fault condition.
5	RTN	–	Reference ground for all internal voltages.
6	GND	–	System Ground.
7	ILIM	I/O	A resistor from this pin to RTN sets the overload and short-circuit current limit. See the Overload and Short Circuit Protection section.
8	dVdT	I/O	A capacitor from this pin to RTN sets output voltage slew rate. See the Hot Plug-In and In-Rush Current Control section.
9	$\overline{\text{FLT}}$	O	Fault event indicator. It is an open drain output. If unused, leave floating.
10	OUT	Power	Output Voltage.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NO.	NAME		
–	PowerPad^{TM}	–	Connect PowerPad to RTN plane for heat sinking. Do not use PowerPad as the only electrical connection to RTN.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, all voltages referred to GND (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range	IN, IN–OUT	–60	60	V
	OUT (TPS26624 and TPS26625 Only)	$-(60-V_{IN})$	60	
	IN, IN–OUT (10 ms transient), T_A = 25 ℃	–70	70	
	[IN, OUT, $\overline{\text{FLT}}$, $\overline{\text{SHDN}}$] to RTN	–0.3	60	
	[UVLO, OVP, dVdT, ILIM] to RTN	–0.3	5	
	RTN	–60	0.3	
Sink current	$I_{\overline{FLT}}$, I_{dVdT}, $I_{\overline{SHDN}}$		10	mA
Source current	I_{dVdT}, I_{ILIM}	Internally limited		
Operating junction temperature	T_J	–40	150	°C
Transient junction temperature		–65	$T_{(TSD)}$	°C
Storage temperature	T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
IN	Input voltage	4.5		57	V
OUT, $\overline{\text{FLT}}$	Input voltage	0		57	V
UVLO, OVP, dVdT, ILIM	Input voltage	0		4	V
$\overline{\text{SHDN}}$	Input voltage	0		6	V
ILIM	Resistance	7.5		267	kΩ
IN, OUT	External capacitance	0.1			µF
dVdT		6.8			nF
T_j	Operating junction temperature	–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS2662	UNIT
		DRC (VSON)	
		10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		TPS2662	UNIT
		DRC (VSON)	
		10 PINS	
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.4	°C/W

7.5 Electrical Characteristics

–40°C ≤ $T_A = T_J$ ≤ +125°C, $V_{(IN)} = 24$ V, $V_{(\overline{SHDN})} = 2$ V, $R_{(ILIM)} = 267$ kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)} = 1$ µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$V_{(IN)}$	Operating input voltage		4.5		57	V
$V_{(PORR)}$	Internal POR threshold, rising		3.54	3.73	4.2	V
$V_{(PORHys)}$	Internal POR hysteresis			110		mV
$IQ_{(ON)}$	Supply current	Enabled: $V_{(\overline{SHDN})} = 2$ V		343	482	µA
$IQ_{(OFF)}$		$V_{(\overline{SHDN})} = 0$ V		11.5	25	µA
$I_{(VINR)}$	Reverse Input supply current	$V_{(IN)} = -24$ V, $V_{(OUT)} = 0$ V		50	130	µA
$V_{(OVC)}$	Over voltage clamp	$V_{(IN)} > 40$ V, ILOAD = 10 mA,TPS26622, TPS26623 Only	36	37.5	40	V
UNDERVOLTAGE LOCKOUT (UVLO) INPUT						
$V_{(UVLOR)}$	UVLO threshold voltage, rising		1.18	1.2	1.23	V
$V_{(UVLOF)}$	UVLO threshold, Falling		1.09	1.1	1.135	V
$I_{(UVLO)}$	UVLO Input Leakage Current	0 V ≤ $V_{(UVLO)}$ ≤ 3.5 V	–100	0	100	nA
$I_{(UVLO)}$	UVLO Input Leakage Current	$V_{(UVLO)} = 5$ V		18.8	38	µA
OVER VOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	Overvoltage threshold voltage, rising		1.18	1.2	1.23	V
$V_{(OVPF)}$	Overvoltage threshold, falling		1.09	1.12	1.135	V
$I_{(OVP)}$	OVP Input Leakage Current	0 V ≤ $V_{(OVP)}$ ≤ 5 V	–100	0	100	nA
LOW IQ SHUTDOWN ($\overline{SHDN}$) INPUT						
$V_{(\overline{SHDN})}$	Output voltage	$I_{(\overline{SHDN})} = 0.1$ µA	2.39	2.781	3.1	V
$V_{(SHUTF)}$	$\overline{SHDN}$ Threshold Voltage for Low IQ Shutdown, Falling		0.9			V
$V_{(SHUTR)}$	$\overline{SHDN}$ Threshold, rising				1.8	V
$I_{(\overline{SHDN})}$	Input current	$V_{(\overline{SHDN})} = 0.4$ V	–10	–2.4		µA
OUTPUT RAMP CONTROL (dVdT)						
$I_{(dVdT)}$	dVdT Charging Current	$V_{(dVdT)} = 0$V	1.68	1.98	2.33	µA
$R_{(dVdT)}$	dVdT Discharging Resistance	$V_{(\overline{SHDN})} = 0$ V, with $I_{(dVdT)} = 10$mA sinking		13.1	22	Ω
$V_{(dVdTmax)}$	dVdT Max Capacitor Voltage		4	4.34	4.75	V
$GAIN_{(dVdT)}$	dVdT to OUT Gain	$V_{(OUT)} / V_{(dVdT)}$	23.9	24.6	25.2	V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$V_{(ILIM)}$	ILIM bias voltage			1		V

Electrical Characteristics (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(OL)}$	Overload Current Limit	$R_{(ILIM)}$ = 267 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.02	0.025	0.032	A
		$R_{(ILIM)}$ = 44.2 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.145	0.152	0.159	
		$R_{(ILIM)}$ = 26.7 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.237	0.25	0.257	
		$R_{(ILIM)}$ = 13.3 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.47	0.5	0.52	
		$R_{(ILIM)}$ = 8.25 kΩ, $V_{(IN)}$ – $V_{(OUT)}$ = 1 V	0.757	0.8	0.827	
		$R_{(ILIM)}$ = 7.5 kΩ, $V_{(IN)}$ – $V_{(OUT)}$= 1 V	0.83	0.88	0.91	
$I_{(OL\_R-OPEN)}$		$R_{(ILIM)}$= OPEN, Open Resistor Current Limit (single point failure test: UL60950)	8	15.5	27	mA
$I_{(OL\_R-SHORT)}$		$R_{(ILIM)}$= SHORT, Shorted Resistor Current Limit (single point failure test: UL60950)	31	39.3	51	mA
$I_{(SCL)}$	Short-Circuit Current Limit	$R_{(ILIM)}$ = 7.5 kΩ, $V_{(IN)}$ – $V_{(OUT)}$= 24 V		0.885		A
$I_{(FASTRIP)}$	Fast-Trip Comparator Threshold			1.6		A
PASS FET OUTPUT (OUT)						
R_{ON}		0.025 A ≤ $I_{(OUT)}$ ≤ 0.8 A, T_J = 25°C, $R_{(ILIM)}$ = 7.5 kΩ	435	478	521	mΩ
		0.025 A ≤ $I_{(OUT)}$ ≤ 0.8A, T_J = 85°C, $R_{(ILIM)}$ = 7.5 kΩ		626	685	
		0.025 A ≤ $I_{(OUT)}$ ≤ 0.8A, –40ºC ≤ T_J ≤125°C, $R_{(ILIM)}$ = 7.5 kΩ	250	478	800	
$I_{lkg(OUT)}$	OUT Leakage Current in Off State	$V_{(IN)}$ = 57 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 0 V, Sourcing		4.38	12	µA
		$V_{(IN)}$ = 0 V, $V_{(\overline{SHDN})}$= 0 V, $V_{(OUT)}$ = 24 V, Sinking		7.27	102	
		$V_{(IN)}$ = – 57V, $V_{(\overline{SHDN})}$= 0V, $V_{(OUT)}$ = 0V, Sinking			168	
	OUT leakage current under output reverse polarity condition	$V_{(IN)}$ = 24 V, $V_{(OUT)}$ = – 24 V, $V_{(\overline{SHDN})}$ = 2 V, TP26624, TPS26625 Only		450		
$V_{(REVTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, falling		–71	–54	–40	mV
$V_{(FWDTH)}$	$V_{(IN)}$ – $V_{(OUT)}$ threshold for reverse protection comparator, rising		1.4	15	30	mV
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull-Down Resistance	$V_{(OVP)}$ = 2 V, $I_{(\overline{FLT})}$ = 5mA sinking	45	82.3	145	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input Leakage Current	0 V ≤ $V_{(\overline{FLT})}$ ≤ 57 V	–100	0	100	nA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD Threshold, rising			155		°C
$T_{(TSDhyst)}$	TSD Hysteresis			10		°C
	Thermal Fault (Latch or Auto-Retry)	TPS26620, TPS26622, TPS26624		Latch		
		TPS26621, TPS26623, TPS26625		Auto–retry		

7.6 Timing Requirements

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{FLT}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
IN and UVLO INPUT					

Timing Requirements (continued)

–40°C ≤ T_A = T_J ≤ +125°C, $V_{(IN)}$ = 24 V, $V_{(\overline{SHDN})}$ = 2 V, $R_{(ILIM)}$ = 267 kΩ, $\overline{\text{FLT}}$ = OPEN, $C_{(OUT)}$ = 1 µF, $C_{(dVdT)}$ = OPEN. (All voltages referenced to GND, (unless otherwise noted))

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
UVLO_$t_{ON(dly)}$	UVLO Turnon Delay	UVLO ↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ = Open		51		µs
		UVLO↑ (100 mV above $V_{(UVLOR)}$) to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ > 4.7 nF		51 + 27.4 x $C_{(dVdT)}$		µs
UVLO_$t_{off(dly)}$	UVLO Turnoff delay	UVLO↓ (100 mV below $V_{(UVLOF)}$) to $\overline{\text{FLT}}$↓		6.14		µs
SHUTDOWN CONTROL INPUT ($\overline{\text{SHDN}}$)						
$t_{SD(dly)}$	SHUTDOWN exit delay	$\overline{\text{SHDN}}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ = Open		156		µs
		$\overline{\text{SHDN}}$↑ to $V_{(OUT)}$ = 100 mV, $C_{(dVdT)}$ > 4.7 nF		156 + 27.4 x $C_{(dVdT)}$		µs
	SHUTDOWN entry delay	$\overline{\text{SHDN}}$↓ (below SHUTF) to $\overline{\text{FLT}}$↓		6.83		µs
OVER VOLTAGE PROTECTION INPUT (OVP)						
$t_{OVP(dly)}$	OVP Exit delay	OVP↓ (20 mV below $V_{(OVPF)}$) to $V_{(OUT)}$ = 100 mV, TPS26620/21/24/25 Only		77		µs
	OVP Disable delay	OVP↑ (20mV above $V_{(OVPR)}$) to $\overline{\text{FLT}}$↓ , TPS26620/21/24/25 Only		4.84		µs
CURRENT LIMIT						
$t_{CL(dly)}$	Maximum duration in current limit	$I_{(ILIM)}$ < $I_{(OUT)}$ < $I_{(FASTRIP)}$, $V_{(IN)}$ – $V_{(OUT)}$ < 2.6 V		512		ms
$t_{FASTTRIP(dly)}$	Fast-Trip Comparator Delay	$I_{(OUT)}$ > $I_{(FASTRIP)}$, $V_{(IN)}$ – $V_{(OUT)}$ = 2 V		1.5		µs
		$I_{(OUT)}$ > $I_{(FASTRIP)}$, 4.5 V < $V_{(IN)}$ ≤ 6 V, $V_{(IN)}$ – $V_{(OUT)}$ ≥ 2.6 V		1.4		µs
		$I_{(OUT)}$ > $I_{(FASTRIP)}$, 6 V < $V_{(IN)}$ ≤ 57 V, $V_{(IN)}$ – $V_{(OUT)}$ ≥ 2.6 V		220		ns
REVERSE PROTECTION COMPARATOR						
$t_{REV(dly)}$	Reverse Protection Comparator Delay	($V_{(IN)}$ – $V_{(OUT)}$) ↓ (10 mV overdrive below $V_{(REVTH)}$) to internal FET turn OFF		15		µs
		($V_{(IN)}$ – $V_{(OUT)}$) ↓ (1 V overdrive below $V_{(REVTH)}$) to internal FET turn OFF		3.71		
		($V_{(IN)}$ – $V_{(OUT)}$) ≤ – 2.6 V to internal FET turn OFF		0.31		
		($V_{(IN)}$ – $V_{(OUT)}$) ↓ (150 mV overdrive below $V_{(REVTH)}$) to $\overline{\text{FLT}}$↓		45		
$t_{FWD(dly)}$		($V_{(IN)}$ – $V_{(OUT)}$) ↑ (100 mV overdrive above $V_{(FWDTH)}$) to $\overline{\text{FLT}}$↑		63		
THERMAL SHUTDOWN						
Retry Delay in TSD				512		ms
OUTPUT RAMP CONTROL (dVdT)						
t_{dVdT}	Output Ramp Time	$\overline{\text{SHDN}}$ ↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = 22 nF		11		ms
		$\overline{\text{SHDN}}$ ↑ to $V_{(OUT)}$ = 23.9 V, with $C_{(dVdT)}$ = open		0.664		
FAULT FLAG ($\overline{\text{FLT}}$)						
t_{PGOODF}	PGOOD Delay	Falling edge		875		µs
t_{PGOODR}		Rising edge, $C_{(dVdT)}$ = Open		1.4		ms
		Rising edge, $C_{(dVdT)}$ > 4.7 nF		750 + 573 x $C_{(dVdT)}$		µs

7.7 Typical Characteristics

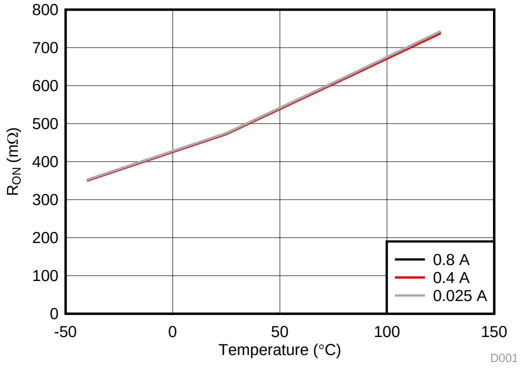


Figure 1. On-Resistance vs Temperature Across Load Current

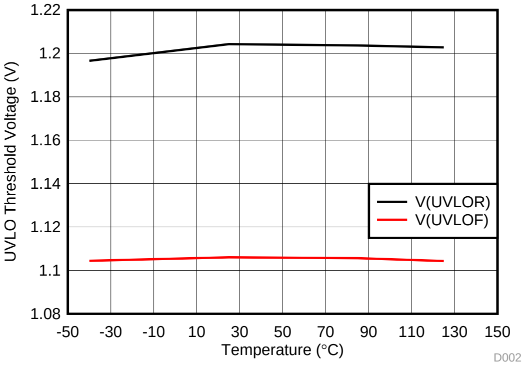


Figure 2. UVLO Threshold Voltage vs Temperature

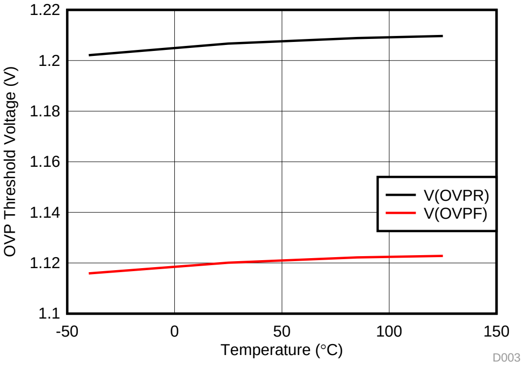


Figure 3. OVP Threshold Voltage vs Temperature

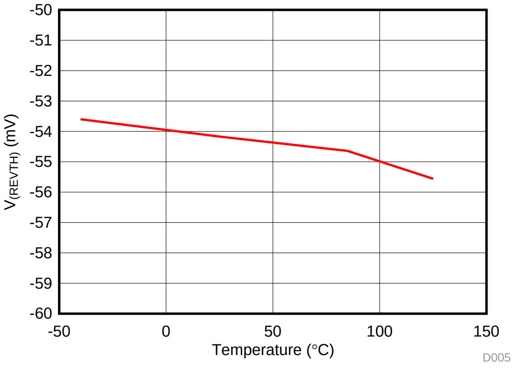


Figure 4. Reverse Voltage Threshold vs Temperature

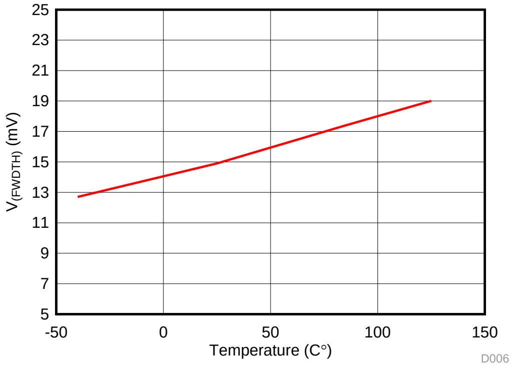


Figure 5. $V_{(FWDTH)}$ vs Temperature

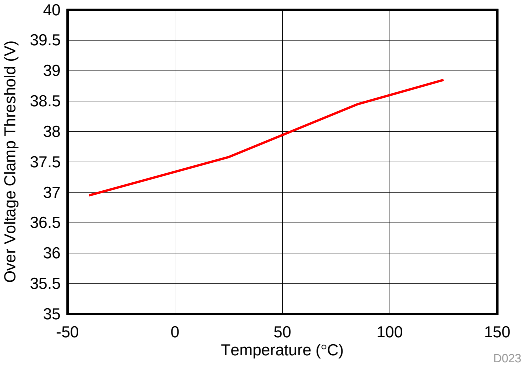


Figure 6. Overvoltage Clamp Threshold vs Temperature

Typical Characteristics (continued)

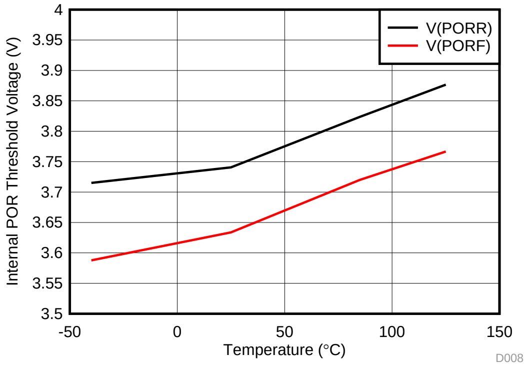


Figure 7. Internal POR Threshold Voltage vs Temperature

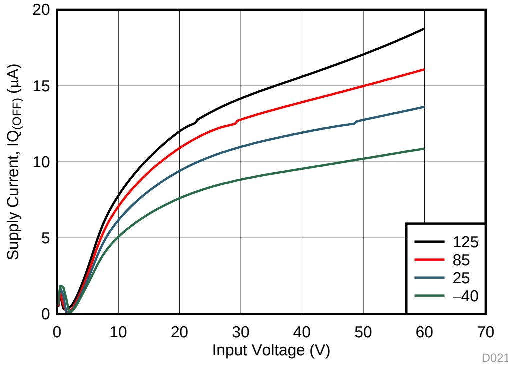


Figure 8. Input Supply Current vs Supply Voltage in Shutdown

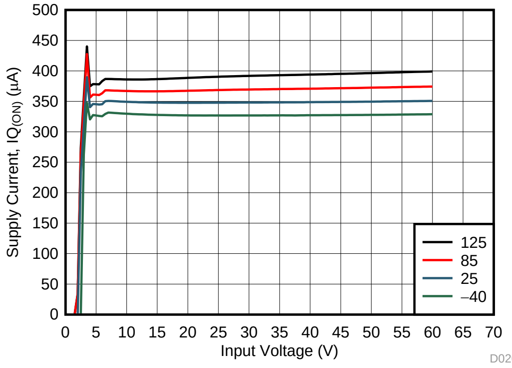
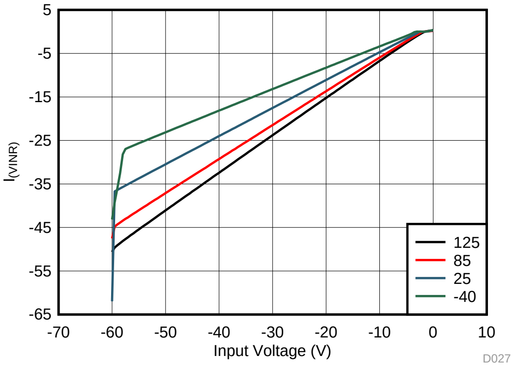


Figure 9. Input Supply Current vs Supply Voltage During Normal Operation



$V_{(OUT)} = 0$ V

Figure 10. Input Supply Current vs Reverse Supply Voltage, $–V_{(IN)}$

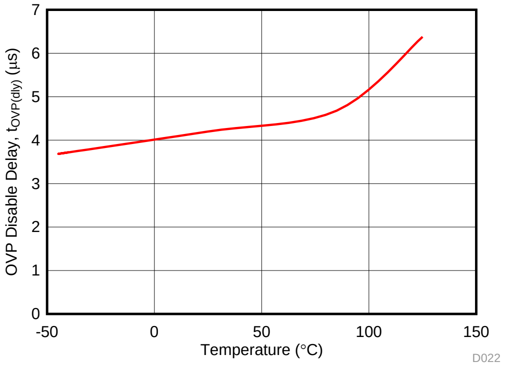


Figure 11. OVP Disable Delay vs Temperature

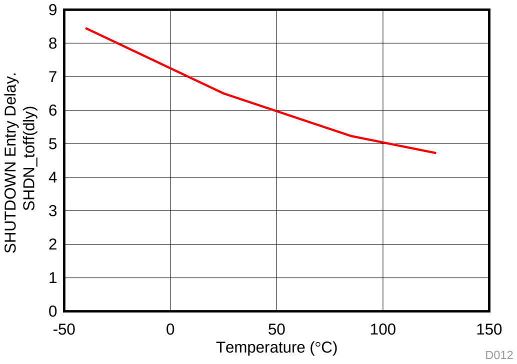


Figure 12. Shutdown Entry Delay vs Temperature

Typical Characteristics (continued)

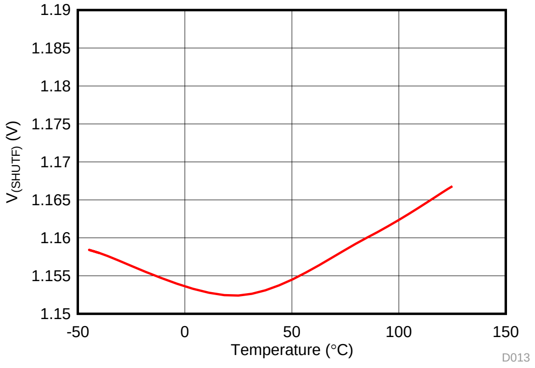


Figure 13. Shutdown Threshold Voltage Shutdown vs Temperature

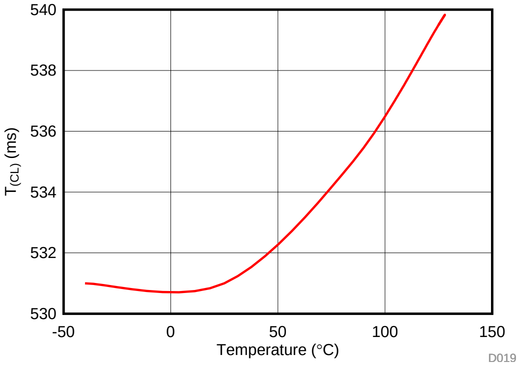


Figure 14. Max Duration in Current Limiting $t_{(CL)}$ vs Temperature

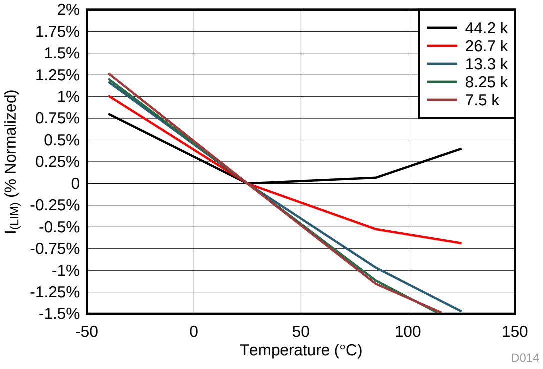


Figure 15. Current Limit (% Normalized) vs Temperature

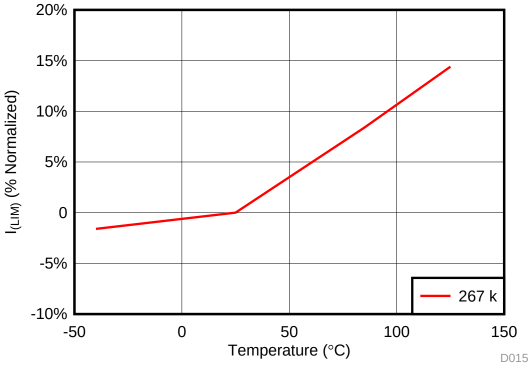


Figure 16. Current Limit (% Normalized) vs Temperature

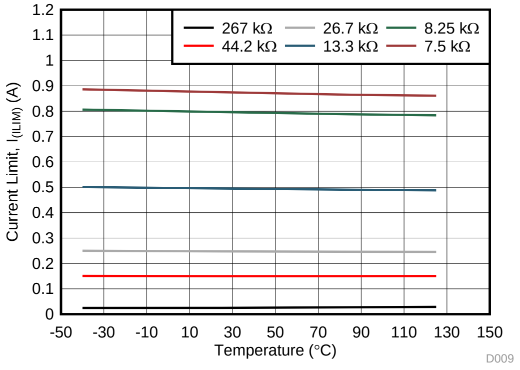


Figure 17. Over Load Current Limit vs Temperature

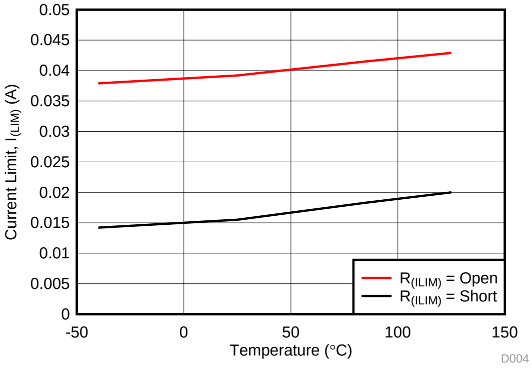


Figure 18. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature

Typical Characteristics (continued)

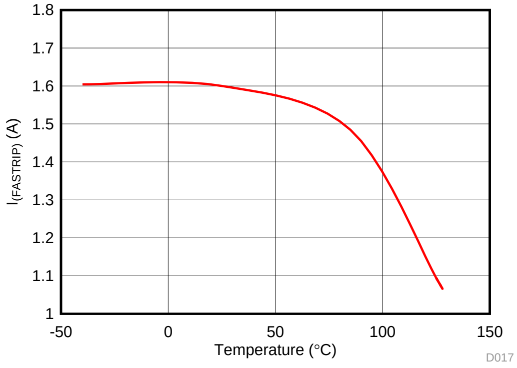


Figure 19. Fast-trip Comparator Threshold $I_{(FASTTRIP)}$ vs Temperature Threshold

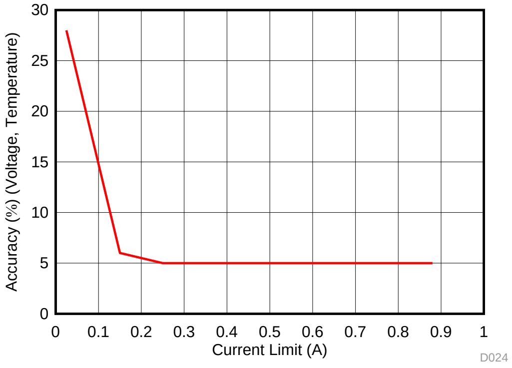


Figure 20. Current Limit Accuracy vs Current Limit, $I_{(OL)}$

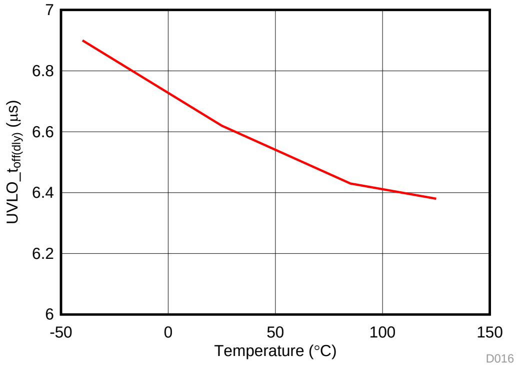


Figure 21. UVLO Turnoff Delay vs Temperature

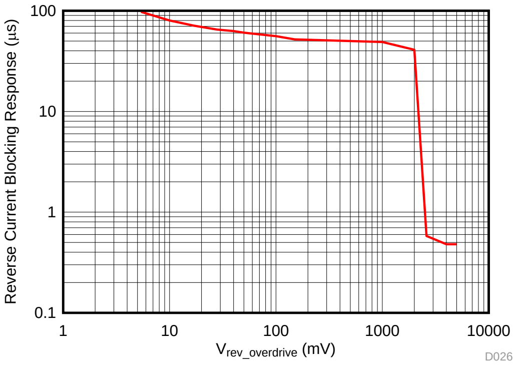
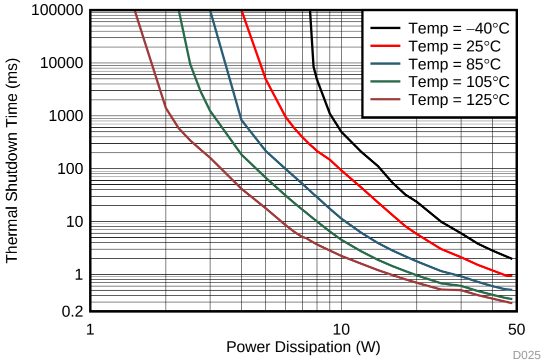
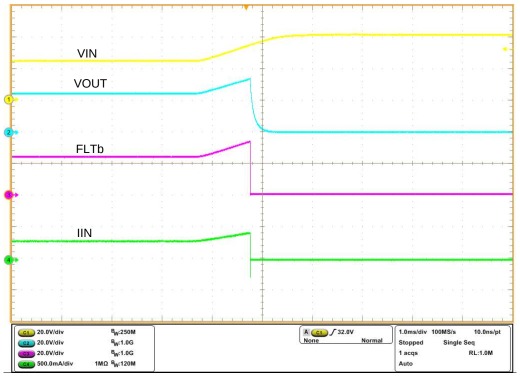


Figure 22. Reverse Current Blocking Response Time vs Reverse Comparator Overdrive Voltage



Taken on 2-Layer board, 2 oz.(0.08-mm thick) with RTN plane area: 0.8 cm^2 (Top) and 4.5 cm^2 (Bottom)

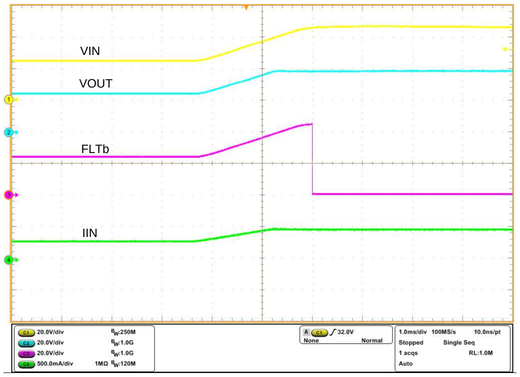
Figure 23. Thermal Shutdown Time vs Power Dissipation



R_{ILIM} = 7.5 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 80 Ω
OVP setting at 33 V

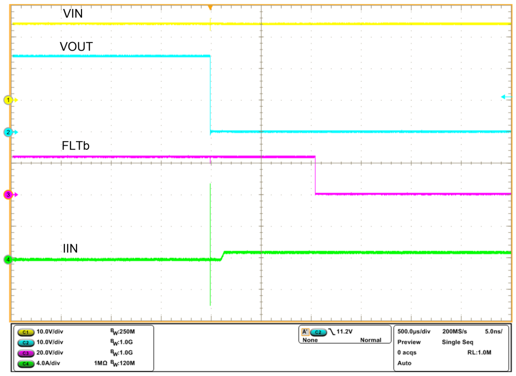
Figure 24. OVP Overvoltage Cut-Off Response

Typical Characteristics (continued)



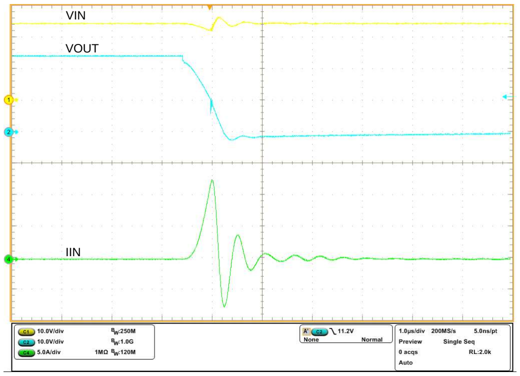
R_{ILIM} = 7.5 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 80 Ω

Figure 25. OV Clamp Response (TPS26602 Only)



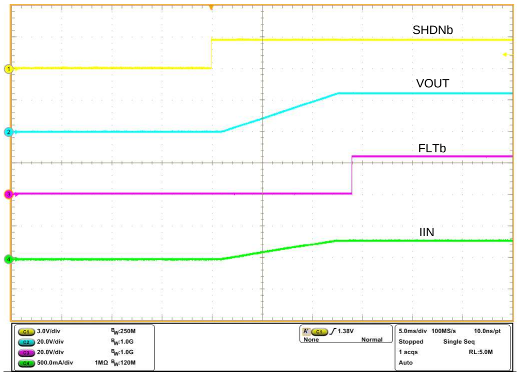
R_{ILIM} = 7.5 kΩ R_{FLTb} = 100 kΩ

Figure 26. Hot-Short: Fast Trip Response and Current Regulation



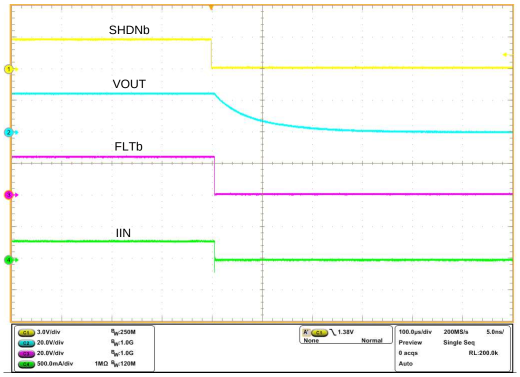
R_{ILIM} = 7.5 kΩ

Figure 27. Hot-Short: Fast Trip Response (Zoomed)



R_{ILIM} = 7.5 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 80 Ω

Figure 28. Turnon Control With $\overline{\text{SHDN}}$



R_{ILIM} = 7.5 kΩ R_{FLTb} = 100 kΩ R_{LOAD} = 80 Ω

Figure 29. Turnoff Control With $\overline{\text{SHDN}}$

8 Parameter Measurement Information

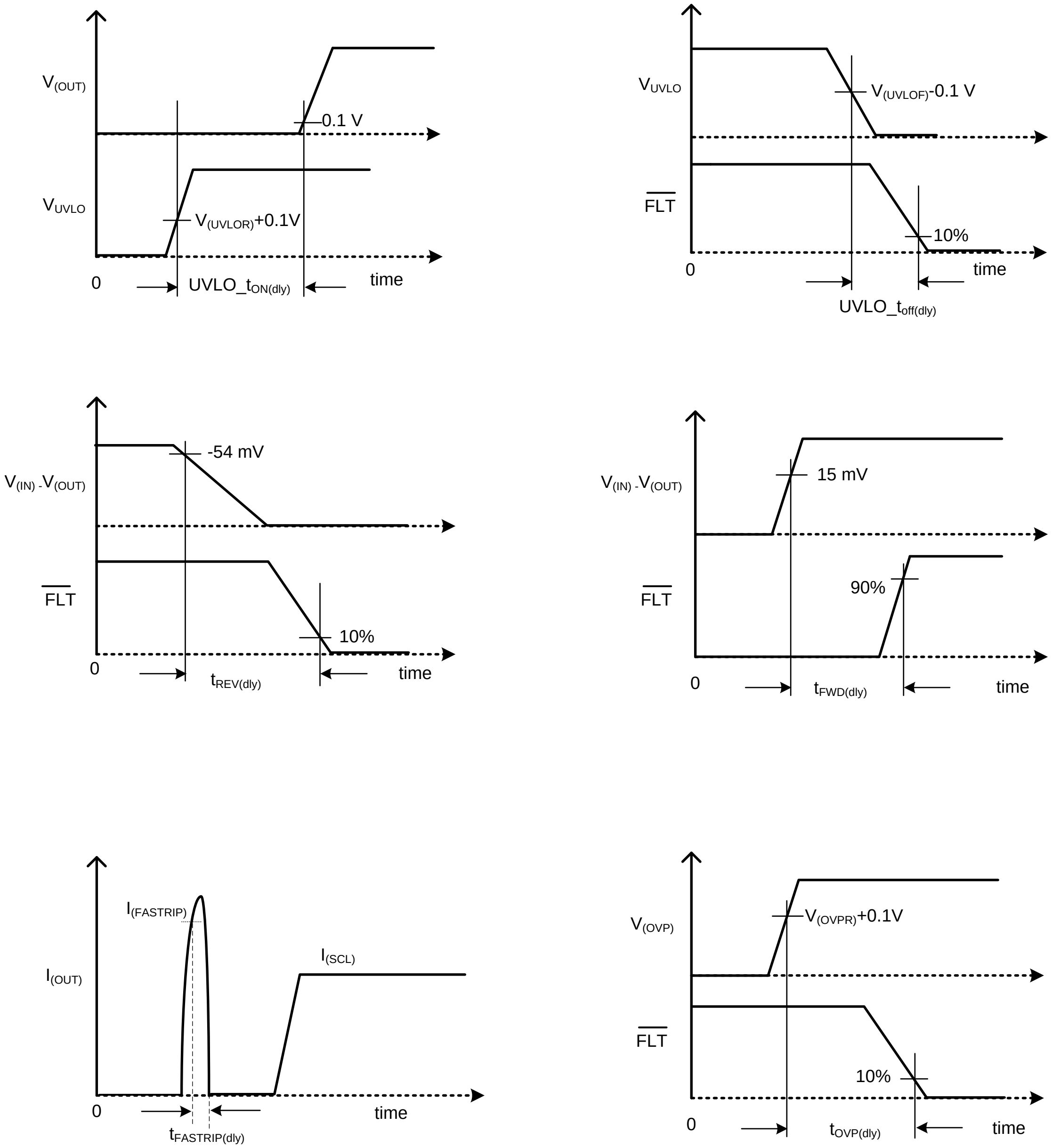


Figure 30. Timing Waveforms

9 Detailed Description

9.1 Overview

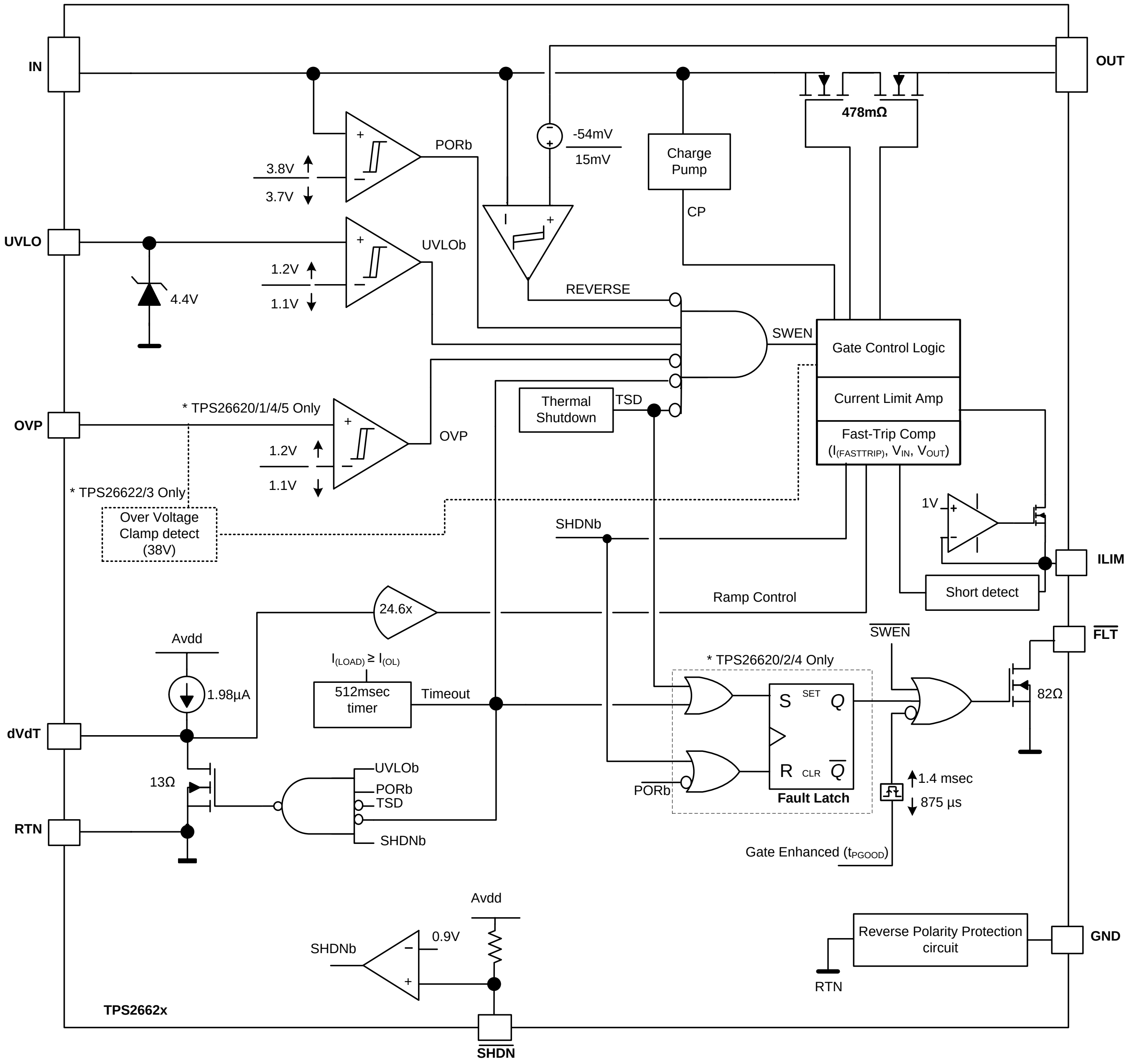
The TPS2662x is a family of high voltage industrial eFuses with integrated back-to-back MOSFETs and enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 4.5 V to 57 V. The device can withstand ±60 V positive and negative supply voltages without damage. The device feature fully integrated reverse polarity protection and require zero additional power components. For hot-pluggable boards, the device provides hot-swap power management with in-rush current control. Load, source and device protections are provided with many programmable features including overcurrent, overvoltage, undervoltage. The precision overcurrent limit (±5% at 880 mA) helps to minimize over design of the input power supply, while the fast response short circuit protection 220 ns (typical) immediately isolates the faulty load from the input supply when a short circuit is detected.

The internal robust protection control blocks of the TPS2662x along with its ±60 V rating helps to simplify the system designs for the surge compliance ensuring complete protection of the load and the device. TPS2662x devices are immune to noise tests like Electrical Fast Transients that are common in industrial applications and simplifies the system design that require criterion-A performance during this test.

The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault signal for the downstream system. The TPS2662x monitor functions threshold accuracy of ±3% ensures tight supervision of the supply bus, eliminating the need for a separate supply voltage supervisor chip.

The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Undervoltage Lockout (UVLO)

When the voltage at UVLO pin falls below $V_{(UVLOF)}$ during input power fail or input undervoltage fault, the internal FET quickly turns off and $\overline{\text{FLT}}$ is asserted. The UVLO comparator has a hysteresis of 100 mV. To set the input UVLO threshold, connect a resistor divider network from IN supply to UVLO terminal to RTN as shown in Figure 31.

Feature Description (continued)

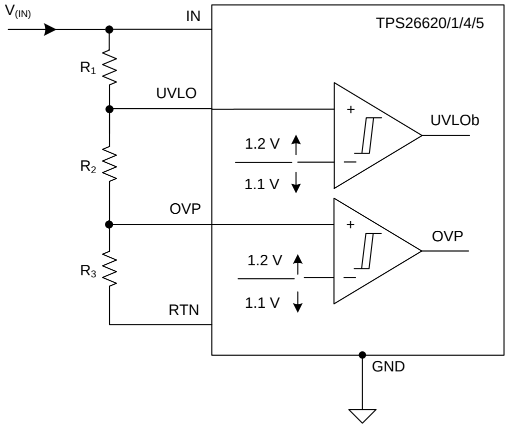


Figure 31. UVLO and OVP Thresholds Set by R_1, R_2 and R_3

If the Undervoltage Lockout function is not needed, the UVLO terminal must be connected to the IN terminal with a 1 MΩ resistor. UVLO pin is 5 V rated and this resistor limits the UVLO pin current to < 60 µA. The UVLO terminal must not be left floating.

9.3.2 Overvoltage Protection (OVP)

The TPS2662x family incorporate circuitry to protect the system during overvoltage conditions. The TPS26620, TPS26621, TPS26624 and TPS26625 feature overvoltage cut off functionality. A voltage more than $V_{(OVPR)}$ on OVP pin turns off the internal FET and protects the downstream load. To program the OVP threshold externally, connect a resistor divider from IN supply to OVP terminal to RTN as shown in Figure 31. If the over voltage feature is not to be used then connect OVP terminal to RTN directly.

The TPS26622 and TPS26623 features an internally fixed 38 V overvoltage clamp (V_{OVC}) functionality. The OVP terminal of these devices must be connected to the RTN terminal directly. These devices clamp the output voltage to V_{OVC}, when the input voltage exceeds 38 V. During the output voltage clamp operation, the power dissipation in the internal MOSFET is $P_D = (V_{IN} – V_{OVC}) \times I_{OUT}$. Excess power dissipation for prolonged period can make the device to enter into thermal shutdown. Figure 25 illustrates the overvoltage clamp functionality.

9.3.3 Hot Plug-In and In-Rush Current Control

The devices are designed to control the inrush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane’s supply voltage and prevents unintended resets of the system power. The controlled start-up also helps to eliminate conductive and radiative interferences. An external capacitor connected from the dVdT pin to RTN defines the slew rate of the output voltage at power-on as shown in Figure 32 and Figure 33.

Feature Description (continued)

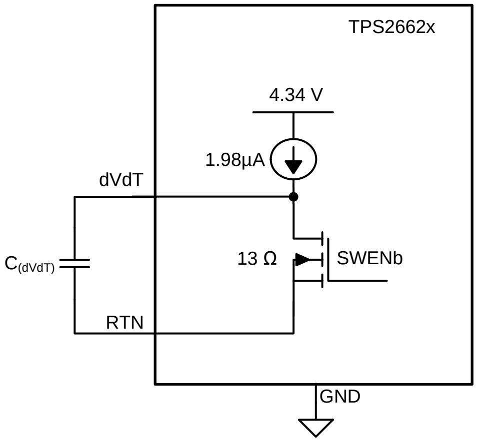


Figure 32. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

The dVdT pin can be left floating to obtain a predetermined slew rate (t_{dVdT}) on the output. When the terminal is left floating, the devices set an internal output voltage ramp rate of 24V/660 µs. A capacitor can be connected from dVdT pin to RTN to program the output voltage slew rate slower than 24V/660 µs. Use Equation 1 and Equation 2 to calculate the external $C_{(dVdT)}$ capacitance.

Equation 1 governs slew rate at start-up.

$$I_{(dVdT)} = \left(\frac{C_{(dVdT)}}{Gain_{(dVdT)}}\right) \times \left(\frac{dV_{(OUT)}}{dt}\right)$$

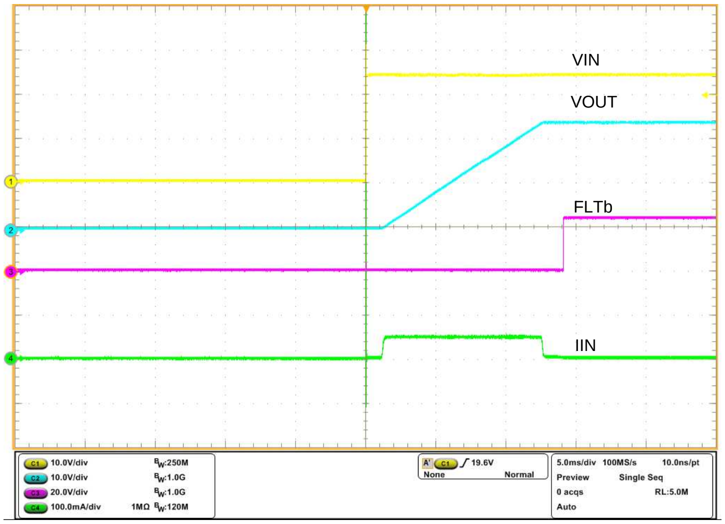
where

- $I_{(dVdT)}$ = 1.98 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$ = Desired output slew rate
- $Gain_{(dVdT)}$ = dVdT to V_{OUT} gain = 24.6 (1)

The total ramp time (t_{dVdT}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using Equation 2.

$$t_{dVdT} = 20.5 \times 10^3 \times V_{(IN)} \times C_{(dVdT)} \quad (2)$$

Feature Description (continued)



C_{dVdT} = 22 nF C_{OUT} = 22 µF R_{ILIM} = 7.5 kΩ

Figure 33. Hot Plug In and Inrush Current Control at 24-V Input

9.3.4 Reverse Polarity Protection

9.3.4.1 Input Side Reverse Polarity Protection

The TPS26620, TPS26621, TPS26622 and TPS26623 eFuses feature fully integrated input side reverse polarity protection. The internal FETs of the eFuse turn OFF during the input reverse polarity event and protect the downstream loads from negative supply voltages that can appear due to field mis-wiring on the input power terminals. Figure 34 illustrates the reverse input polarity protection functionality.

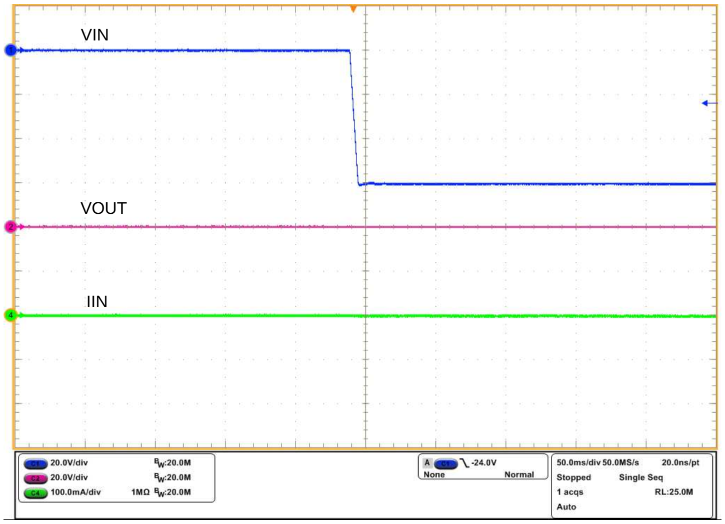


Figure 34. Reverse Input Supply Protection at –60 V

Feature Description (continued)

9.3.4.2 Output Side Reverse Polarity Protection

TheTPS26624 and TPS26625 eFuses feature fully integrated input as well as output reverse polarity protection. The internal FETs of the eFuse turn OFF during the output reverse polarity event and protects the upstream circuits from negative voltage that can appear at the output of the eFuse due to field miswiring at the output side with an external isolated power supplies. Figure 35 illustrates the performance during output side reverse polarity event with $V_{(IN)}$ un-powered and Figure 36 illustrates the performance with $V_{(IN)}$ powered. Figure 37 illustrates the output recovery performance after the reverse polarity is removed.

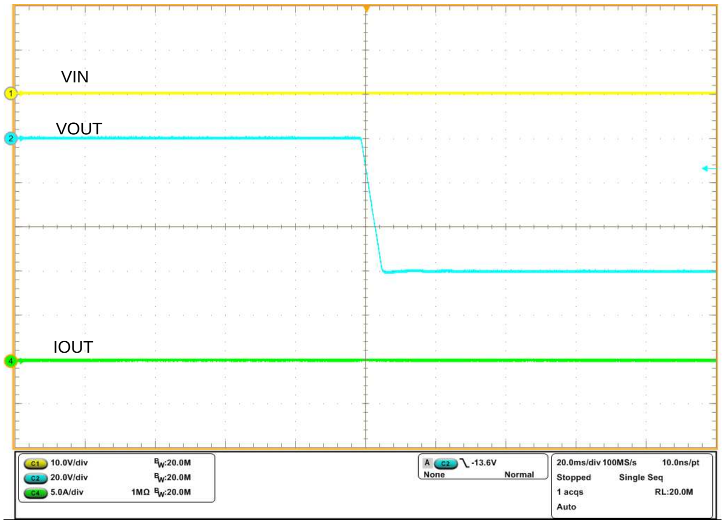


Figure 35. Reverse Output Polarity Protection with –60 V at OUT and VIN = 0 V

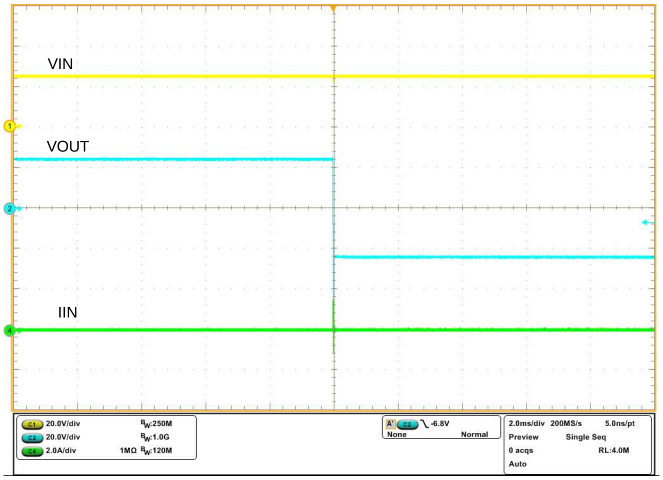


Figure 36. Reverse Output Polarity Protection with –24 V at OUT and 24 V at IN

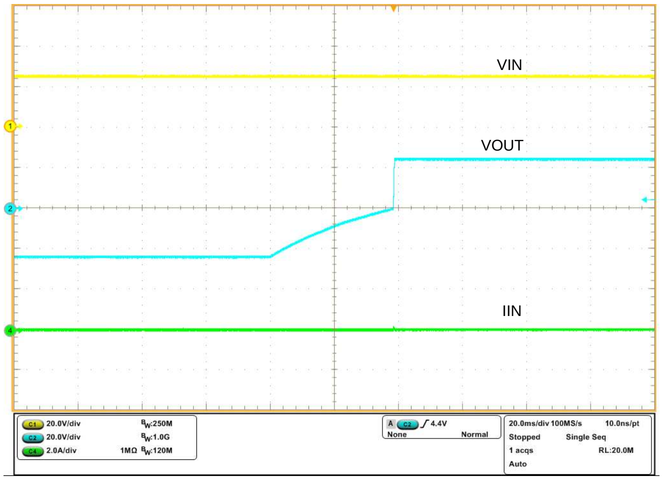


Figure 37. Response During Coming Out of Output Reverse Polarity Fault Condition

9.3.5 Overload and Short Circuit Protection

The device monitors the load current by sensing the voltage across the internal sense resistor. The FET current is monitored during start-up and normal operation.

Feature Description (continued)

9.3.5.1 Overload Protection

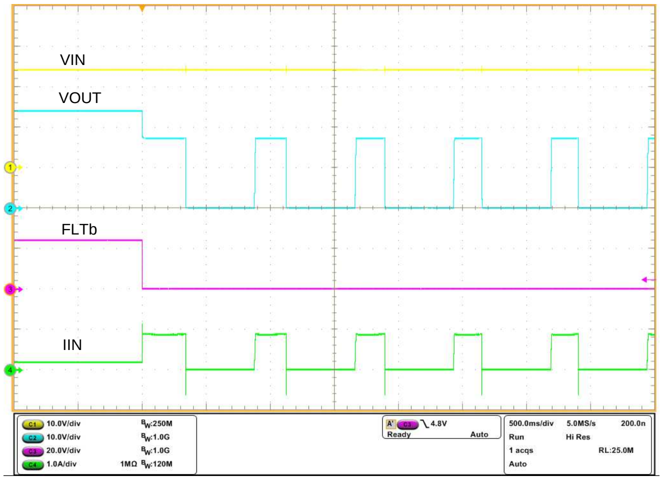
Connect a resistor across ILIM to RTN to program the over load current limit $I_{(OL)}$. During over load conditions the device regulates the current through it at $I_{(OL)}$ programmed by the $R_{(ILIM)}$ resistor as shown in Equation 3 for a maximum duration of $t_{CL(dly)}$.

$$I_{OL} = \frac{6.636}{R_{ILIM}}$$

where

- $I_{(OL)}$ is the overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ (3)

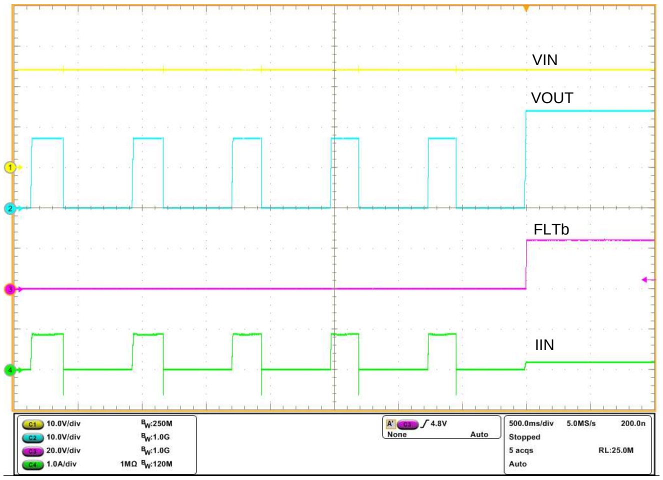
During the current limit operation the output voltage droops and this may cause the device to hit the thermal shutdown threshold $T_{(TSD)}$ before $t_{CL(dly)}$ time. Once the thermal shutdown threshold is hit or $t_{CL(dly)}$ is elapsed, the internal FETs of TPS2662x will turn OFF. FETs in TPS26620, TPS26622 and TPS26624 remain OFF and latched. To reset the latch, cycle the $\overline{SHDN}$, UVLO or recycle the V_{IN}. TPS26621, TPS26623 and TPS26625 commences an auto-retry cycle after a retry time of 512 msec. The internal FETs turn back on in dVdT mode after this retry time. If the overload still exists then the device regulates the current at programmed current limit $I_{(OL)}$.



Load transition from 120 Ω to 20 Ω

VIN = 24 V, R_{ILIM} = 7.5 kΩ

Figure 38. Auto-Retry Fault Behavior



Load transition from 20 Ω to 120 Ω

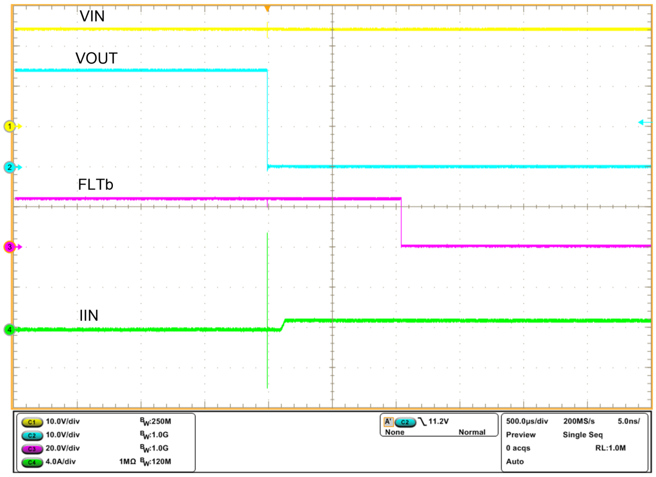
VIN = 24 V, R_{ILIM} = 7.5 kΩ

Figure 39. Response During Coming Out of Overload Fault

9.3.5.2 Short Circuit Protection

During a transient output short circuit event, the current through the device increases rapidly. As the current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator. The fast-trip comparator architecture is designed for fast turn OFF ($t_{FASTTRIP(dly)}$ = 220 ns (typical)) of the internal FET during an output short circuit event. The fast-trip threshold is internally set to $I_{(FASTRIP)}$. The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device turns back on slowly, allowing the current-limit loop to regulate the output current to $I_{(OL)}$. Then the device functions similar to the overload condition. Figure 40 and Figure 41 illustrates the behavior of the system during output short circuit condition.

Feature Description (continued)



VIN = 24 V, R_{ILIM} = 7.5 kΩ

Figure 40. Output Hot Short Functionality at 24-V Input

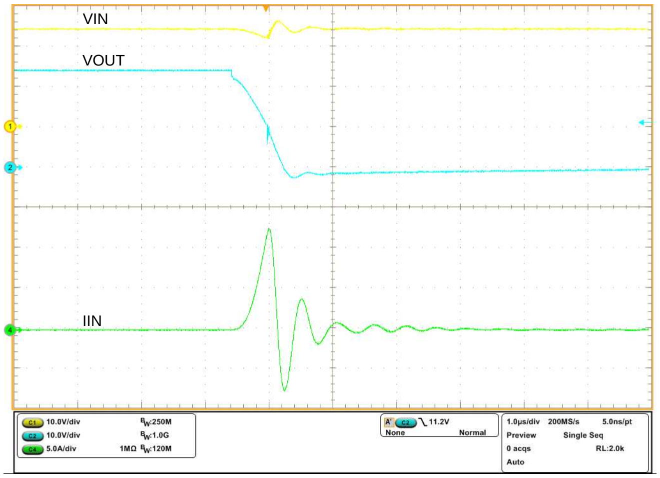
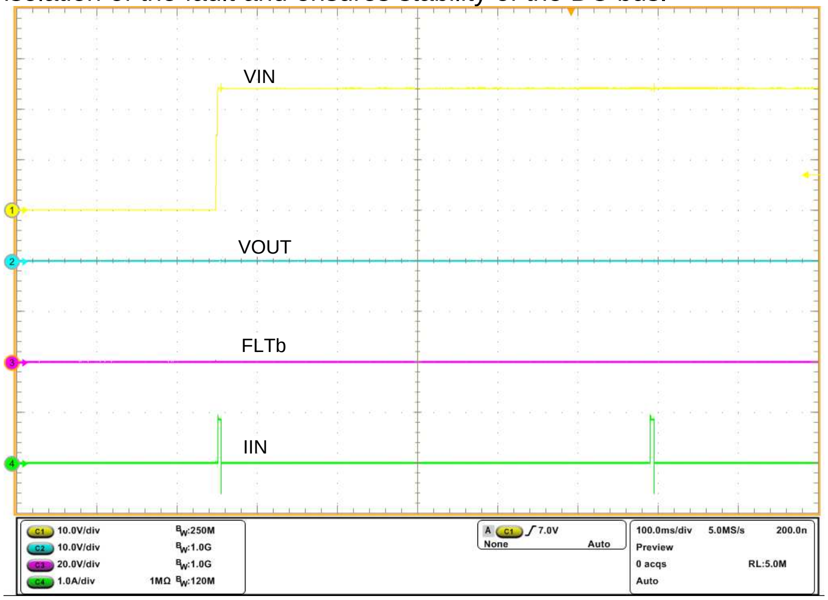


Figure 41. Hot-Short: Fast Trip Response (Zoomed)

The fast-trip comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the differential voltage across $V_{(IN)}$ and $V_{(OUT)}$ once the current through the device exceeds $I_{(FASTTRIP)}$. Higher the voltage difference $V_{(IN)} – V_{(OUT)}$, faster the turn OFF time, $t_{FASTTRIP(dly)}$.

9.3.5.2.1 Start-Up With Short-Circuit On Output

When the device is started with short-circuit on the output, it limits the load current to the current limit $I_{(OL)}$ and functions similar to the overload condition. Figure 42 illustrates the function of the device in this condition. This feature helps in quick isolation of the fault and ensures stability of the DC bus.



VIN = 24 V R_{ILIM} = 7.5 kΩ

Figure 42. Start-Up With Short on Output

Feature Description (continued)

9.3.6 Reverse Current Protection

The device monitors $V_{(IN)}$ and $V_{(OUT)}$ to provide true reverse current blocking when a reverse condition or input power failure condition is detected. The reverse comparator turns OFF the internal FET within 310 ns (typical) as soon as $V_{(IN)} - V_{(OUT)}$ falls below –2.6 V. It turns on within 63 µs (typical) once the differential forward voltage $V_{(IN)} - V_{(OUT)}$ exceeds 115 mV. Figure 43 and Figure 44 illustrates the behavior of the system during input hot short circuit condition.

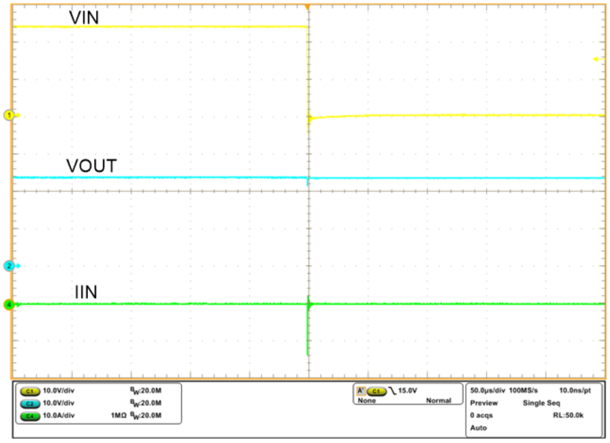


Figure 43. Input Hot Short Functionality at 24-V Supply

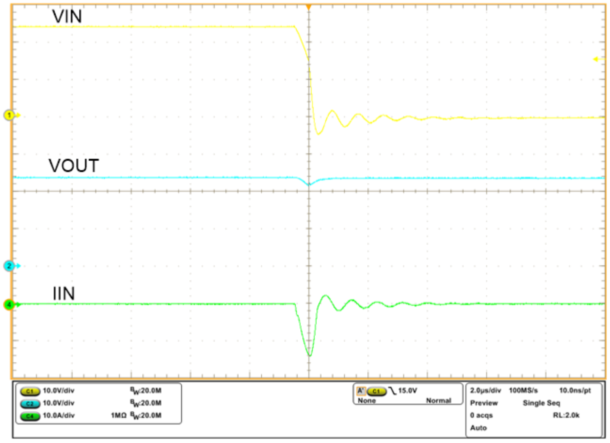


Figure 44. Hot-Short: Fast Trip Response (Zoomed)

The reverse comparator architecture has a supply line noise immunity resulting in a robust performance in noisy environments. This is achieved by controlling the turn OFF time of the internal FET based on the over-drive differential voltage $V_{(IN)} - V_{(OUT)}$ over $V_{(REVTH)}$. Higher the over-drive, faster the turn OFF time, $t_{REV(dly)}$. Figure 22 shows the reverse current blocking response time versus over-drive voltage.

9.3.7 FAULT Response

The $\overline{\text{FLT}}$ open-drain output asserts (active low) under the following conditions:

- Fault events such as undervoltage, overvoltage, over load, reverse current and thermal shutdown conditions
- The device enters low current shutdown mode when $\overline{\text{SHDN}}$ is pulled low
- During start-up when the internal FET GATE is not fully enhanced

The device is designed to eliminate false reporting by using an internal "de-glitch" circuit for fault conditions without the need for an external circuitry.

The $\overline{\text{FLT}}$ signal can also be used as Power Good indicator to the downstream loads like DC-DC converters. An internal Power Good (PGOOD) signal is OR'd with the fault logic. During start-up, when the device is operating in dVdT mode, PGOOD and $\overline{\text{FLT}}$ it remains low and is de-asserted after the dVdT mode is completed and the internal FET is fully enhanced. The PGOOD signal has deglitch time incorporated to ensure that internal FET is fully enhanced before heavy load is applied by the downstream converters. Rising deglitch delay is determined by $t_{PGOOD(degl)}$ = Maximum {(750 + 573× $C_{(dVdT)}$), t_{PGOODR}}, where $C_{(dVdT)}$ is in nF and $t_{PGOOD(degl)}$ is in µs. $\overline{\text{FLT}}$ can be left open or connected to RTN when not used. $V_{(IN)}$ falling below $V_{(PORF)}$ = 3.6 V resets $\overline{\text{FLT}}$.

9.3.8 IN, OUT, RTN, and GND Pins

A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended input operating voltage range is 4.5 to 57 V. $V_{(OUT)}$, in the ON condition, is calculated using Equation 4.

$$V_{(OUT)} = V_{(IN)} - \left(RON \times I_{(OUT)}\right)$$

Feature Description (continued)

Where,

- RON is the total ON resistance of the internal FETs. (4)

GND pin must be connected to the system ground. RTN is the device ground reference for all the internal control blocks. Connect the TPS2662x family support components: $R_{(ILIM)}$, $C_{(dVdT)}$ and resistors for UVLO and OVP with respect to the RTN pin. Internally, the device has reverse input polarity protection block between RTN and the GND terminal. Connecting RTN pin to GND pin disables the reverse polarity protection feature and the TPS2662x gets permanently damaged when operated under this fault event.

9.3.9 Thermal Shutdown

The device has a built-in overtemperature shutdown circuitry designed to protect the internal FETs, if the junction temperature exceeds $T_{(TSD)}$. After the thermal shutdown event, depending upon the mode of fault response, the device either latches off or commences an auto-retry cycle 512 ms after $T_J < [T_{(TSD)} – 13.5°C]$. During the thermal shutdown, the fault pin $\overline{\text{FLT}}$ pulls low to indicate a fault condition.

9.4 Device Functional Modes

9.4.1 Low Current Shutdown Control ($\overline{\text{SHDN}}$)

The internal FETs and the load current can be switched off by pulling the $\overline{\text{SHDN}}$ pin below 0.9 V threshold with a micro-controller GPIO pin or can be controlled remotely with an opto-isolator device as shown in Figure 45 and Figure 46. The device quiescent current reduces to 10 µA (typical) in shutdown state. To assert $\overline{\text{SHDN}}$ low, the pull down must sink at least 10 µA at 400 mV. To enable the device, $\overline{\text{SHDN}}$ must be pulled up to at least 1.8 V. Once the device is enabled, the internal FETs turnon with dVdT mode.

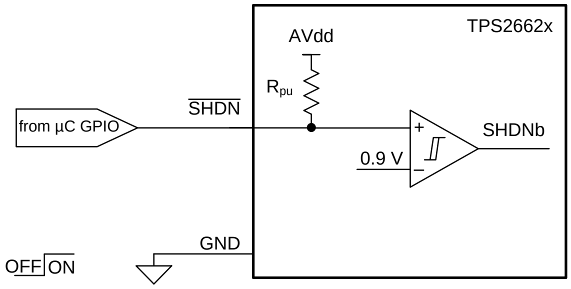


Figure 45. Shutdown Control

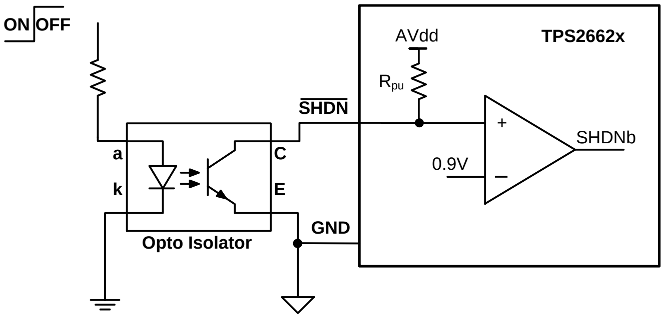


Figure 46. Opto-Isolator Shutdown Control

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPS2662x family is an industrial eFuse, typically used for Hot-Swap and power rail protection applications. It operates from 4.5 V to 57 V with programmable current limit, overvoltage, undervoltage and reverse polarity protections. The device aids in controlling in-rush current and provides robust protection against reverse current and field miss-wiring conditions for systems such as PLC I/O modules and Sensor power supplies. The device also provides robust protection for multiple faults on the system rail.

The *Detailed Design Procedure* section can be used to select component values for the device.

Alternatively, the *WEBENCH®* software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS2662 Design Calculator* is available in the web product folder.

10.2 Typical Application

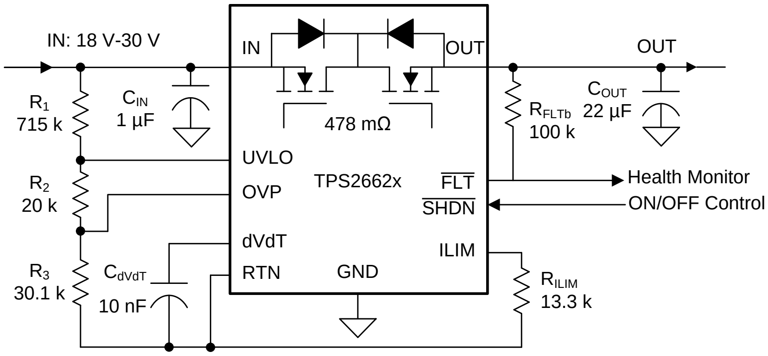


Figure 47. 24-V, 500 mA eFuse Input Protection Circuit for PLC I/O Module

10.2.1 Design Requirements

Table 1 shows the Design Requirements for TPS2662x.

Table 1. Design Requirements

DESIGN PARAMETER		EXAMPLE VALUE
$V_{(IN)}$	Typical input voltage	24 V
$V_{(UV)}$	Undervoltage lockout set point	18 V
$V_{(OV)}$	Overvoltage cutoff set point	30 V
$T_{(SU)}$	Load during start-up	96 Ω
$I_{(LIM)}$	Current limit	500 mA
$C_{(OUT)}$	Load capacitance	22 µF
T_A	Maximum ambient temperature	125ºC

10.2.2 Detailed Design Procedure

10.2.2.1 Step by Step Design Procedure

To begin the design process, the designer must know the following parameters:

- Input operating voltage range
- Maximum output capacitance
- Maximum current limit
- Load during start-up
- Maximum ambient temperature

This design procedure below seeks to control junction temperature of the device in both steady state and start-up conditions by proper selection of the output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.2.2 Programming the Current-Limit Threshold $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 5.

$$R_{ILIM} = \frac{6.636}{I_{LIM}} = 13.27\ k\Omega$$

where

- I_{LIM} = 500 mA (5)

Choose the closest standard 1% resistor value : $R_{(ILIM)}$ = 13.3 kΩ

10.2.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using an external voltage divider network of R_1, R_2 and R_3 connected between IN, UVLO, OVP and RTN pins of the device. The values required for setting the undervoltage and overvoltage are calculated by solving Equation 6 and Equation 7.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \tag{6}$$

$$V_{(UVLOR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \tag{7}$$

For minimizing the input current drawn from the power supply $\{I_{(R123)} = V_{(IN)}/(R_1+R_2+R_3)\}$, it is recommended to use higher value resistance for R_1, R_2 and R_3.

However, the leakage current due to external active components connected at resistor string can add error to these calculations. So, the resistor string current, $I(R_{123})$ must be chosen to be 20 times greater than the leakage current of UVLO and OVP pins.

From the device electrical specifications, $V_{(OVPR)}$ = 1.19 V and $V_{(UVLOR)}$ = 1.19 V. From the design requirements, $V_{(OV)}$ is 30 V and $V_{(UV)}$ is 18 V. To solve the equation, first choose the value of R_3 = 30.1 kΩ and use Equation 6 to solve for (R_1 + R_2) = 728.7 kΩ. Use Equation 7 and value of (R_1 + R_2) to solve for R_2 = 20.05 kΩ and finally R_1= 708.6 kΩ.

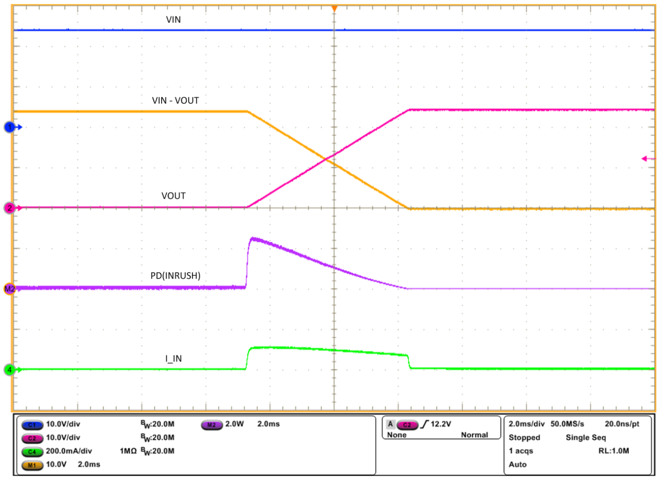
Choose the closest standard 1% resistor values: R_1 = 715 kΩ, R_2 = 20 kΩ, and R_3 = 30.1 kΩ.

10.2.2.4 Setting Output Voltage Ramp Time—(t_{dVdT})

For a successful design, the junction temperature of the device must be kept below the absolute-maximum rating during dynamic (start-up) and steady state conditions. The dynamic power dissipation is often an order magnitude greater than the steady state power dissipation. It is important to determine the right start-up time and the in-rush current limit for the system to avoid thermal shutdown during start-up with and without load. The ramp-up capacitor $C_{(dVdT)}$ is calculated considering the two possible cases:

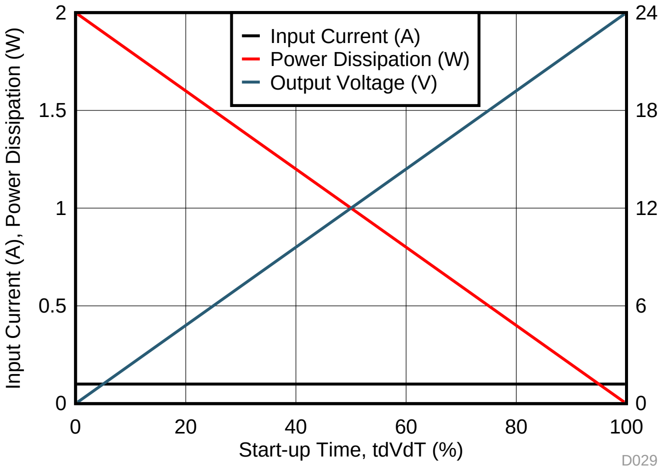
10.2.2.4.1 Case 1: Start-Up Without Load—Only Output Capacitance $C_{(OUT)}$ Draws Current During Start-Up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipation decreases. Typical ramp-up of the output voltage, inrush current and instantaneous power dissipated in the device during start-up are shown in Figure 48. The average power dissipated in the device during start-up is equal to the area of triangular plot (red curve in Figure 49) averaged over t_{dVdT}.



V_{IN} = 24 V C_{dVdT} = 10 nF C_{OUT} = 22 µF

Figure 48. Start-Up Without Load



V_{IN} = 24 V C_{dVdT} = 10 nF C_{OUT} = 22 µF

Figure 49. $P_{D(INRUSH)}$ Due to Inrush Current

The inrush current is determined as shown in Equation 8.

$$I = C \times \frac{dV}{dT} \geq I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{dVdT}} \tag{8}$$

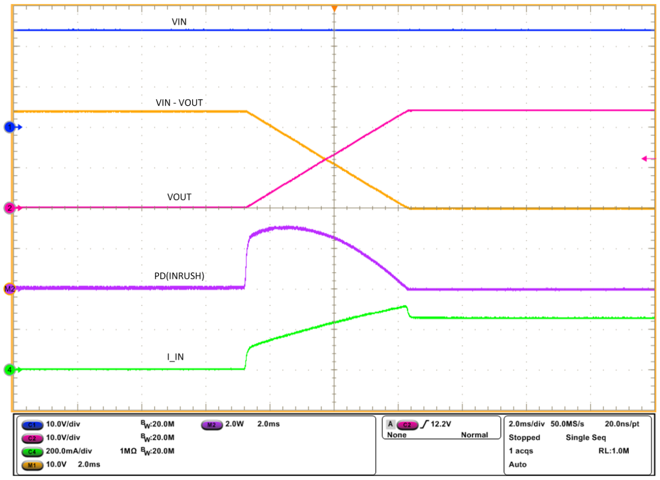
Average power dissipated during start-up is given by Equation 9.

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \tag{9}$$

Equation 9 assumes that the load does not draw any current until the output voltage reaches its final value.

10.2.2.4.2 Case 2: Start-Up With Load —Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-Up

When the load draws current during the turnon sequence, additional power is dissipated in the device. Considering a resistive load RL(SU) during start-up, typical ramp-up of output voltage, load current and the instantaneous power dissipation in the device are shown in Figure 50. Instantaneous power dissipation with respect to time is plotted in Figure 51.



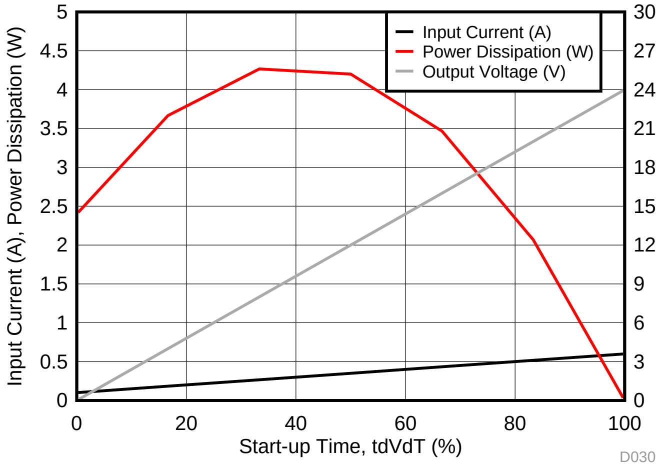
V_{IN} = 24 V

C_{dVdT} = 10 nF

$R_{L(SU)}$ = 96 Ω

C_{OUT} = 22 µF

Figure 50. Start-Up With Load



V_{IN} = 24 V

C_{dVdT} = 10 nF

$R_{L(SU)}$ = 96 Ω

C_{OUT} = 22 µF

Figure 51. $P_{D(INRUSH)}$ Due to Inrush and Load Current

The additional power dissipation during start-up is calculated using

$$P_{D(LOAD)} = \frac{1}{6} \times \frac{V_{(IN)}^2}{R_{L(SU)}} \tag{10}$$

Total power dissipated in the device during start-up is given by

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \tag{11}$$

Total current during start-up is given by .

$$I_{(STARTUP)} = I_{(INRUSH)} + I_{L(t)} \tag{12}$$

For the design example under discussion,

Select the inrush current $I_{(INRUSH)}$ = 0.1 A and t_{dVdT} calculated using Equation 8 is 5.28 ms.

For a given start-up time, C_{dVdT} capacitance value calculated using Equation 2 is 10.7 nF for t_{dVdT} = 5.28 ms and V_{IN} = 24 V.

Choose the closest standard value: 10.0 nF and 16-V capacitor.

The inrush power dissipation due to output capacitor alone is calculated using Equation 9 and it is 1.2 W. Considering the start-up with 96-Ω load, the additional power dissipation calculated using Equation 10 is 1 W. The total device power dissipation during start-up is 2.2 W

The power dissipation with or without load, for a selected start-up time must not exceed the thermal shutdown limits as shown in Figure 52.

From the thermal shutdown limit graph, at T_A = 125°C, thermal shutdown time for 2.2 W is close to 580 ms. It is safe to have a minimum 30% margin to allow for variation of the system parameters such as load, component tolerance, input voltage and layout. Selected 10-nF C_{dVdT} capacitor and 5.28-ms start-up time (t_{dVdT}) are well within the limit for successful start-up with 96 Ω load.

Higher value $C_{(dVdT)}$ capacitor can be selected to further reduce the power dissipation during start-up.

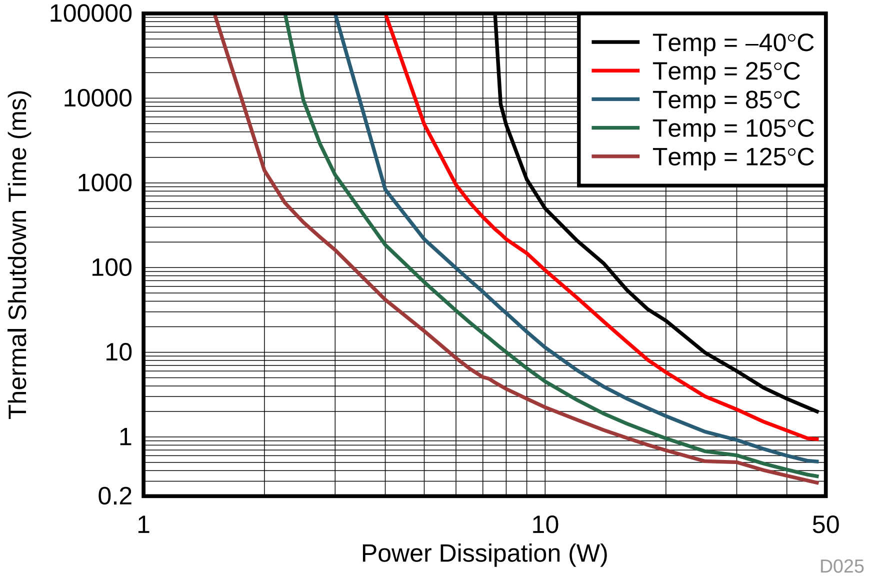


Figure 52. Thermal Shutdown Time vs Power Dissipation

10.2.2.4.3 Support Component Selections - $R_{\overline{FLT}}$ and $C_{(IN)}$

The $R_{\overline{FLT}}$ *Absolute Maximum Ratings* serves as pull-up for the open-drain fault output. The current sink by this pin must not exceed 10 mA (see the *Absolute Maximum Ratings* table). Typical resistance value in the range of 10 kΩ to 100 kΩ is recommended for $R_{\overline{FLT}}$. The C_{IN} is a local bypass capacitor to suppress noise at the input. Typical capacitance value in the range of 0.1 µF to 1 µF is recommended for $C_{(IN)}$.

10.2.3 Application Curves

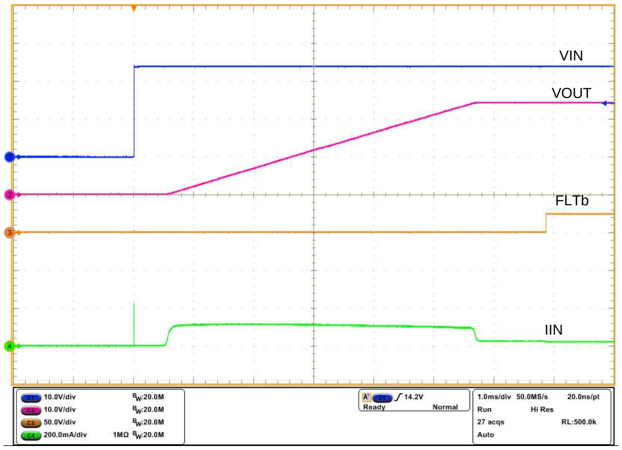


Figure 53. Hot Plug With VIN - No Load

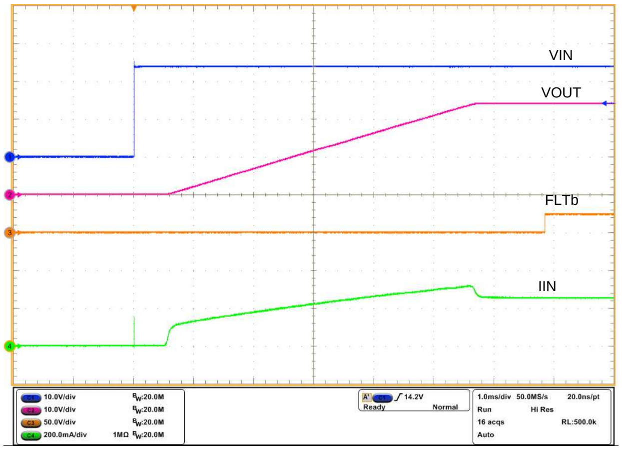


Figure 54. Hot-Plug With VIN - 96-Ω Load

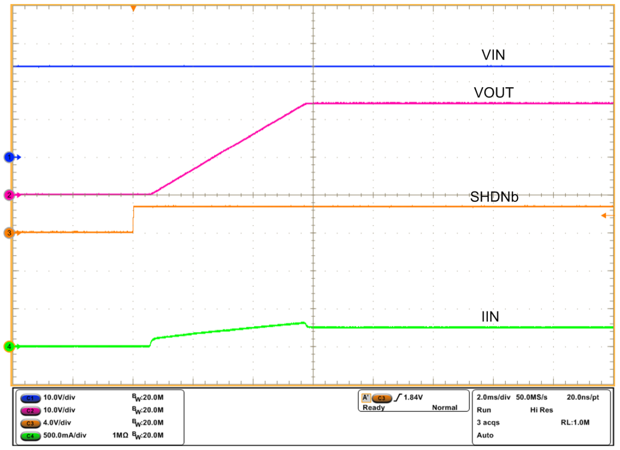


Figure 55. Start-Up With Shutdown Pin - 96-Ω Load

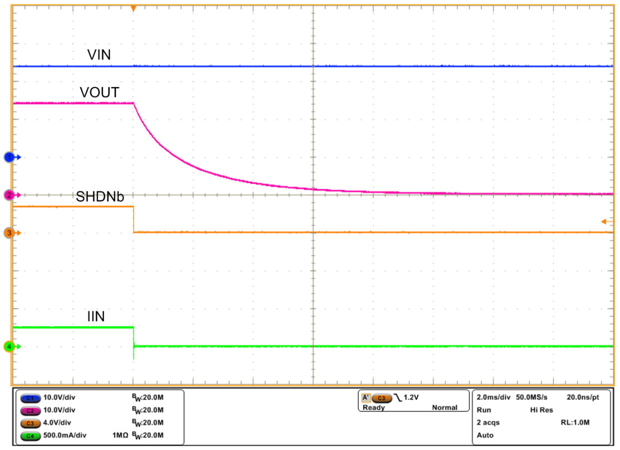


Figure 56. Power Down With Shutdown Pin - 96-Ω Load

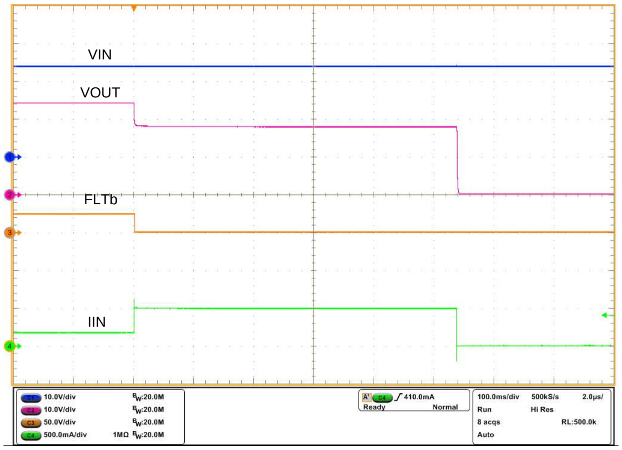


Figure 57. Over Load Response - Load Stepped From 136-Ω to 36-Ω Load

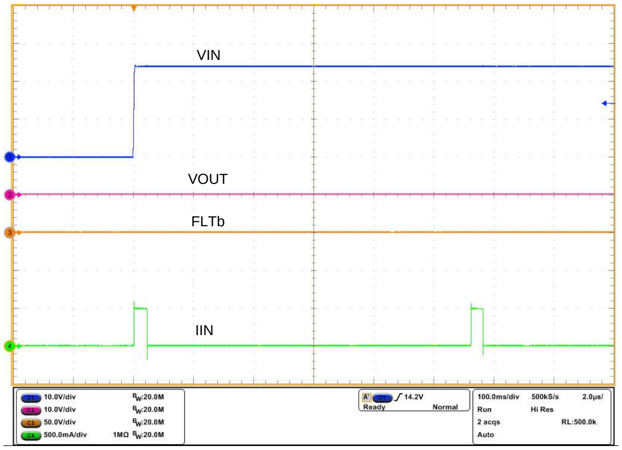


Figure 58. Turn ON with Short Circuit on Output

10.3 System Examples

10.3.1 Field Supply Protection in PLC, DCS I/O Modules

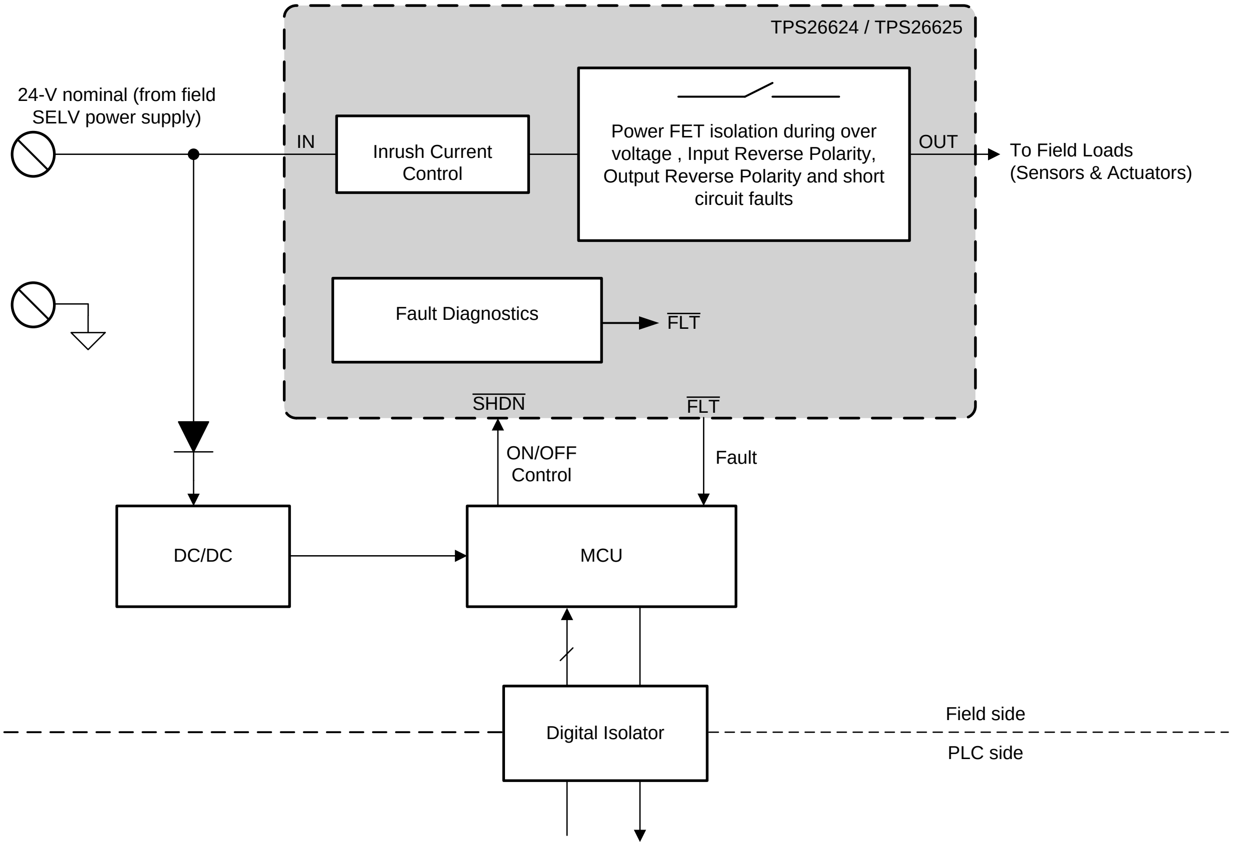


Figure 59. Power Delivery Circuit Block Diagram in I/O Modules

The PLC or Distributed Control System (DCS) I/O modules are often connected to an external field power supply to support higher power requirements of the field loads like sensors and actuators. Power-supply faults or miswiring can damage the loads or cause the loads not to operate correctly. The TPS26624 and TPS26625 can be used as a front end protection circuit to protect and provide stable supply to the field loads. Undervoltage, Overvoltage and input and output side reverse polarity protection features of these devices prevent the loads to experience voltages outside the operating range, which can permanently damage the loads.

Field power supply is often connected to multiple I/O modules that can deliver more current than a single I/O module can handle. Overcurrent protection scheme of the TPS2662x family limits the current from the power supply to the module so that the maximum current does not rise above what the board is designed for. Fast short circuit protection scheme isolates the faulty load from the field supply quickly and prevents the field supply to dip and cause interrupts in the other I/O modules connected to the same field supply. High accurate (±5% at 0.88 A) current limit facilitates more I/O modules to be connected to field supply. Fault indication ($\overline{FLT}$) features facilitate continuous load monitoring.

The TPS26624 and TPS26625 also acts as a smart diode with protection against reverse current during output side miswiring. Reverse current can potentially damage the field power supply and cause the I/O modules to run hot or may cause permanent damage.

If the field power supply is connected in reverse polarity on the input side (which is not unlikely as field power supplies are usually connected with screw terminals), field loads can permanently get damaged due to the reverse voltage. Also, during the installation the field power supply could be miswired on the output side instead of on the input side which could damage the upstream power supply and electronics. The input and output reverse polarity protection feature of the TPS26624 and TPS26625 prevents the reverse voltage to appear at the load side as well as supply side offering complete system protection during field miswiring.

System Examples (continued)

10.3.2 Simple 24-V Power Supply Path Protection

With the TPS2662x, a simple 24-V power supply path protection can be realized using a minimum of four external components as shown in the schematic diagram in Figure 60. The external components required are: a 1Meg Ω $R_{(1)}$ resistor across IN and UVLO pins, a $R_{(ILIM)}$ resistor to program the current limit, $C_{(IN)}$ and $C_{(OUT)}$ capacitors.

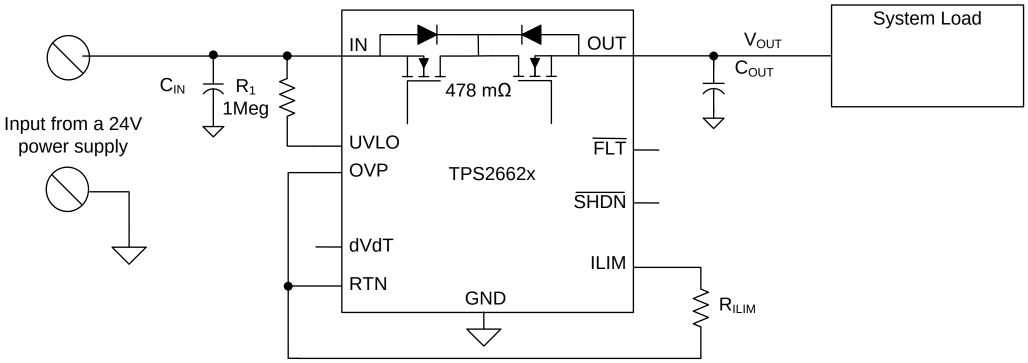


Figure 60. TPS2662x Configured for a Simple 24-V Supply Path Protection

Protection features with this configuration include:

- Load and device protection from reverse input polarity fault down to –60 V
- Upstream supply and device protection from reverse output polarity fault down to –(60 – VIN) V with TPS26624 and TPS26625 variants
- Protection from 60 V from the external SELV supply: Over Voltage Clamp at 38 V with TPS26622 and TPS26623 variants
- Inrush current control with 24V and 660 µs output voltage slew rate
- Reverse Current Blocking
- Accurate current limiting with Auto-Retry with TPS26621, TPS26623, TPS26625 variants
- Accurate current limiting with Latch-off with TPS26620, TPS26622, TPS26624 variants

10.3.3 Power Stealing in Smart Thermostat

The adjustable protection features of the TPS2662x eFuse like the inrush current limiting, over voltage and over current protection simplifies the input power management design in smart thermostats. Refer to the TI Design report, *Power Stage Reference Design for Power Stealing Thermostat* for further information.

10.4 Do's and Don'ts

- Do not connect RTN to GND. Connecting RTN to GND disables the Reverse Polarity protection feature.
- Do connect the TPS2662x support components $R_{(ILIM)}$, $C_{(dVdT)}$, and UVLO, OVP resistors with respect to RTN pin.
- Do connect device PowerPAD to the RTN plane for an enhanced thermal performance.

11 Power Supply Recommendations

The TPS2662x eFuse is designed for the supply voltage range of 4.5 V ≤ V_{IN} ≤ 57 V. If the input supply is located more than a few inches from the device, an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply must be rated higher than the current limit set to avoid voltage droops during overcurrent and short circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) depends on the value of inductance in series to the input or output of the device. These transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include:

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Use of a Schottky diode across the output and GND to absorb negative spikes in the designs with TPS26620, TPS26621, TPS26622, TPS26623 devices and a TVS clamp in the designs withTPS26624 and TPS26625 devices
- A low value ceramic capacitor ($C_{(IN)}$ to approximately 0.1 µF) to absorb the energy and dampen the transients.

The approximate value of input capacitance can be estimated with Equation 13.

$$V_{spike(Absolute)} = V_{(IN)} + I_{(Load)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}}$$

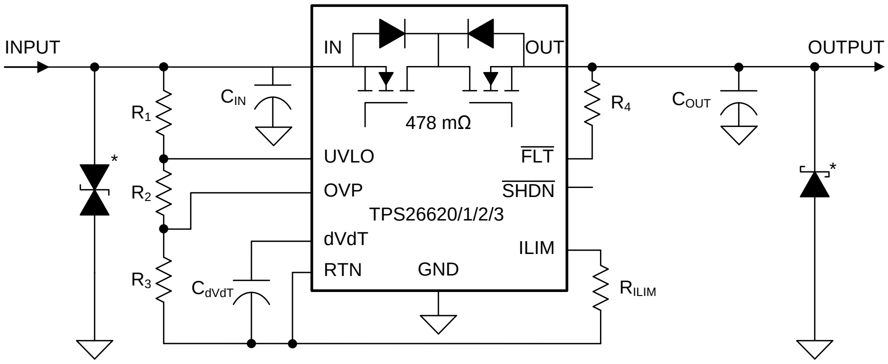
where

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

(13)

Some applications may require additional Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device. These transients can occur during positive and negative surge tests on the supply lines. In such applications it is recommended to place at least 1 µF of input capacitor to limit the falling slew rate of the input voltage within a maximum of 20 V/µs.

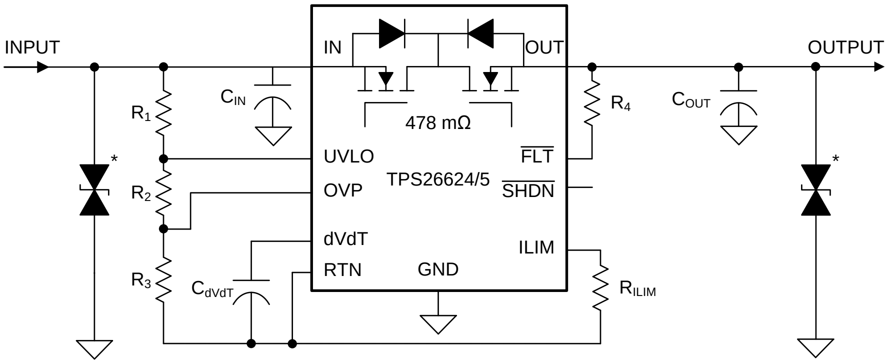
The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 61 and Figure 62.



* Optional components needed for suppression of transients

Figure 61. Circuit Implementation With Optional Protection Components for TPS26620, TPS26621, TPS26622 and TPS26623

Transient Protection (continued)



* Optional components needed for suppression of transients

Figure 62. Circuit Implementation With Optional Protection Components for TPS26624 and TPS26625

12 Layout

12.1 Layout Guidelines

- For all the applications, a 0.1 µF or higher value ceramic decoupling capacitor is recommended between IN terminal and GND.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 63 for a typical PCB layout example.
- High current carrying power path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- RTN, which is the reference ground for the device must be a copper plane or island.
- Locate all the TPS2662x family support components $R_{(ILIM)}$, $C_{(dVdT)}$, UVLO, OVP resistors close to their connection pin. Connect the other end of the component to the RTN with shortest trace length.
- The trace routing for the R_{ILIM} component to the device must be as short as possible to reduce parasitic effects on the current limit and current monitoring accuracy. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it must be physically close to the OUT and GND pins.
- Thermal Considerations: When properly mounted, the PowerPAD package provides significantly greater cooling ability. To operate at rated power, the PowerPAD must be soldered directly to the board RTN plane directly under the device. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications. Designs that do not need reverse input polarity protection can have RTN, GND and PowerPAD connected together. PowerPAD in these designs can be connected to the PCB ground plane.

12.2 Layout Example

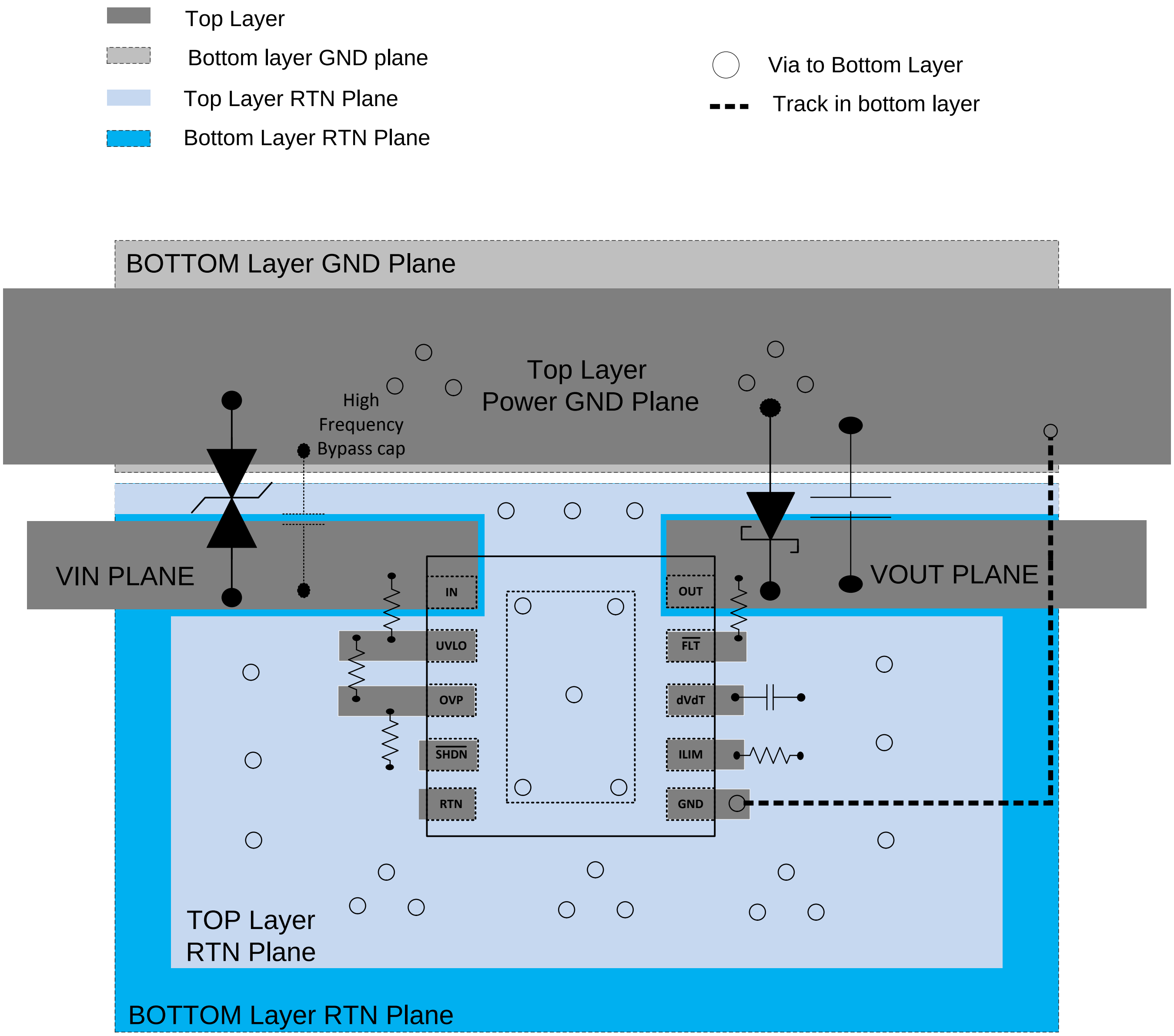


Figure 63. Typical PCB Layout Example With a 2 Layer PCB

13 Device and Documentation Support

13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS26620DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED00	Samples
TPS26620DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED00	Samples
TPS26621DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED01	Samples
TPS26621DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED01	Samples
TPS26622DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED02	Samples
TPS26622DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED02	Samples
TPS26623DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED03	Samples
TPS26623DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED03	Samples
TPS26624DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED04	Samples
TPS26624DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED04	Samples
TPS26625DRCR	ACTIVE	VSON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED05	Samples
TPS26625DRCT	ACTIVE	VSON	DRC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ED05	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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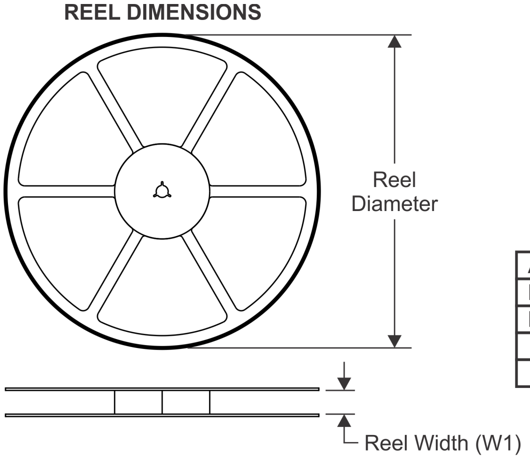
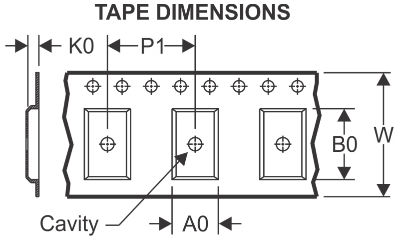
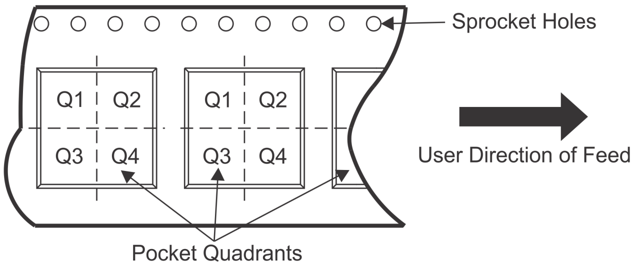
TAPE AND REEL INFORMATION


REEL DIMENSIONS


TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

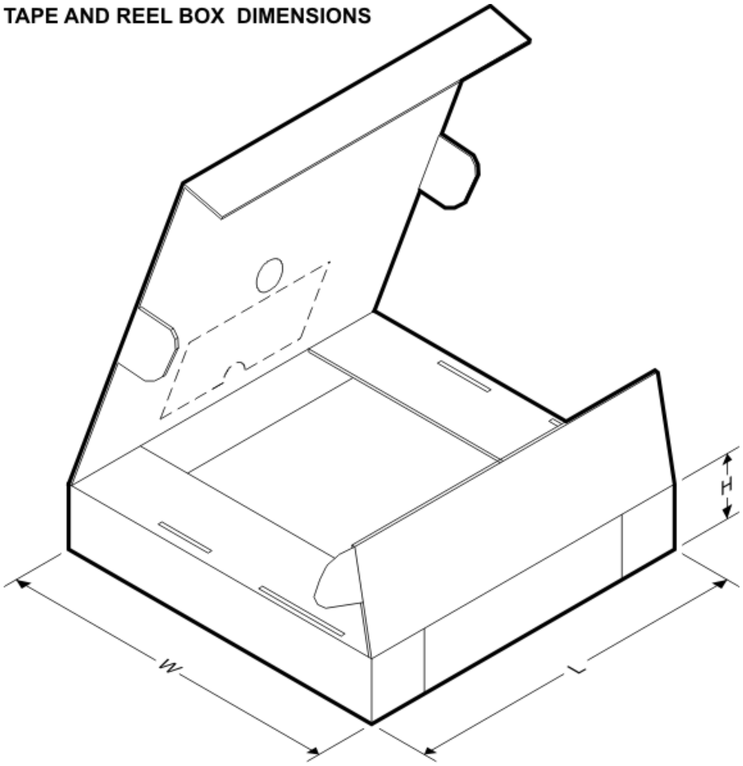
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

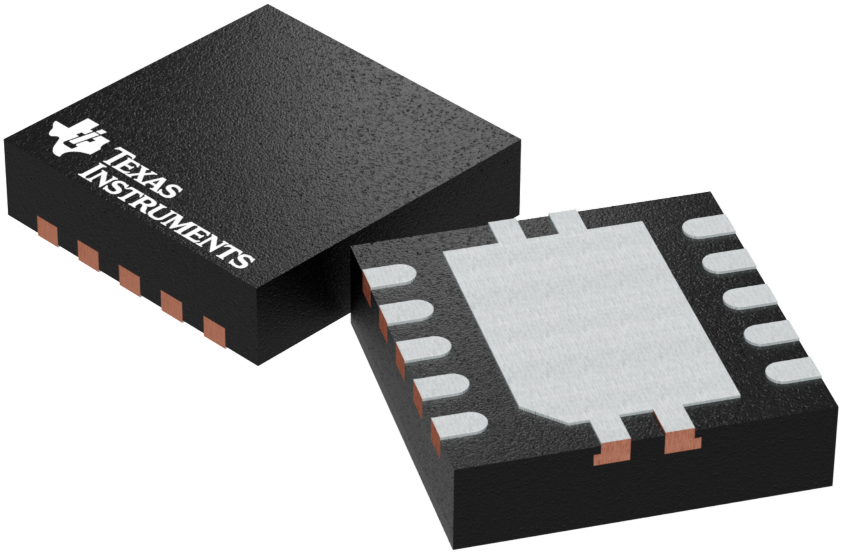
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS26620DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26620DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26621DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26621DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26622DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26622DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26623DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26623DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26624DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26624DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26625DRCR	VSON	DRC	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS26625DRCT	VSON	DRC	10	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

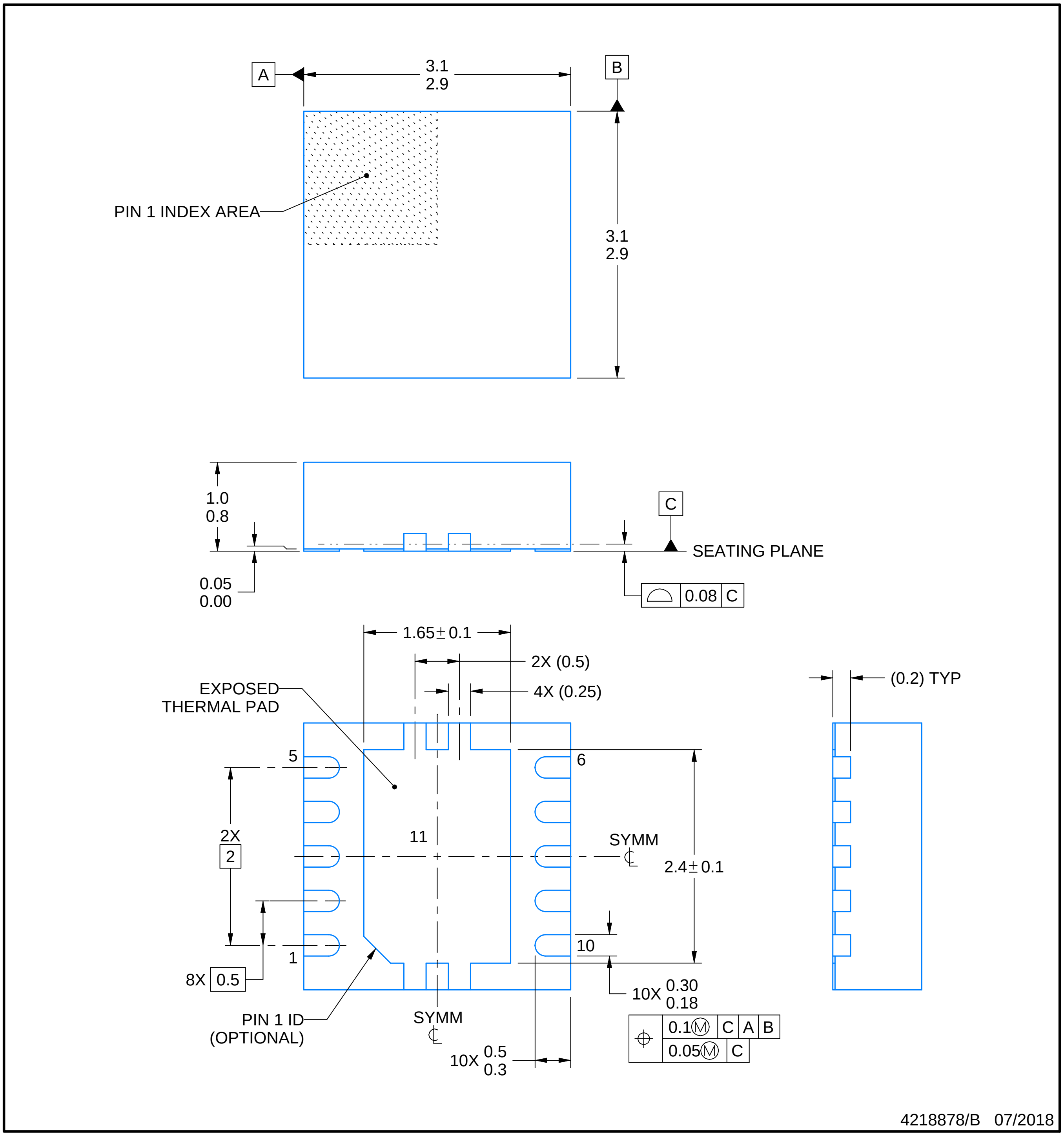


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS26620DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26620DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26621DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26621DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26622DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26622DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26623DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26623DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26624DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26624DRCT	VSON	DRC	10	250	210.0	185.0	35.0
TPS26625DRCR	VSON	DRC	10	3000	367.0	367.0	35.0
TPS26625DRCT	VSON	DRC	10	250	210.0	185.0	35.0

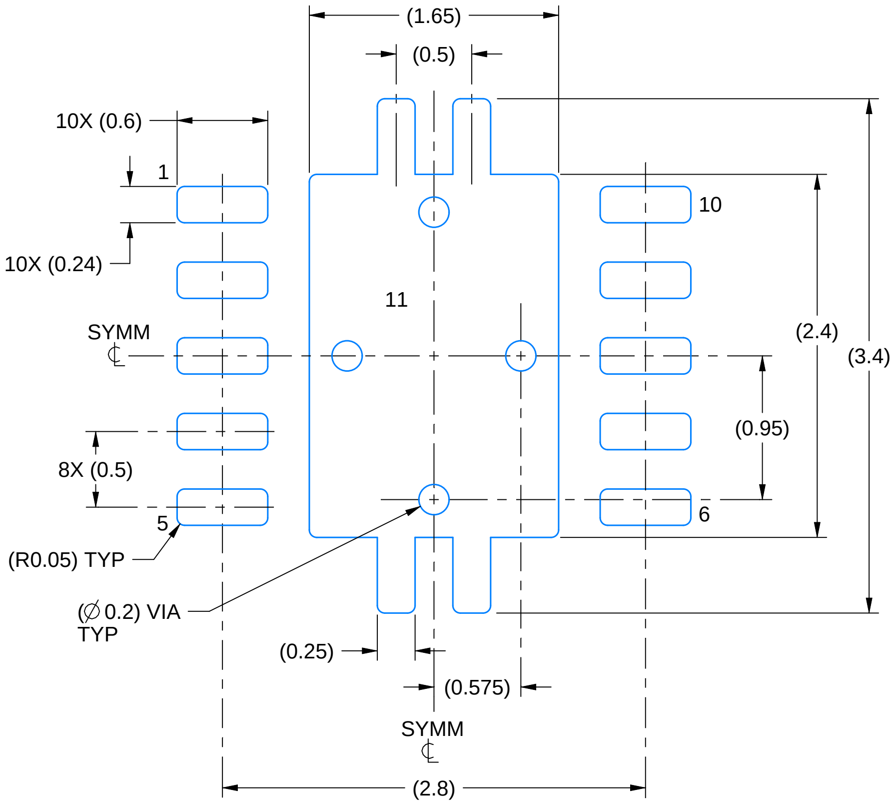


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

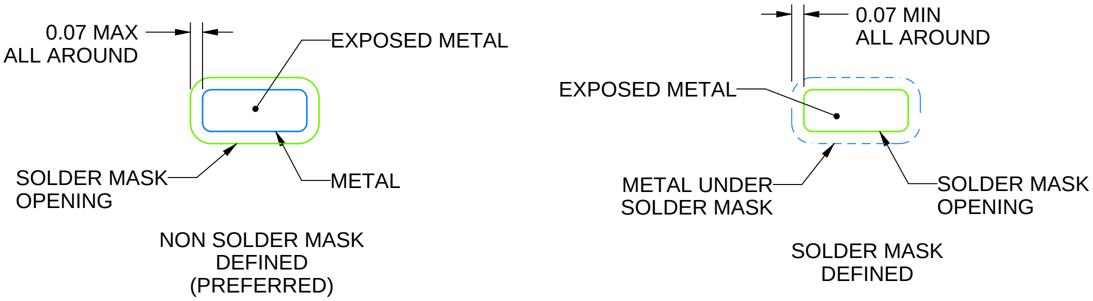


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



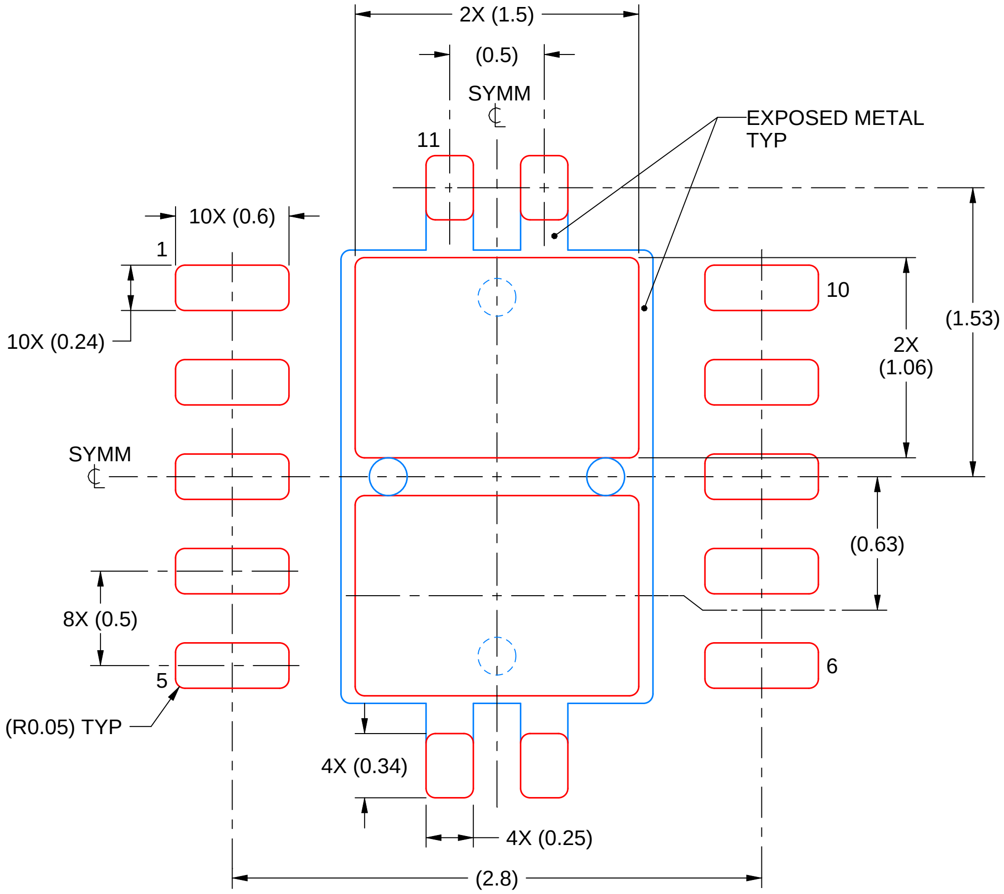
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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