Power Factor Correction without a Multiplier

The UCC28019 Power Factor Correction controller IC is capable of providing high-quality sinusoidal current (high power factor and low harmonics) without the use of a multiplier within the control loop. This is accomplished by forcing the input current to follow the off-time duty cycle D_{OFF}, which varies sinusoidally.

OVERVIEW

For the boost topology, $V_{OUT} = V_{IN} * 1/(1-D_{ON})$, where D_{ON} = Duty Cycle.

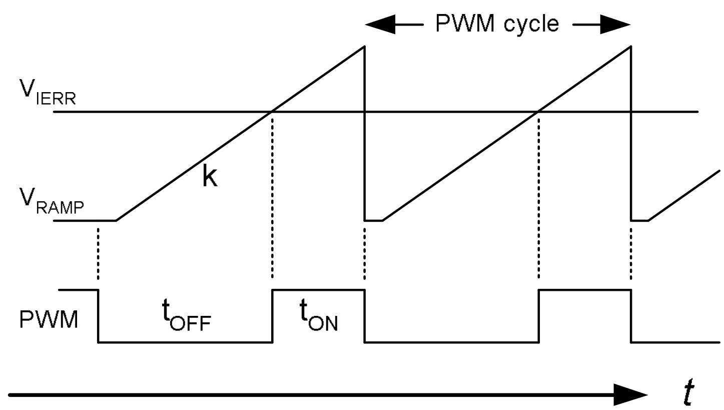
Rearranging terms, we get: $D_{OFF} = V_{IN} / V_{OUT}$, where $D_{OFF} = 1-D_{ON} = t_{OFF} / T_{SW}$.

Assume V_{OUT} is constant (neglect output ripple voltage) and $V_{IN} = V_{PK}|\sin(wt)|$,

then we see that D_{OFF} varies sinusoidally, $D_{OFF} = (V_{PK} / V_{OUT}) * |\sin(wt)|$

and so t_{OFF} also varies sinusoidally. $t_{OFF} = T_{SW} * (V_{PK} / V_{OUT}) * |\sin(wt)|$

Because of the 2x line frequency ripple on V_{OUT}, the voltage loop frequency response must be very slow, to avoid attenuation of this ripple. As a result, the voltage error amplifier output, VCOMP, can be considered a constant level during steady-state operation. VCOMP establishes a certain PWM ramp slope, k.
The current error amplifier provides a signal V_{IERR} proportional to I_L which is compared to the PWM ramp to establish the interval t_{OFF}.



We see that: $V_{IERR} = k * t_{OFF} = k * T_{SW} * (V_{PK} / V_{OUT}) * |\sin(wt)|$

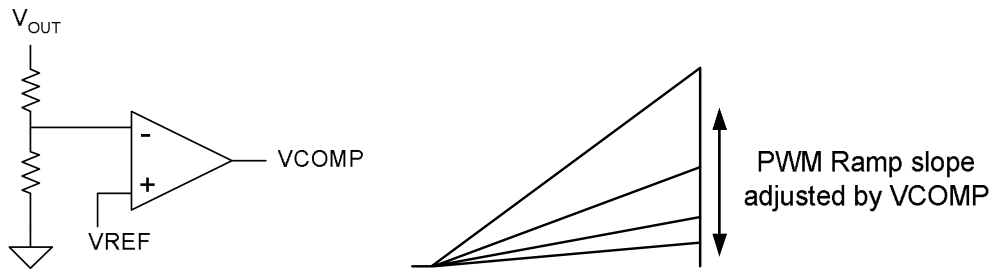
where k, T_{SW}, V_{PK}, and V_{OUT} can all be considered constants,
and V_{IERR} represents I_L, which is the same as I_{IN}.

During t_{ON}, V_{IN} is applied across the inductor. As V_{IN} increases, I_{IN} also increases.
For a given ramp slope, t_{OFF} increases proportional to V_{IN}.
Similarly, as V_{IN} decreases, I_{IN} also decreases.
The result is that I_{IN} tracks V_{IN}, and maintains a high power factor.

The voltage loop adjusts the slope k of the PWM ramp to maintain regulation of the output if operating load or line conditions change.

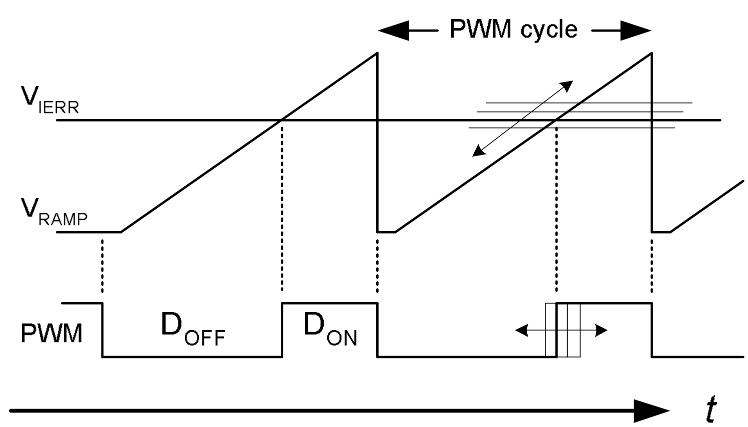
DETAIL

In the steady-state, the voltage error amplifier output seeks to maintain an equilibrium voltage at VCOMP for the amount of P_{IN} required, given a constant V_{IN} rms voltage. The VCOMP voltage is modified by a non-linear gain stage to establish a certain ramp slope at the PWM comparator.

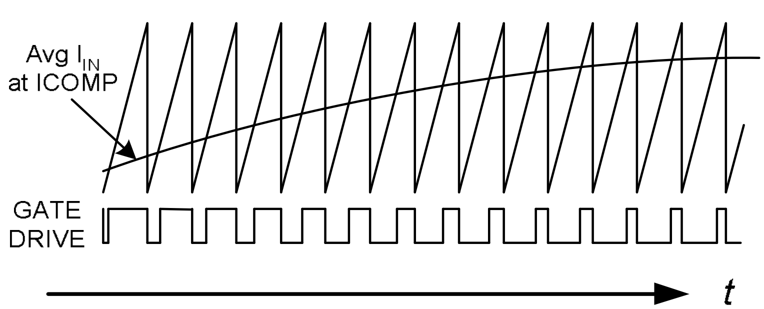


At the same time, the current error amplifier delivers a signal V_{IERR} proportional to the average inductor current I_L (switching ripple filtered out), which is also modified by a different non-linear gain and then compared to the PWM ramp.
(The inductor current is the same as the input current. $I_L = |I_{IN}|$)
The non-linear gains are applied to compensate for the wide variations in line and load that must be regulated within the limited voltage range of the PWM ramp.

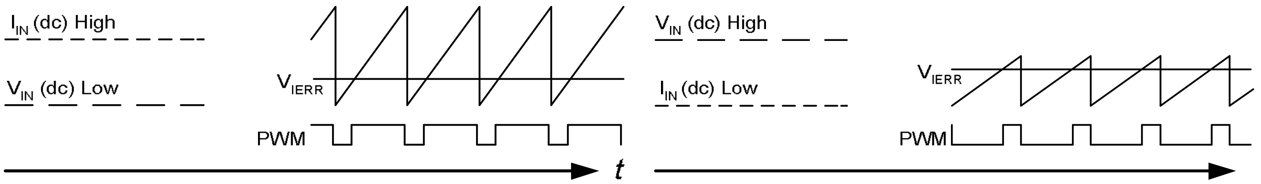
PWM occurs (D_{ON}) when the ramp voltage exceeds the modified current signal.



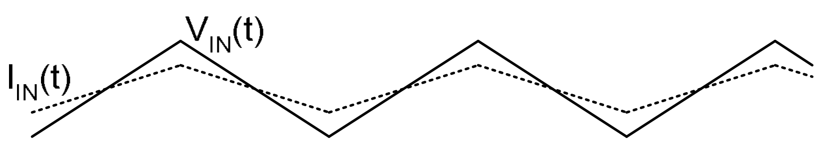
As V_{IN} increases, I_L (and average I_{IN}) grows during the ON-time of each switching cycle, tracking the increase of V_{IN}.



- Consider the case where V_{IN} is a constant dc level. Then in the steady-state, VCOMP sets a specific ramp slope such that the average I_{IN} matches t_{OFF} and stays constant. If V_{OUT} moved too low, VCOMP would slowly increase and the PWM ramp slope would increase – leading to longer ON-times and higher current. At some point V_{OUT} would get too high and VCOMP would decrease, the PWM ramp slope would decrease, and I_{IN} would then decrease. With proper loop compensation, the system finds a stable equilibrium and I_{IN} stays constant.



- Consider the case where V_{IN} is a periodic triangle voltage. Then in the steady-state, VCOMP sets a different ramp slope k, "constant" over the entire V_{IN} period (actually over several periods). As V_{IN} increases, I_L ramps up more than it ramps down each switching cycle (because V_{OUT}-V_{IN} decreases), so V_{IERR} (I_L) crossing the PWM ramp generates a progressively smaller D_{ON} (increasing D_{OFF}). Therefore, average I_L (and I_{IN}) follows V_{IN}. The same description holds for a decreasing V_{IN} ramp.



- Consider the case where V_{IN} is a sine wave. A sine wave can be thought of as an infinite series of voltage ramps with dc at the peaks. It follows then that I_L and I_{IN} match V_{IN} sinusoidally as well, because V_{IN} changes very slowly with respect to the switching frequency.