## Hello Nisarg,

It looks like the device is turning off due to a fault. When the device first power up when the VDD threshold reaches VDD(on) 4 gate driver pulses will be initiated to look for a fault. If a fault is observed the gate drive will stop, the reference will turn off and VDD will be discharged until it reaches (VDD(off)) and then will allow VDD to be charge to VDD(on) and will try to start again.

The following table list the faults that can trigger the UCC28780 controller chances are one of these will activate the fault. I also believe an under voltage/line fault may trigger this fault as well.

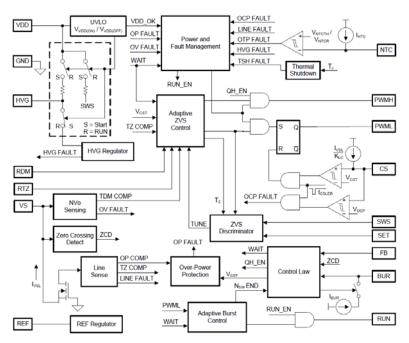
## 7.4.10 System Fault Protections

The UCC28780 provides extensive protections on different system fault scenarios. The protection features are summarized in Table 2.

Table 2. System Fault Frotection				
PROTECTION	SENSING	THRESHOLD	DELAY TO ACTION	ACTION
VDD UVLO	VDD voltage	$V_{VDD(OFF)} \le V_{VDD} \le V_{VDD(ON)}$	None	UVLO reset
Over-power protection (OPP)	CS voltage	$V_{CST(OPP)} \le V_{CST} \le V_{CST(MAX)}$	t <sub>OPP</sub> (160 ms)	t <sub>FDR</sub> restart (1.5s)
Peak current limit (PCL)	CS voltage	$V_{CST} \le V_{CST(MAX)}$		
Over-current protection (OCP)	CS voltage	V <sub>CS</sub> ≥ V <sub>OCP</sub>	3 PWML pulses	t <sub>FDR</sub> restart
Output short-circuit protection (SCP)	CS, VS, and VDD voltages	$ \begin{array}{l} (1) \ V_{VDD} = V_{VDD(OFF)} \& \ V_{CST} \geq V_{CST(OPP)} \ ; \ (2) \ V_{VDD} \\ = V_{VDD(OFF)} \& \ V_{VS} \leq 0.6 \ V \end{array} $	≤t <sub>OPP</sub>	t <sub>FDR</sub> restart
Output over-voltage protection (OVP)	VS voltage	$V_{VS} \ge V_{OVP}$	3 PWML pulses	t <sub>FDR</sub> restart
Brown-in detection	VS current	I <sub>VSL</sub> ≤ I <sub>VSL(RUN)</sub>	4 PWML pulses	UVLO reset
Brown-out detection	VS current	I <sub>VSL</sub> ≤ I <sub>VSL(STOP)</sub>	t <sub>BO</sub> (60ms)	UVLO reset
Over-temperature protection (OTP)	NTC voltage	R <sub>NTC</sub> ≤ R <sub>NTCTH</sub>	3 PWML pulses	UVLO reset until R <sub>NTC</sub> ≥ R <sub>NTCR</sub>
Thermal shutdown	Junction	$T_J \ge T_{J(STOP)}$	3 PWML pulses	UVLO reset

Table 2. System Fault Protection

## 7.2 Functional Block Diagram



You just need to determine which fault is shutting the device down. I would start with input under voltage. The EVM needs at least 90V RMS to startup. If you are feeding this with a DC supply you would need 127.3 V.

If it does not turn out to input under voltage you evaluated the aux winding that supplies power to VDD, the CS pin, PWL pin, and the output. With this information you should be able to determine the fault. More than likely it would be peak current limit (PCL), output over power (OPP) or over voltage fault. These are covered in section 7.4.10., 7.4.10.6, 7.4.10.7 in the data sheet.

Regards,

Mike