Boosting Efficiency in Off-line Power Converters

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Although losses are incurred when power supplies include power-factor correction, innovative control techniques enable designers to minimize the losses so they meet 80 PLUS guidelines for power factor and efficiency.

Over the past few years there has been a big push by some environmental agencies to have off-line ac-to-dc power converters include power-factor correction (PFC). It started with the European Union's EN61000-3-2 input-current harmonic content specifications for power converters. Even though this was not a power factor specification per se, power-supply designers found it easier to meet this requirement with PFC preregulators. So this specification was a driving force for off-line power converters to have PFC.

In the United States, electric utilities have been sponsoring the 80 PLUS incentive program, which offers a cash rebate for power converters that are greater than 80% efficient with a power factor of 0.9 at full load. Having PF preregulators in off-line power converters helps the power company greatly by reducing losses in the transmission lines and also by making better use of the available line power.

However, this benefit does not come for free and has created many challenges for power-supply designers. The PFC preregulator makes the off-line power converter less efficient, which makes it more difficult for some designs to meet the higher efficiency requirements of 80 PLUS. Fortunately, there are several innovative control techniques that make PFC preregulator designs more efficient.

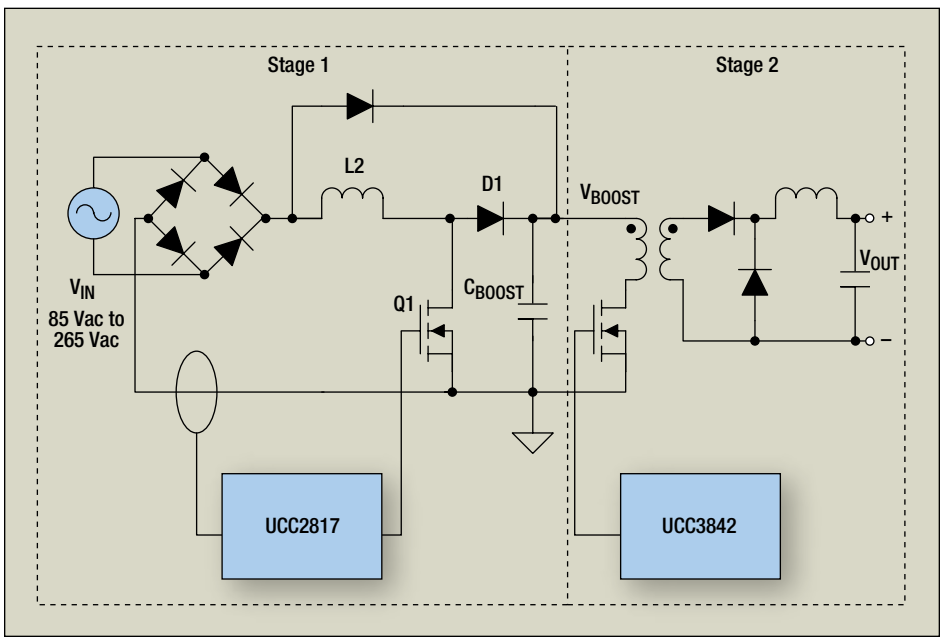

Fig. 1. *In off-line power supplies, a two-stage approach to power-factor correction is common. The front end, Stage 1, is a boost converter that shapes the input current and produces a high dc voltage, which is then stepped down by the converter in Stage 2.*

The Efficiency Penalty

It is no secret to the utilities that PFC reduces transmission line losses by reducing line root-mean-square (rms) currents caused by ac-to-dc power converters. However, off-line power converters with PFC are generally less efficient than a well-designed power converter without PFC.

Typically, off-line converters with PFC are done with two power stages. Stage 1 is generally a boost converter that uses average current-mode control techniques to shape the input current. Stage 2 is a step-down converter that steps the boost voltage down to a more usable voltage (Fig. 1). The overall total system efficiency (η_{TOTAL}) is the product of Stage 1's efficiency (η_{STAGE1}) and

Stage 2's efficiency (η_{STAGE2}), which makes for an overall less-efficient power supply:

$\eta_{TOTAL} = \eta_{STAGE1} \times \eta_{STAGE2}$.

A large contributor to losses in traditional PFC preregulators is the reverse-recovery current in the boost diode. The following equation describes the switching losses in the boost diode at a given switching cycle due to reverse-recovery current:

$$P_{D1_{SWITCHING}} = \frac{1}{2} I_D \times t_{RR} \times f_S,$$

where I_D is the peak diode current, t_{RR} is the boost diode's reverse-recovery time and f_S is the switching frequency at which the boost converter is operating.

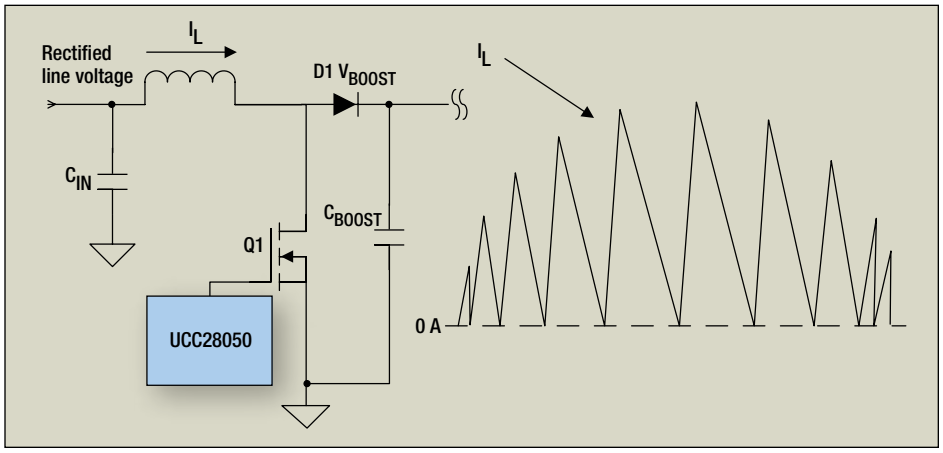

Fig. 2. *The transition-mode PFC preregulator (left) employs zero-current switching, whereby the controller waits for the inductor to completely de-energize before turning on the boost FET for the next switching cycle. A drawback of this circuit is that inductor ripple current (right) is twice the average input current.*

Transition-mode PFC

One PFC control technique adopted to remove reverse-recovery losses was the transition-mode PFC preregulator. This PFC boost preregulator incorporates zero-current switching to remove the reverse-recovery losses in the boost diode. The transition-mode PFC preregulators have zero-current detection that waits for the inductor to completely de-energize before turning on the boost FET for the next switching cycle. This technique uses pulse frequency modulation (PFM).

When designed correctly, the transition-mode PFC preregulator will have an inductor with a similar volume to the inductor used in an average current-mode control preregulator, but with no reverse-recovery losses in the boost diode. This characteristic also allows the designer to use inexpensive diodes. However, this topology does have some limitations. For example, the inductor ripple current is twice the average input current, which results in higher boost inductor and boost capacitor rms currents. These higher currents generally limit this topology to applications under 400 W. (Fig. 2).

Another major contributor to the losses in a PFC preregulator is the boost FET's switching losses. The following equation is an approximation of FET switching losses ($P_{Q1_{SWITCHING}}$) in a given switching cycle:

$$P_{Q1_{SWITCHING}} = \frac{1}{2} V_{BOOST} \times I_D \times (t_R + t_F) \times f_S + \frac{1}{2} \times C_{OSS} \times (V_{BOOST})^2 \times f_S + V_G \times Q_G \times f_S,$$

where V_{BOOST} is the PFC output voltage, I_D is the peak FET and diode current for a given switching period, f_S is the FET's switching frequency, and t_R and t_F are the FET's drain-to-source rise and fall times, respectively. C_{OSS} is the FET's total drain-to-source capacitance, V_G is the maximum voltage applied to the gate of the FET and Q_G is the FET's total gate charge.

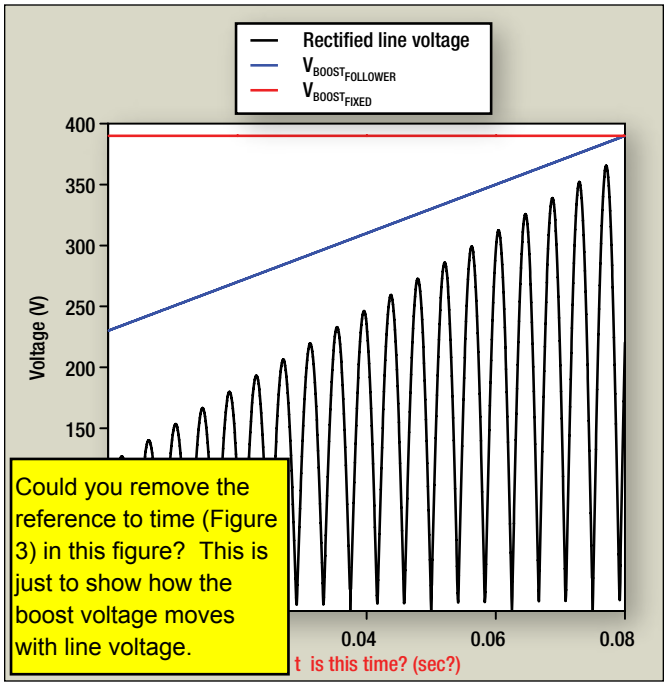

Fig. 3. *The PFC boost follower's output tracks changes in line voltage, improving the efficiency of the boost stage particularly at low line voltages.*

Traditionally, PFC preregulators are designed to have a fixed output voltage ($V_{BOOST_{FIXED}}$) that needs to be set higher than the peak input voltage. When the converter is operating at low line input, this high output voltage is greater than it needs to be and penalizes the converter's overall system efficiency. In Stage 2, the input to the downstream converter does not need a fixed input and can easily handle a 3:1 variation in input voltage.

To improve efficiency and reduce switching losses, a technique was developed called a PFC boost follower. This technique exploits the fact that a PFC preregulator generally is in a two-stage power system and does not require a fixed

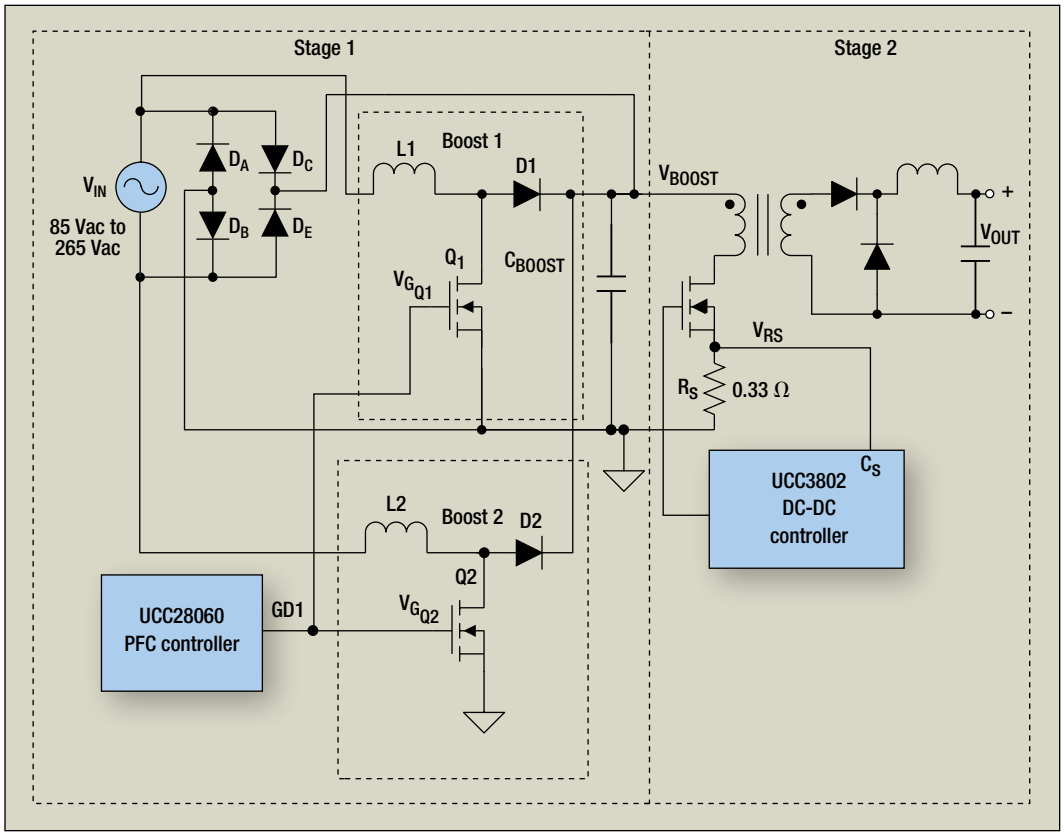

Fig. 4. *In an off-line converter with a semi-bridgeless PFC preregulator, only one of the bridge diodes (D_A or D_B) needs to conduct once the boost capacitor has been peak charged.*

output voltage. The boost follower converter is designed to have the boost voltage ($V_{BOOST_{FOLLOWER}}$) track changes in line voltage to improve system efficiency.

To alleviate the stress of holdup requirements on the boost capacitor, these converters typically are designed to have the minimum boost voltage (V_{BOOST}) set to be at least twice the peak input voltage at the minimum input line voltage. The boost follower's output will then increase and decrease with changes in line voltage to ensure the highest efficiency possible. Fig. 3 provides a graphical comparison of output voltage versus line voltage for a fixed output-voltage PFC boost and for a PFC boost follower.

The boost-follower innovation in PFC control greatly reduces switching losses but has one major limitation. This design typically requires four times the holdup capacitance of a fixed output-voltage PFC preregulator for universal applications where the input voltage varies 3:1.

Another promising topology for reducing losses in PFC preregulators and improving efficiency is the semi-bridgeless PFC preregulator (Fig. 4). This topology does require two boost stages, boost 1 and boost 2, where the boost inductors are tied directly to the input of the converter. It also requires a full-wave rectifier (D_A, D_B, D_C and D_E) to peak charge the common PFC boost capacitance (C_{BOOST}) during initial power-up.

However, after the boost capacitor has been peak charged, and the converter is up and running, the power converter only requires one rectifier diode at a time (D_A or D_B) in the diode bridge to conduct for proper operation. This is different from the traditional PFC boost, where two of the bridge rectifier diodes are always conducting. This innovative technique improves efficiency by removing the conduction losses of one rectifier diode, which improves overall system efficiency.

Interleaved Boost Stages

The latest innovation in PFC control is interleaved PFC boost stages. This control technique requires that two power factor corrected boost stages operate 180 degrees out of phase. The many benefits of this topology have made it so popular. A major one is the cancellation of input and output inductor ripple currents. If designed correctly, the interleaved boost PFC topology can reduce the total volume of the boost inductor and EMI filter

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result in up to a 25% reduction in capacitor volume. This is not to be confused with the amount of boost capacitance the design requires for holdup. That capacitance value is typically determined by holdup time and output power. Fig. 5 shows a functional schematic of an off-line power converter with interleaved PFC preregulator (Stage 1).

Another major benefit, interleaved PFC preregulators can reduce conduction losses by up to 50% when com-
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$_{ON_{SINGLE}}$) to the total conduction
FC ($P_{CONDUCTION_{INTERLEAVED}}$). The
ses should make the interleaved
ficient at higher power levels,
ominate. This helps to improve maximum load efficiency in the off-line converter:

Single Stage is correct. If you used single phase it would be confused with single phase operation when phase management is incorperated.

$P_{CONDUCTION_{SINGLE}} = I^2R$

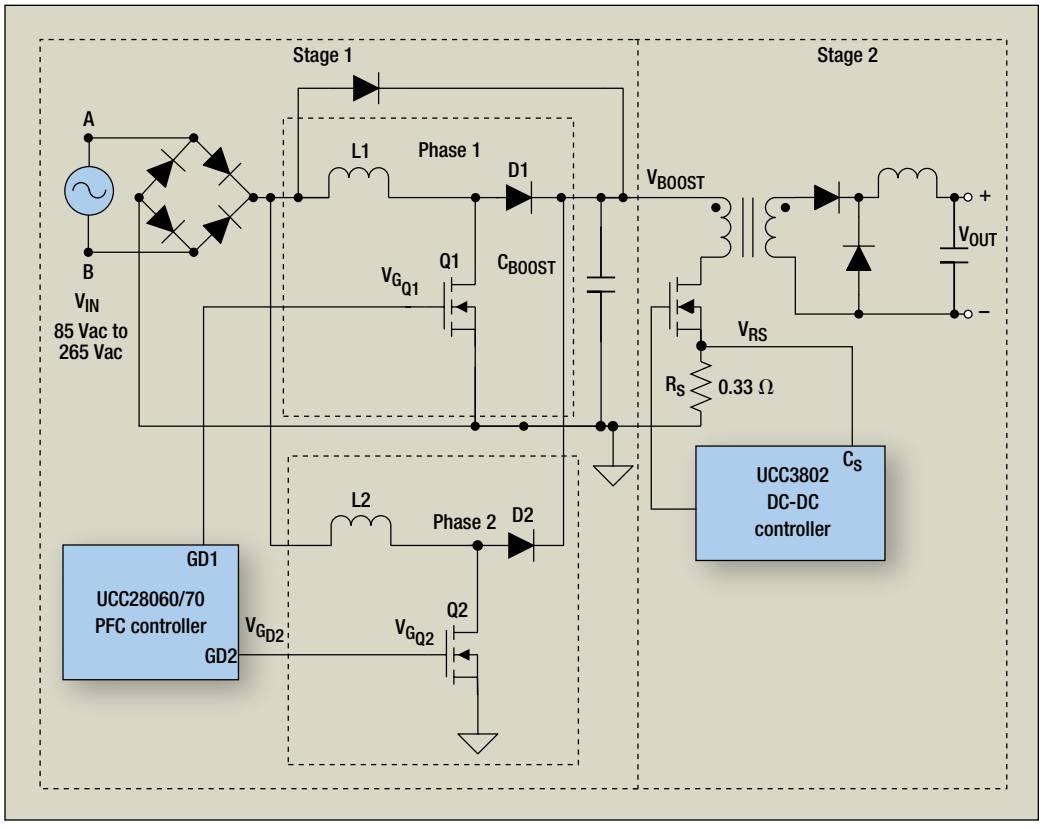

Fig. 5. *An off-line power converter with interleaved PFC offers multiple benefits such as the reduction in input and output ripple currents and lowered conduction losses.*

$$P_{CONDUCTION_{INTERLEAVED}} = \left(\frac{I}{2}\right)^2 R + \left(\frac{I}{2}\right)^2 R = \frac{I^2R}{2}$$

$$\frac{P_{CONDUCTION_{SINGLE}}}{2} = P_{CONDUCTION_{INTERLEAVED}}.$$

Even though interleaving PFC preregulators can improve efficiency where conduction losses dominate over switching losses, interleaving preregulators can decrease light-load system efficiency where switching losses dominate ($P_{SWITCHING}$). This added loss is mainly due to the increased FET C_{OSS} and gate-drive switching losses. The following equation is an approximation of total boost FET and boost diode switching losses for an interleaved PFC preregulator for a given switching cycle.

$$P_{SWITCHING} = 2\left(\frac{I_D V_{BOOST}(t_R + t_f)f_S}{2} + \frac{C_{OSS} \times (V_{BOOST})^2 f_S}{2} + V_G Q_G f_S + I_D V_{BOOST} t_{RR} f_S\right),$$

where V_G is the maximum gate voltage applied to the gate of the FET during activation and Q_G is the total gate charge at the maximum gate voltage.

To improve the interleaved PFC preregulator's efficiency, a control technique called phase management was developed. This technique requires control circuitry to monitor the converter's output power and turn on and off interleaved PFC phases based on the total loading of the converter.

At higher power levels where conduction losses dominate, the control circuitry has both phases enabled to reduce conduction losses. At lighter loads where switching losses dominate, the control circuitry turns off one of the phases and goes into single-phase operation. This reduces switching losses and makes it easier for the design to meet 80 PLUS light-load requirements. **PETech**