

BUR Hysteresis Circuitry to Eliminate ABM→AAM Transition (Audible Noise)

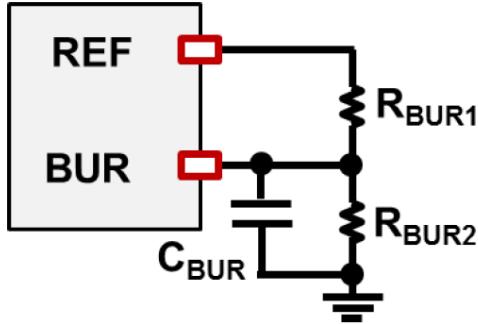
HVC

Jaden, Ning / Pei-Hsin, Liu

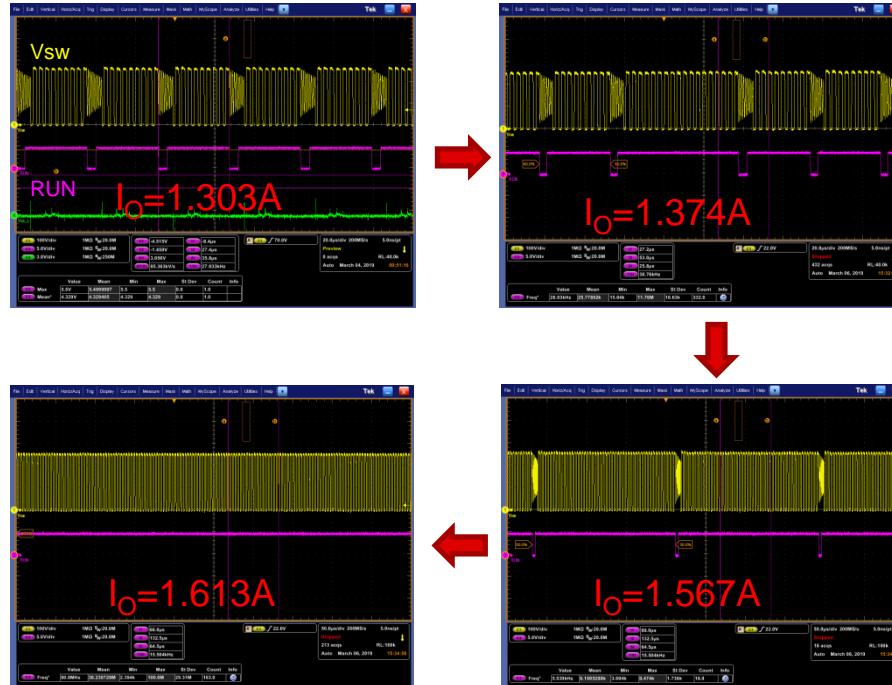
03/06/2019

Fixed BUR-Pin Voltage(V_{BUR}): $V_o=20V$

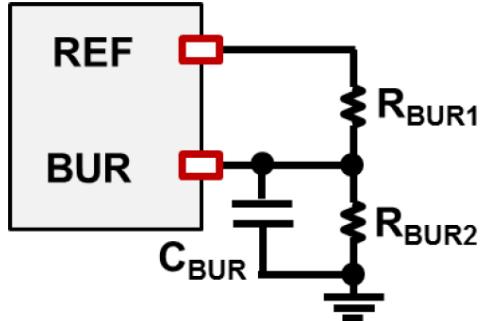
Test condition: $V_{in}=115V_{ac}$, $V_o=20V$, TI 45W EVM



- AAM-ABM transition is 0.3A for 20V/45W output
- For the design which varnished transformer and Lower V_{BUR} are acceptable



Fixed BUR-Pin Voltage(V_{BUR}): $V_o=5V$



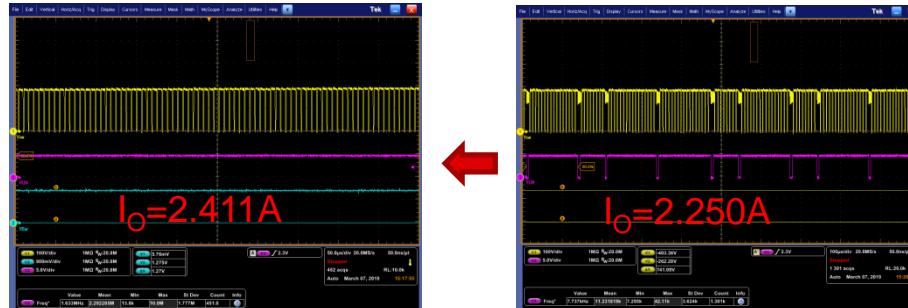
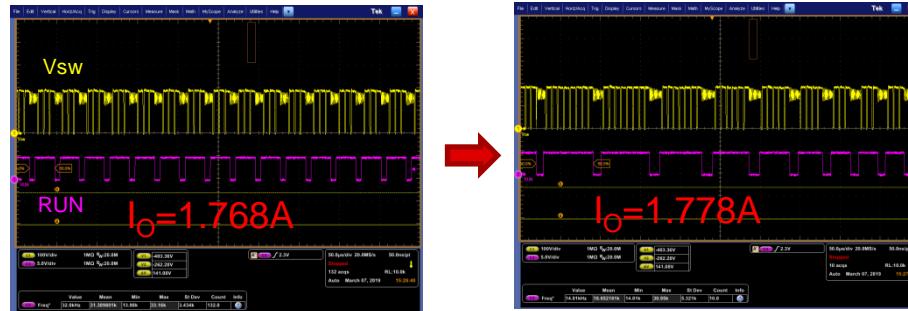
Test condition: $V_{in}=115\text{ Vac}$, $V_o=5\text{ V}$, TI 45W EVM

- Lower V_o results in lower f_{sw} operation.

When N_{sw} adjusts under lower f_{sw} case, f_{BUR} variation is larger,

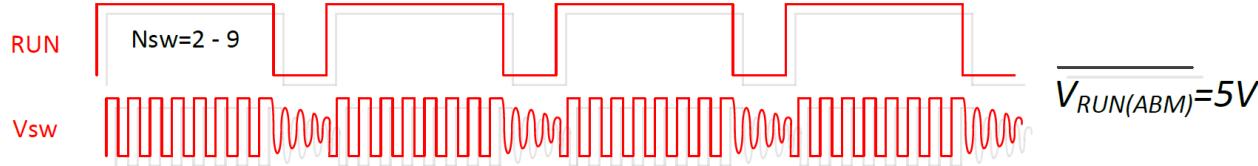
Larger variation f_{BUR} force ABM loop performing different N_{sw} among adjacent burst packets

- ABM-AAM transition is 0.6A for 5V output



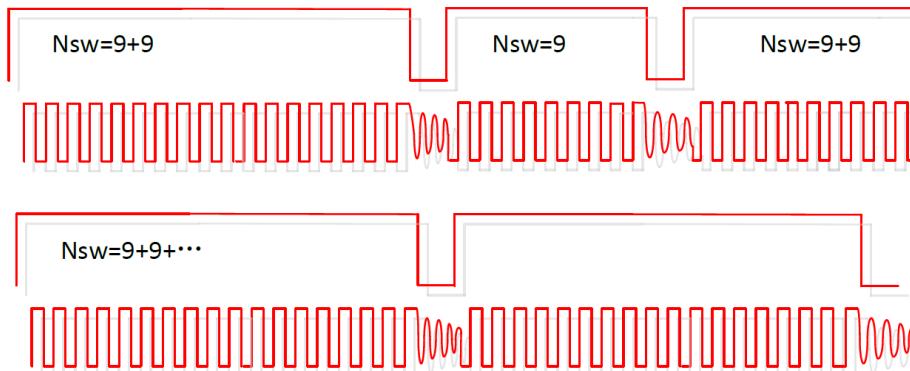
RUN Pin Voltage information

ABM:



$$\overline{V_{RUN(ABM)}} = 5V * (N_{SW}T_{SW}/T_{BUR})$$

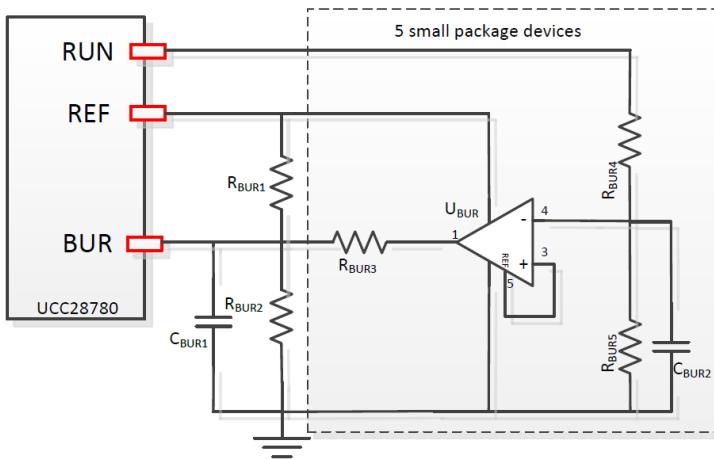
ABM-AAM Transition:



$$\overline{V_{RUN(ABM)}} \approx 5V$$

More Pulses (Nsw), Higher V_{RUN} , When V_{RUN} is closer to 5V, it indicates that it's deeper AAM-ABM transition

Circuit Design Example



*U_{BUR} is a open drain output comparator which integrated reference voltage

Design guide:

$$V_{RUN}=5V$$

$$V_{COMP_REF}=1.242V \text{ (TLV3011)}$$

$$D_{ABM}=N_{SW}T_{SW}/T_{BUR}$$

$$K_{DIVIDER}=R_{BUR5}/(R_{BUR4}+R_{BUR5})$$

$$V_{COMP_REF}=V_{RUN}*D_{ABM}*K_{DIVIDER}$$

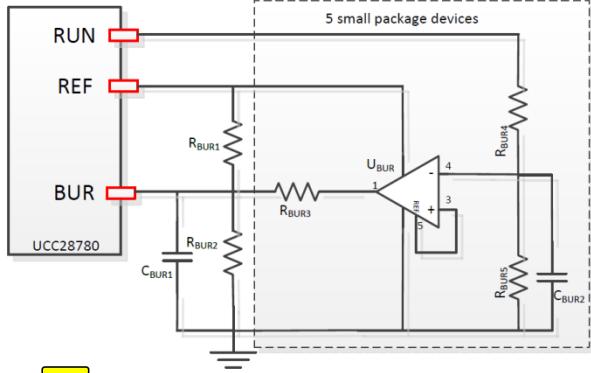
$$\frac{R_{BUR4}*R_{BUR5}}{R_{BUR4}+R_{BUR5}} * C_{BUR2} \approx 20\mu S$$

*D_{ABM} is around 0.86 ~0.95 when N_{SW} = 9 pulses

Ref	Recommend
R _{BUR1}	196k
R _{BUR2}	63.4k
C _{BUR1}	180pF
R _{BUR3}	150k
U _{BUR}	TLV3011AID
R _{BUR4}	427k
R _{BUR5}	150k
C _{BUR2}	180pF

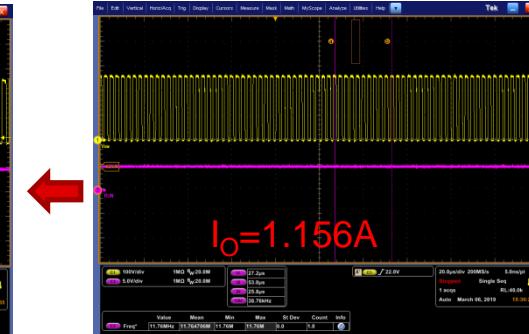
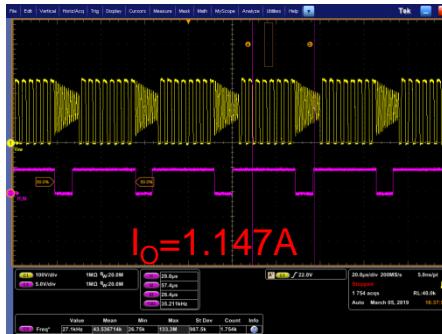
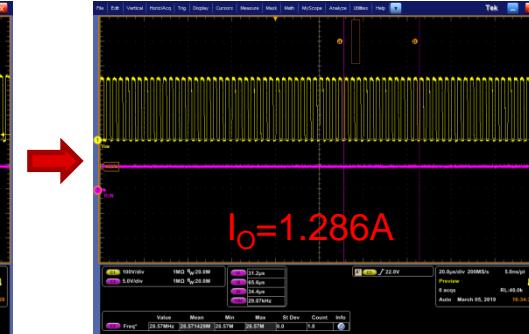
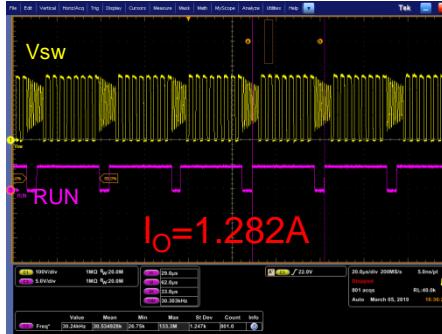
*All of R&C can use 0402 package

Verification at $V_O=20V$ (V_{BUR} : 1.22V \leftrightarrow 0.93V)

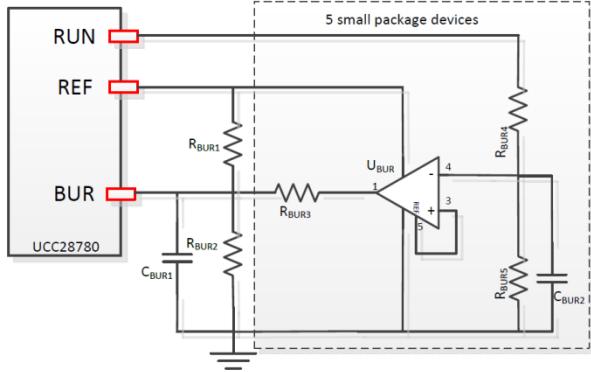


- Concept: When RUN frequency is low (More pulses in a burst package), R_{BUR3} parallel with R_{BUR2} , and lowering V_{BUR} to force controller into AAM
- For the design which varnished transformer and Lower V_{BUR} are Not acceptable

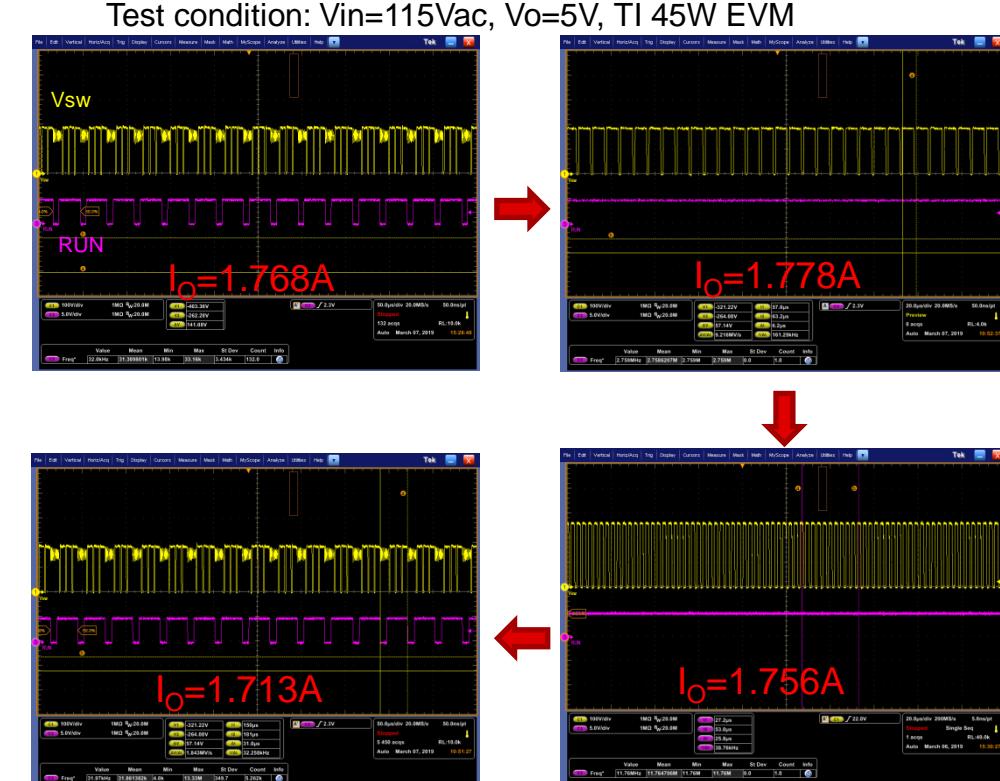
Test condition: $V_{in}=115\text{Vac}$, $V_O=20\text{V}$, TI 45W EVM



Verification at $V_O=5$ V (V_{BUR} : 1.22V \leftrightarrow 0.93V)



- Concept: When RUN frequency is low (More pulses in a burst package), R_{BUR3} parallel with R_{BUR2} , and lowering V_{BUR} to force controller into AAM
- For the design which varnished transformer and Lower V_{BUR} are Not acceptable



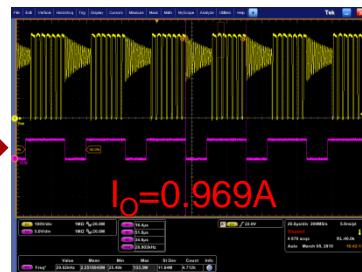
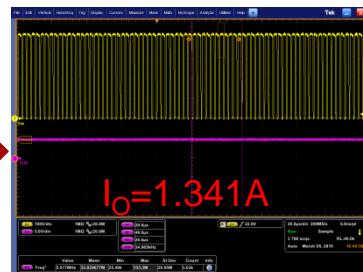
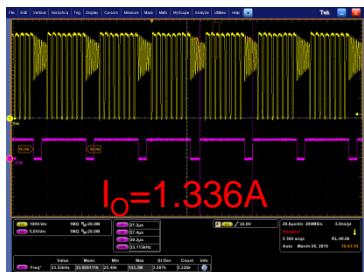
Debug tips(1)

- How to choose R_{BUR3}

R_{BUR3} set the hysteresis voltage (V_{Hys}) of V_{BUR} , Once V_{Hys} is enough for power stage jumping from ABM to AAM, The bigger , the better. Since large V_{Hys} will impact average efficiency. Special at high line.

R_{BUR1}	R_{BUR2}	V_{BUR}	R_{BUR3}	$V_{BUR RBUR3}$	V_{Hys}	I_o_{AAM}	I_o_{ABM}	I_{o_Hys}
196K	63.4K	1.219V	100k	0.826V	0.393V	1.322A	0.585A	0.737A
			150k	0.925V	0.294V	1.341A	0.969A	0.372A

* I_{o_AAM} means Load ramp up from 0A until controller entry AAM, while I_{o_ABM} means load ramp down from full load until controller entry ABM. $I_{o_Hys} = I_{o_AAM} - I_{o_ABM}$



	I_o	Pin(w)	$P_o(w)$	Effi.
ABM	1.00A	21.89	20.00	91.36%
AAM	1.00A	21.91	20.00	91.28%

*ABM: Load ramp up from 0A , so $I_o=1A$, Still in ABM

*AAM: Load ramp down from 2A, due to I_{o_Hys} .Still in AAM



Inclusion: Such as 0.372A I_{o_Hys} impact for average efficiency is ignorable

Condition: $V_{in}=230V_{ac}$, $V_o=20V$, $R_{BUR3}=150k$

TI Information – Selective Disclosure

Debug tips(2)

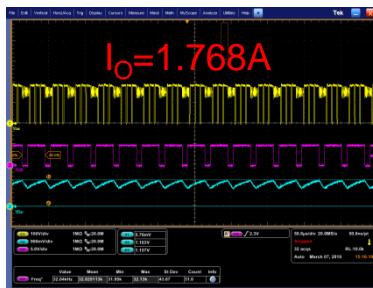
- How to choose C_{BUR2}

$$\frac{R_{BUR4} \cdot R_{BUR5}}{R_{BUR4} + R_{BUR5}} \cdot C_{BUR2} \approx 20\mu\text{s}$$

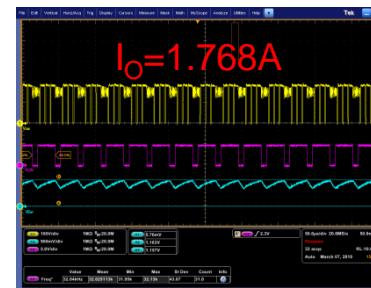


R_{BUR4}, R_{BUR5} and C_{BUR2} configured as filter for RUN signal, Too strong RUN filter will delays the response of comparator U_{BUR}, Special in low output voltage 5V when ABM-AAM transition happens. And smaller RUN filter time will in advance let ABM enter AAM than target setting.

C_{BUR2}=200pF



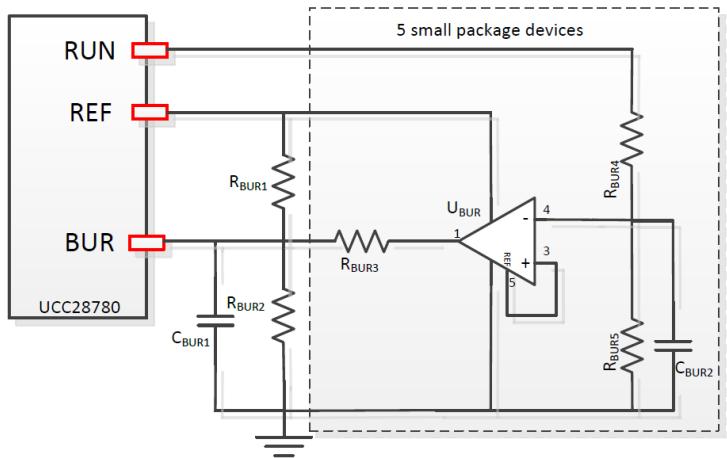
C_{BUR2}=180pF



Test condition: Vin=115Vac, Vo=5V

Note: Considering the tolerance of MLCC, C_{BUR2} value should be slightly decreased base on test results

Appendix



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