

4215105/A 11/2017

NOTES:

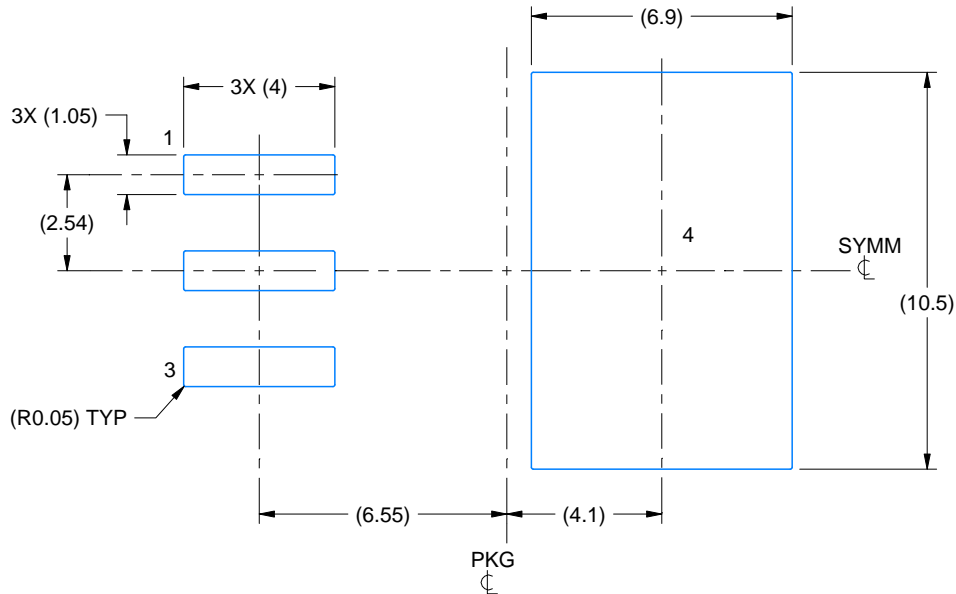
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Features may not exist and shape may vary per different assembly sites.
4. Reference JEDEC registration TO-263, except minimum lead thickness and minimum exposed pad length.

# EXAMPLE BOARD LAYOUT

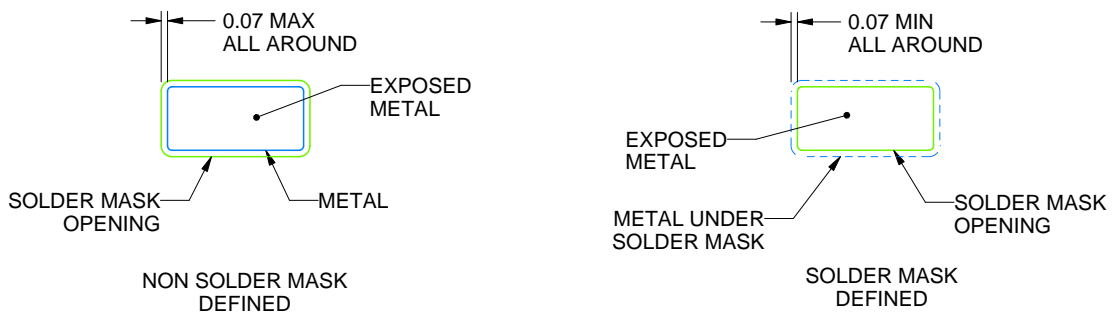
KTT0003B

TO-263 - 4.83 mm max height

TO-263



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:5X



SOLDER MASK DETAILS

4215105/A 11/2017

NOTES: (continued)

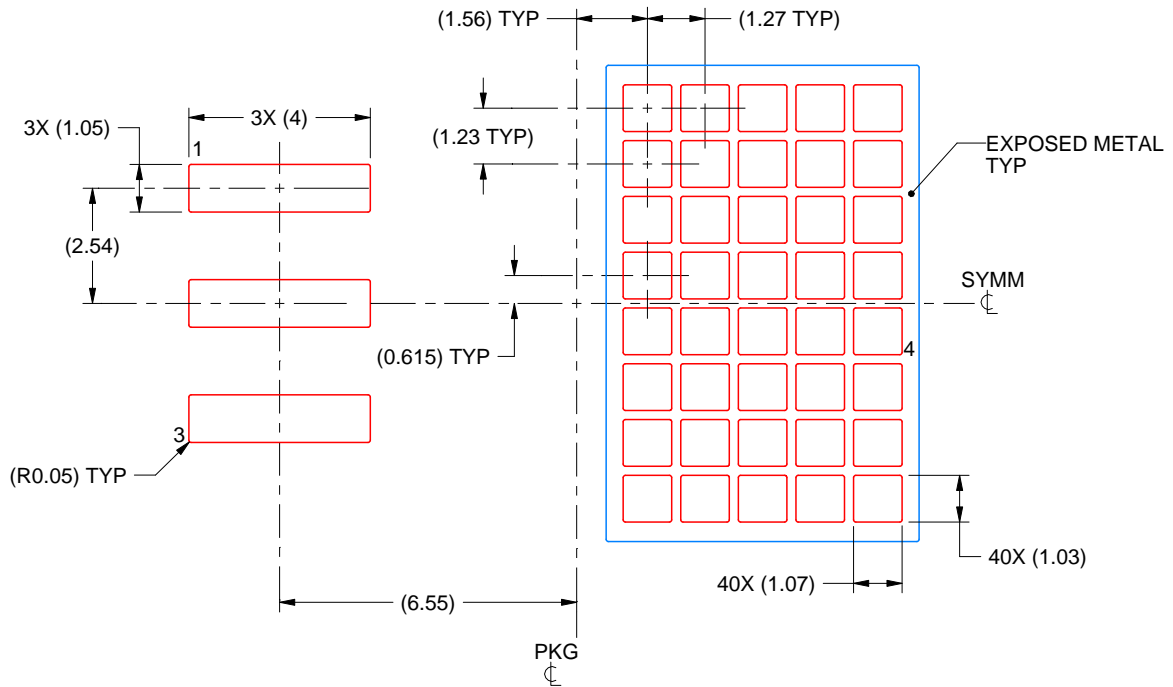
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slm002](http://www.ti.com/lit/slm002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
6. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

KTT0003B

TO-263 - 4.83 mm max height

TO-263



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
EXPOSED PAD  
60% PRINTED SOLDER COVERAGE BY AREA  
SCALE:6X

4215105/A 11/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.