REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change to military drawing format. Add vendors CAGE 48726, 34333, and U4637. Editorial changes throughout.	87-03-20	M. A. FRYE
B	Change CAGE code to 67268. Add device type 02. Delete vendor CAGE code U4637. Delete switching circuits. Extensive changes to table I. Editorial changes throughout.	88-07-20	M. A. FRYE
C	Add one vendor CAGE U4637 for device types 01 and 02. Inactivate device type 01 for new design.	89-05-03	M. A. FRYE
D	Changes in accordance with N.O.R. 5962-R155-92.	92-12-23	M. A. FRYE
E	Changes in accordance with N.O.R. 5962-R103-95.	94-04-19	M. A. FRYE
F	Add power dissipation, theta JA, and derating limits for case outline 2 as specified in paragraph 1.3. - ro	02-02-07	R. MONNIN
G	Make correction to Marking paragraph 3.5. - ro	05-06-03	R. MONNIN
H	Update drawing to current requirements of MIL-PRF-38535. -rrp	11-11-08	C. SAFFLE
J	Update drawing to current requirements of MIL-PRF-38535. -jch	20-07-24	J. ESCHMEYER

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

REV																				
SHEET																				
REV	J	J																		
SHEET	15	16																		

REV STATUS	REV	J	J	J	J	J	J	J	J	J	J	J	J	J	J
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
DONALD R. OSBORNE

DLA LAND AND MARITIME
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
D.A.DiCENZO

APPROVED BY
N. A. HAUCK

DRAWING APPROVAL DATE
86-02-19

REVISION LEVEL
J

MICROCIRCUIT, LINEAR, REGULATING PULSE WIDTH MODULATOR, MONOLITHIC SILICON

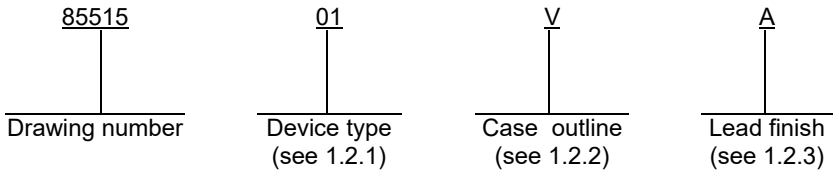
SIZE	CAGE CODE	
A	**14933**	**85515**

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:



1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	1526	Pulse-width modulator
02	1526A	Pulse-width modulator

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Input voltage (V_{IN}) ..... 40 V dc
Collector supply voltage (V_C) ..... 40 V dc
Logic inputs ..... -0.3 V dc to +5.5 V dc
Analog inputs ..... -0.3 to +V_{IN}
Output current (I_{SOURCE} or I_{SINK}) ..... ±200 mA
Reference output current ..... 50 mA
Maximum power dissipation (P_D) (T_A = +25°C):
  Case V ..... 1,000 mW 1/ 2/
  Case 2 ..... 1,500 mW 1/ 2/
Maximum junction temperature (T_J) ..... +150°C
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):
  Case V ..... 100°C/W
  Case 2 ..... 80°C/W

1/ For case V, derate at 10 mW/°C for ambient temperatures above +50°C. For case 2, derate at 13 mW/°C for ambient temperatures above +25°C.
2/ Must withstand the added P_D due to short circuit current; e.g., I_{OS}.

1.4 Recommended operating conditions.

Input voltage (V_{IN}):
Device type 01 ..... 8 V dc to 35 V dc
Device type 02 ..... 7 V dc to 35 V dc
Collector supply voltage (V_C) ..... 4.5 V dc to 35 V dc
Ambient operating temperature (T_A) ..... -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 2.

3.2.4 Switching waveforms. The switching waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Power consumption section							
Standby current	I_{IN}	$\overline{SHUTDOWN}$ = 0.4 V,	1,2,3	01		30	mA
		V_{IN} = 35 V		02		20	
Reference section							
Reference output voltage	V_{REF}	I_{LOAD} = 0 mA	1	All	4.95	5.05	V
			2,3		4.90	5.10	
Line regulation	V_{RLINE}	V_{IN} = 8 V to 35 V	1,2,3	01		20	mV
		V_{IN} = 7 V to 35 V		02		10	
Load regulation	V_{RLOAD}	I_{LOAD} = 0 mA to -20 mA	1,2,3	01		30	mV
				02		20	
Short circuit current	I_{OS}	V_{REF} = 0 V, t ≤ 25 ms	1,2,3	01	-125		mA
				02	-100		
Output noise voltage	N_O	f_O = 10 Hz to 10 kHz T_A = +25°C 3/	4	All		200	μVrms
Ripple rejection	ΔV_{IN} /	V_{IN} = 15 V,	4	01	50		dB
	ΔV_{REF}	+1 V rms at 2.4 kHz	4,5,6	02	50		
Oscillator section 4/							
Initial accuracy	A_{CC}	R_T = 4.12 kΩ ±0.1%, C_T = 0.01 μF ±0.1 %,	4	All	36.8	43.2	kHz
		$R_{deadtime}$ = 0 Ω	5,6	02	36	44	
Voltage stability	Δf_{OSC}	V_{IN} = 8 V to 35 V	4,5,6	All		1	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Oscillator section – continued. 4/							
Maximum frequency	f_{OSC} (MAX)	R_T = 2 kΩ, C_T = 470 pF	4,5,6	01	400		kHz
				02	500		
Clock width	t_{PW}	2 kΩ pull up applied to SYNC pin, T_A = +25°C	9	01		2.0	µs
				02		1.6	
Sawtooth peak voltage	V_{RAMPPK}	V_{IN} = 35 V, f = 40 kHz	4,5,6	All	2.7	3.5	V
Sawtooth valley voltage	$V_{RAMPVLY}$	V_{IN} = 8 V, f = 40 kHz	4,6	All	0.5		V
			5		0.45		
Pulse width modulator (PWM) comparator section							
"A" minimum duty cycle	t_{ON}	V_{COMP} = 0.4 V, V_{CM} = 0 V, R_T = 4.12 kΩ ±0.1%, C_T = 0.01 µF ±0.1 %, $R_{deadtime}$ = 0 Ω	9,10,11	All		0	%
"B" minimum duty cycle	t_{OSC} (MIN)	V_{COMP} = 0.4 V, V_{CM} = 0 V, R_T = 4.12 kΩ ±0.1%, C_T = 0.01 µF ±0.1 %, $R_{deadtime}$ = 0 Ω	9,10,11	All		0	%

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Pulse width modulator (PWM) comparator section - continued							
"A" maximum duty cycle	t_{ON}	V_{COMP} = 3.6 V, V_{CM} = 0 V, R_T = 4.12 kΩ ±0.1%, C_T = 0.01 µF ±0.1 %, $R_{deadtime}$ = 0 Ω	9,10,11	All	45		%
"B" maximum duty cycle	t_{OSC} (MAX)	V_{COMP} = 3.6 V, V_{CM} = 0 V, R_T = 4.12 kΩ ±0.1%, C_T = 0.01 µF ±0.1 %, $R_{deadtime}$ = 0 Ω	9,10,11	All	45		%
Error amplifier section							
Input offset voltage	V_{IO}	$R_S \le 2$ kΩ, V_{NI}(+ERROR pin) = 2.5 V	1,2,3	All		5	mV
+Input bias current	$+I_{IB}$	$R_S \le 2$ kΩ, VNI(+ERROR pin) = 2.5 V	1,2,3	All		1	µA
-Input bias current	$-I_{IB}$	$R_S \le 2$ kΩ, VNI(+ERROR pin) = 2.5 V	1,2,3	All		1	µA
Input offset current	I_{IO}	$R_S \le 2$ kΩ, VNI(+ERROR pin) = 2.5 V	1,2,3	All		0.1	µA
Open loop gain	A_{VS}	$R_L \ge 10$ MΩ	4	01	64		dB
			4,5,6	02	64		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Error amplifier section - continued							
Common mode rejection ratio	CMRR	V_{CM} = 0 V to 5.2 V	4,5,6	All	70		dB
Supply voltage rejection ratio	SVRR	V_{IN} = 8 V to 35 V,	4	01	66		dB
		V_{CM} = 2.5 V	4,5,6	02	66		
Output high level voltage	V_{HI}	$V_{+ERROR} - V_{-ERROR} \ge$ 150 mV, I_{SOURCE} = -100 µA	4,5,6	All	3.6		V
Output low level voltage	V_{LO}	$V_{-ERROR} - V_{+ERROR} \ge$ 150 mV, I_{SINK} = 100 µA	4,5,6	All		0.4	V
Unity gain band width	G_{BW}	A_V = 0 dB, 3/ T_A = +25°C	4	All	800		kHz
Output drivers section							
Saturation voltage, Side A at 20 mA Side B at 20 mA	$V_{CE(SAT)}$	V_C = 15 V, I_{SINK} = 20 mA, SHUTDOWN = GND	1,2,3	All		0.3	V
Saturation voltage, Side A at 100 mA Side B at 100 mA	$V_{CE(SAT)}$	V_C = 15 V, ISINK = 100 mA, SHUTDOWN = GND	1,2,3	All		2.0	V
High output voltage, Side A at 20 mA Side B at 20 mA	V_{EO}	V_C = 15 V, V_{NI} = 5 V, I_{SOURCE} = -20 mA, $V_{I(-ERROR\ pin)}$ = GND	1,2,3	All	12.5		V
High output voltage, Side A at 100 mA Side B at 100 mA	V_{EO}	VC = 15 V, VNI = 5 V, I_{SOURCE} = -100 mA, $V_{I(-ERROR\ pin)}$ = GND	1,2,3	All	12.0		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Output drivers section - continued							
Shut down delay time, Side A,	t_{SD}	V_C = 15 V, 3/	9	01		0.5	µs
Side B		T_A = +25°C		02		0.3	
Rise time Side A	t_R	V_C = 15 V,	9,10,11	01		0.6	µs
Side B		C_L = 1000 pF		02		0.3	
Fall time Side A, Side B	t_F	V_C = 15 V, C_L = 1000 pF	9,10,11	All		0.2	µs
Collector leakage current, Side A or side B	I_{CEX}	V_C = 35 V, SHUTDOWN = GND	1,2,3	All		150	µA
Total cross conduction charge	Q_{tot}	Total of outputs A+B per complete cycle of output A and output B 5/	1,2	02		12.5	nC
			3			25	
Digital ports section							
High input current: SYNC , RESET , and SHUTDOWN pins	I_{IH}	V_{IH} = 2.4 V	1,2,3	01	-300		µA
				02	-200		
Low input current: SYNC , RESET , and SHUTDOWN pins	I_{IL}	V_{IL} = 0.4 V	1,2,3	01	-500		µA
				02	-360		
High output voltage: SYNC , RESET , and SHUTDOWN pins	V_{OH}	I_{SOURCE} = -40 µA	1,2,3	All	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

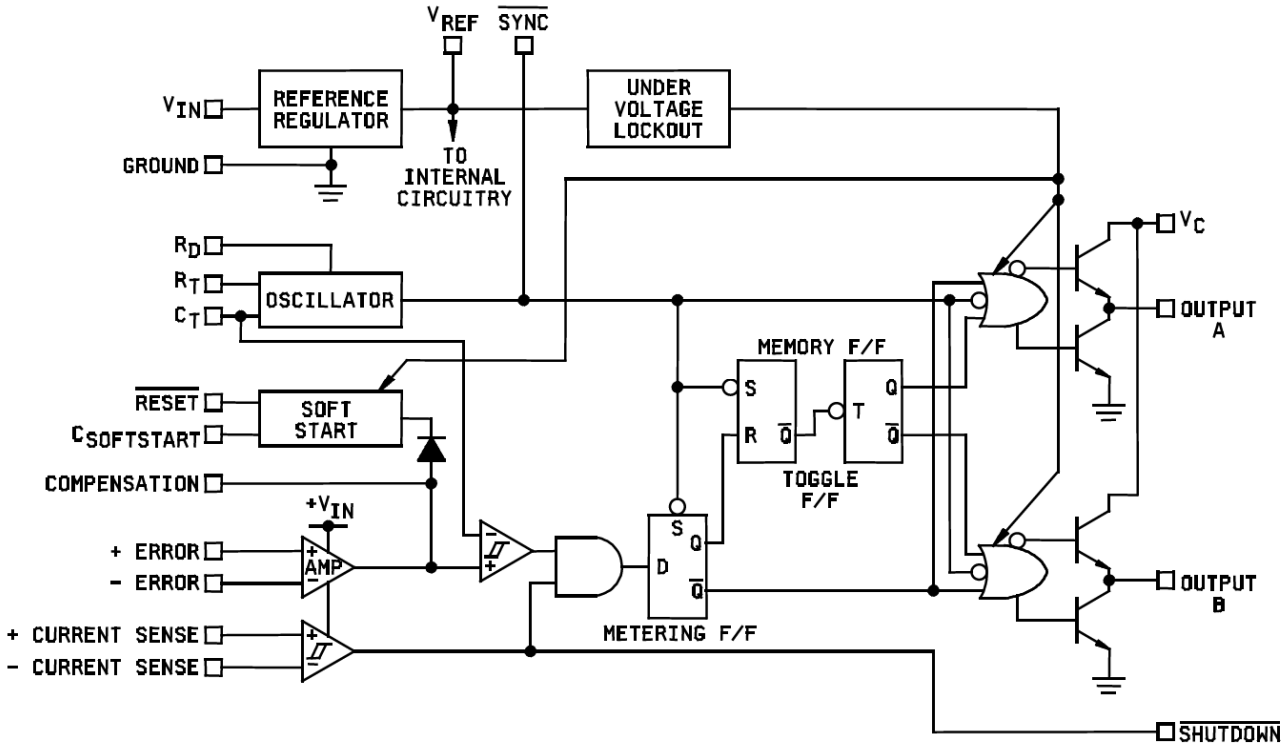
Test	Symbol	Conditions 1/ -55°C ≤ TA ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits 2/		Unit
					Min	Max	
Digital ports section - continued							
Low output voltage: $\overline{SYNC}$, $\overline{RESET}$, and $\overline{SHUTDOWN}$ pins	V_{OL}	I_{SINK} = 3.6 mA	1,2,3	All		0.4	V
Current limit comparator section							
Sense voltage	V_S	V_{CM} = 0 V to 12 V	4	All	90	110	mV
			5,6	01	60	150	
				02	90	110	
Input bias current	I_{IB}	V_{CM} = 0 V	4,5,6	All	-10		µA
Soft start section							
Error clamp voltage	V_{EC}	$\overline{RESET}$ = 0.4 V	4,5,6	All		0.4	V
Capacitor change current	I_{CS}	$\overline{RESET}$ = 2.4 V	4,5,6	All	50	150	µA
Under voltage lockout section							
$\overline{RESET}$ pin out low voltage	$V_{\overline{RL}}$	V_{REF} = 3.8 V	4,5,6	All		0.4	V
$\overline{RESET}$ pin out high voltage	$V_{\overline{RH}}$	V_{REF} = 4.8 V	4,5,6	All	2.4		V

1/ Unless otherwise specified, $V_{IN} = V_C$ = +15 V.
2/ The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
3/ If not tested, shall be guaranteed to specified limits in table I herein.
4/ A 2.7 kΩ pull-up resistor or equivalent may be added from the $\overline{SYNC}$ pin to V_{REF} pin to limit the effects of stray capacitance in automatic test equipment.
5/ Tested at oscillator maximum frequency (R_T = 2 kΩ, C_T = 470 pF).
Total cross conduction charge is defined as: $2(I_{(VC\ pin)} / f_{OSC})$, where the current at the VC pin is the average current in V_C pin and f_{OSC} is the oscillator frequency.

Device type	01 and 02	
Case outlines	V	2
Terminal number	Terminal symbol	
1	+ERROR	NC
2	-ERR0R	+ERROR
3	COMPENSATION	-ERROR
4	$C_{SOFTSTART}$	COMPENSATION
5	$\overline{RESET}$	$C_{SOFTSTART}$
6	-CS	$\overline{RESET}$
7	+CS	-CS
8	$\overline{SHUTDOWN}$	+CS
9	R_T	$\overline{SHUTDOWN}$
10	C_T	R_T
11	$R_{DEADTIME}$	C_T
12	$\overline{SYNC}$	$R_{DEADTIME}$
13	OUTPUT A	$\overline{SYNC}$
14	V_C	OUTPUT A
15	GROUND	V_C
16	OUTPUT B	NC
17	V_{IN}	GROUND
18	V_{REF}	OUTPUT B
19	---	V_{IN}
20	---	V_{REF}

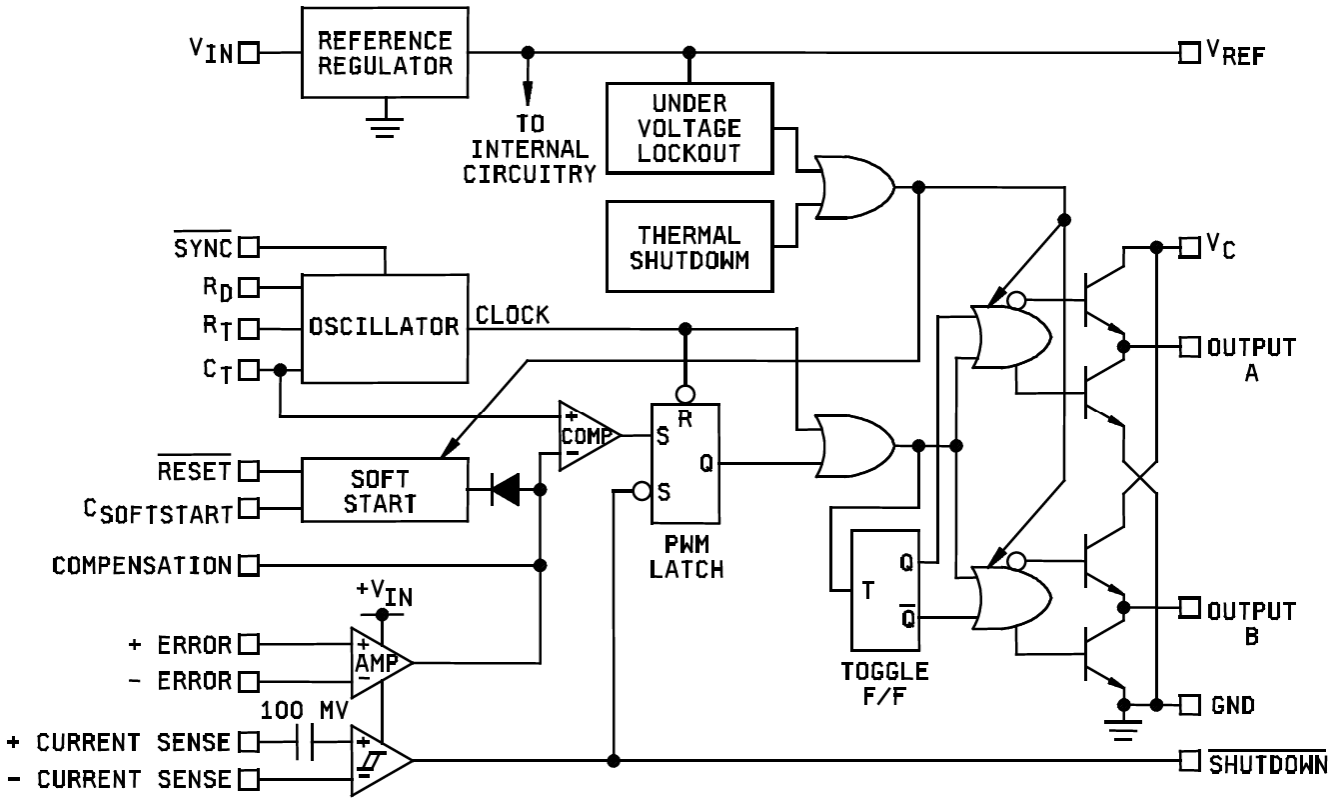
NC = No connection

FIGURE 1. Terminal connections.



NOTE: All others with the exception of CAGE 01295.

FIGURE 2. Logic diagram.



NOTE: For CAGE 01295 devices only, the oscillator's $\overline{\text{SYNC}}$ is not connected to the output gates.

FIGURE 2. Logic diagram – continued.

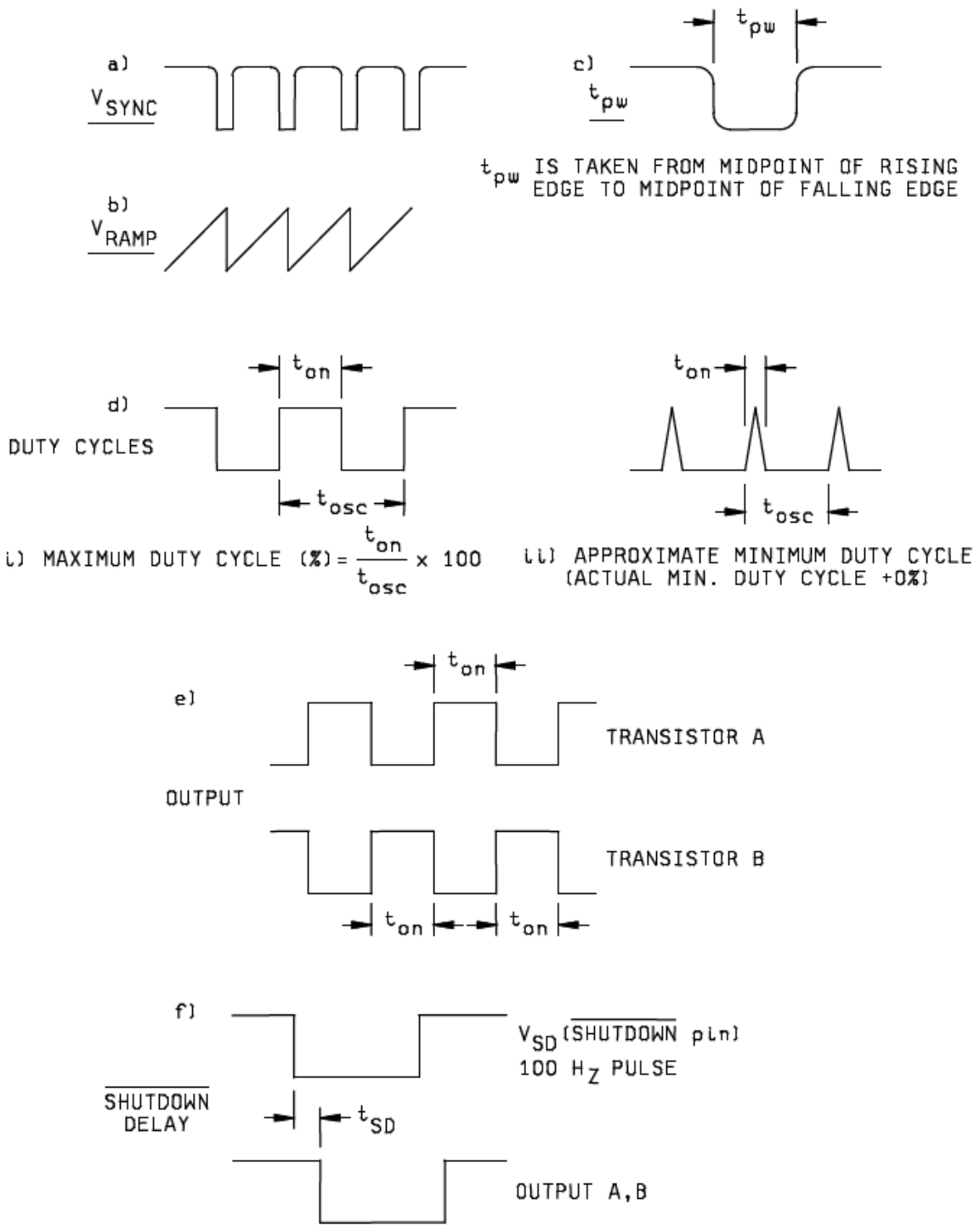


FIGURE 3. Switching waveforms.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,4
Group A test requirements (method 5005)	1,2,3,4,5,6,9,10**,11**
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroup 1.
** Subgroups 10 and 11 shall be guaranteed, if not tested, to the limits specified in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 20-07-24

Approved sources of supply for SMD 85515 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/	Reference military specification PIN
8551501VA	01295	UC1526J/883	M38510/12603BVA
	34333	SG1526BJ-DESC	
	3/	LT1526J	
	3/	SG1526/BVAJC	
	3/	IP1526J/883B	
85515012A	01295	UC1526L/883B	
	34333	SG1526BL-DESC	
8551502VA	01295	UC1526AJ/883	
	3/	IP1526AJ/883B	
85515022A	01295	UC1526AL/883B	

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated Semiconductor Group 8505 Forest Lane P.O. Box 660199 Dallas, TX 75243
34333	Microsemi Analog Mixed Signal Group 11861 Western Avenue Garden Grove, CA 92841-2119