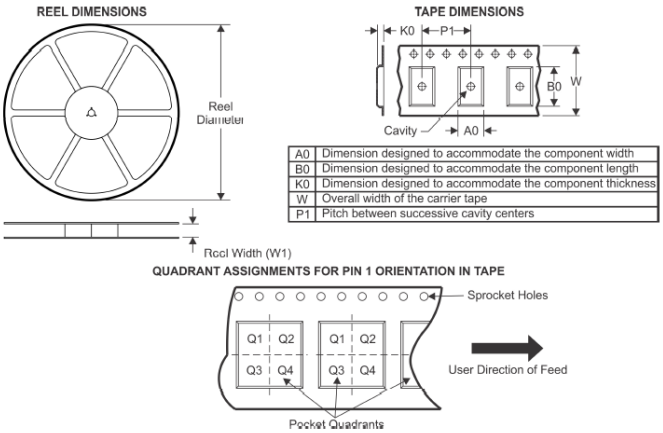
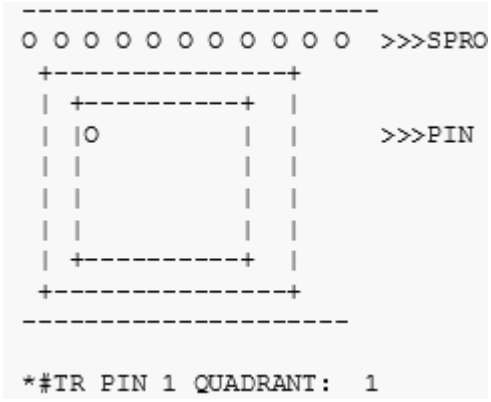
TAPE AND REEL INFORMATION





Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP8557IAYFQR	DSBGA	YFQ	16	3000	178.0	8.4	1.85	2.01	0.76	4.0	8.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP8557IAYFQR	DSBGA	YFQ	16	3000	210.0	185.0	35.0

Marking picture	vendor Name	Part No.	Marking Rule
D41	TI	LP8557IAYFQR	the marking " D41" represents the device name, by identifying units marking D41 correctly to determine device

Component	Homogeneous Material Name.	Substance Name	*CAS No.	Substance Mass. (mg)	Percentage %
Back Side Coating	Other Inorganic Materials	Fused Silica	60676-86-0	0.177772	78.1
	Other Plastics and Rubber	Carbon Black	1333-86-4	0.001821	0.800014
	Other Plastics and Rubber	Other Filler		0.004097	1.799922
	Thermoplastics	Epoxy	85954-11-6	0.043931	19.300065
Solder Bump	Copper and Its Alloys	Copper	7440-50-8	0.004815	0.499963
	Nickel and Its Alloys	Nickel	7440-02-0	0.000482	0.050048
	Other Nonferrous Metals and Alloys	Tin	7440-31-5	0.946218	98.249975
	Precious Metals	Silver	7440-22-4	0.011557	1.200014
Semiconductor Device	Ceramics / Glass	Doped Silicon	7440-21-3	2.244212	100

Basic Information	**Result**
Device Part Number	LP8557IAYFQR
Wafer fab information, process type and node	Aizu/MFAB, CMOS9
Wafer process was qualified and released to production or not.	Mature
Products have been applied with this wafer process?	Yes
Is there any part from the same wafer process family have been used in customer?	YES
Wafer Process Capability(SPC)	Meet SPC Spec
Is there any wafer process CPK<1.33? If yes, please list it and provide the improvement plan.	NO
Chip ID:Do you have chip ID or die ID for this device?	NO
Assembly Factory, Package type	TIEM WCSP
Package Size (Length*Width*Height)	1.8x1.8x0.68mm
Ball/Lead pitch	0.4MM
Is there any part from the same package family have been used in customer? If yes, please list the part number.	YES

Assembly Process Capability(SPC)		Meet spc spec
Is there any assembly process CPK<1.33? If yes, please list it and provide the improvement plan.		NO
Range of Operation Temperature （Ta, Tj or Tc）		-30~85°C
Storage Temperature range		-65 ~ 150°C
Storage limit		1years at customer side
Max.Junctioin Temperature		-30~125°C
IFR, Intrinsic Failure Rate, FIT		1.8FIT@60%CL
MSL, Moisture Sensitive Level		MSL 1
Theta ja, jc and jb	Θja	75.7°C/W
	Θjc	0.5 °C/W
	Θjb	16.2°C/W
ESD (HBM、CDM, for all pin)	HBM	2000
	CDM	500
Latch-Up (At max. Ambient Temperature)		Meet qual test requirement
Test Factory		TIEM
If the chip is new process or new design, And some Lifetime limit test(Test to fail or beyond JEDEC standard) had been down. Please specify the test condition and result details.		NO
Wafer reliability Qualification Report, including: TDDB, HCI, NBTI, PBTI, EM, SM .etc		YES
Package Qualification Report, including: PC, THB, HAST, UHAST, HTSL, TC, BLTC, DT, Bend, PDT, PVT .etc		See TI.com qual report
Device Qualification Report, including: ELFR, HTOL, LTOL, ASER, SSER, ESD-HBM, ESD-CDM, LU .etc		See TI.com qual report
The device should be done reliability monitoring. Please provide the latest Reliability Monitoring Report, including: PC, THB, HAST, UHAST, TC, HTSL, HTOL .etc		ORT test based on package
Characterization report, follow JESD86		Refer to datasheet

Component information: LP8557IAYFQR		Investigation Result
Ball Compositions and ratio		SnAgCu1205
Ball Diameter(μm) before ball attachment		0.25MM
Back side laminate		Yes
Is there RDL layer in WLCSP?		Yes
Package standard		JEDEC
Weight of component (g)		3.4mg
Weight/ available P&P area≤0.06g/mm2		Yes
Is there polarity point on the top side of component?		Yes
Is the polarity point sole?		Yes
Is there any specific location number of terminals in component specification?		Yes
Component orientation can be identified by AOI?		Yes
Are matters RoHS compliant and lead free?		Yes
Are matters are Halogen-free		Yes
Storage Condition	Relative humidity (%)	≥20%&≤70%
	Temperature (℃)	≥-10C&≤35C
	Maximum storage time (month)	12Month at customer side
Packaging type		Tape and real
Position of component pin 1 in packing		Q1
Packaging height(K0)		0.76mm
Packaging width(W)		8mm
component pitch:P1		4mm
ESD packaging		Yes
Rollover rate ≤0.05% in packing		Yes
tray packing Baking conditions: 125℃@24h		Yes

reel tape packing Baking conditions: 40℃@192h	Yes
Can reel tape packing meet EIA-481 standard?	EIA
MSL	1
MSL>=2,moisture sensitive protection must include: moisture sensitive indicator card, desiccant, moisture sensitive grade logo	Yes
Baking requirement meet J-STD-033b if moisture	Yes
Maximum soldering times ≥3	Yes
Can heat resistance of SMT components meet JSTD020D. (should focus on the classification of temperature and reflow profiles, that is table 4-1, 4-2 and 5-2, please refer to sheet6 J-STD-020D in this file)	Yes
Maximum pick-and-place pressure (N)	Meet SMT pick-and-place pressure request
Whether the welding process and design requirements of component have all written to the component specifications	Yes
Whether Pad & stencil design as Mandatory requirements in component spec?	recommended
Whether the device has special requirements for the reflow temperature ramp-up rata and ramp-down rata? Customer follow J-STD-002 standard	No
Are there other mandatory requirements in component spec?	No
Solder ability shall be tested per J-STD-002D and the report must be offered,	Yes

Texas Instruments Qualification Summary

Quality and reliability are built into TI's culture, with the goal of providing customers high quality products. TI's semiconductor technologies are developed with a minimum goal of fewer than 50 Failures in Time (FIT) at 100,000 Power-On-Hours at 105C junction temperature. TI builds simulations, accelerated testing, and robustness evaluations into the product development process. During the product development process, TI carefully assesses silicon process reliability, package reliability, and silicon/package interaction.

TI also evaluates manufacturability of the device to verify a robust silicon and assembly flow to enable continuity of supply to customers. Non-Automotive devices are qualified with industry standard test methodologies performed primarily to the intent of the Joint Electron Devices Engineering Council (JEDEC). TI qualifies new devices, significant changes, and product families based on JEDEC JESD47. The data shown is representative of the material sets, processes, and manufacturing sites used by the device family.

Stress	Reference	Min lot qty	SS / lot	Condition	Duration	Result
HTOL	JESD22-A108	3	77	Life test, 125C	1000 hours	Pass
HTSL	JESD22-A103	3	25	High temp storage ba ke 150C	1000 hours	Pass
AC/UHAST	JESD22-A102/JESD2 2-A118	3	25	Autoclave 121C or un biased HAST 130C / 8 5% RH	96 hours	Pass
THB/HAST	JESD22-A101/JESD2 2-A110	3	25	THB 85C/85%RH or H AST 130C/110C/85% RH	1000 hours or 96 hou rs	Pass
TC	JESD22-A104	3	25	Temperature cycle -6 5/150C	500 cycles	Pass
SD	J-STD-002	3	22	Per specification	>95% lead coverage	Pass
HBM	JS-001	1	3	ESD - HBM	Classification	See data sheet
CDM	JESD22-C101	1	3	ESD - CDM	Classification	See data sheet
LU	JESD78	1	3	Latch-up	Per JESD78	Pass
MSL	J-STD-020	—	—	Per J-STD-020	Classification	See data sheet

TI reference number:17228719