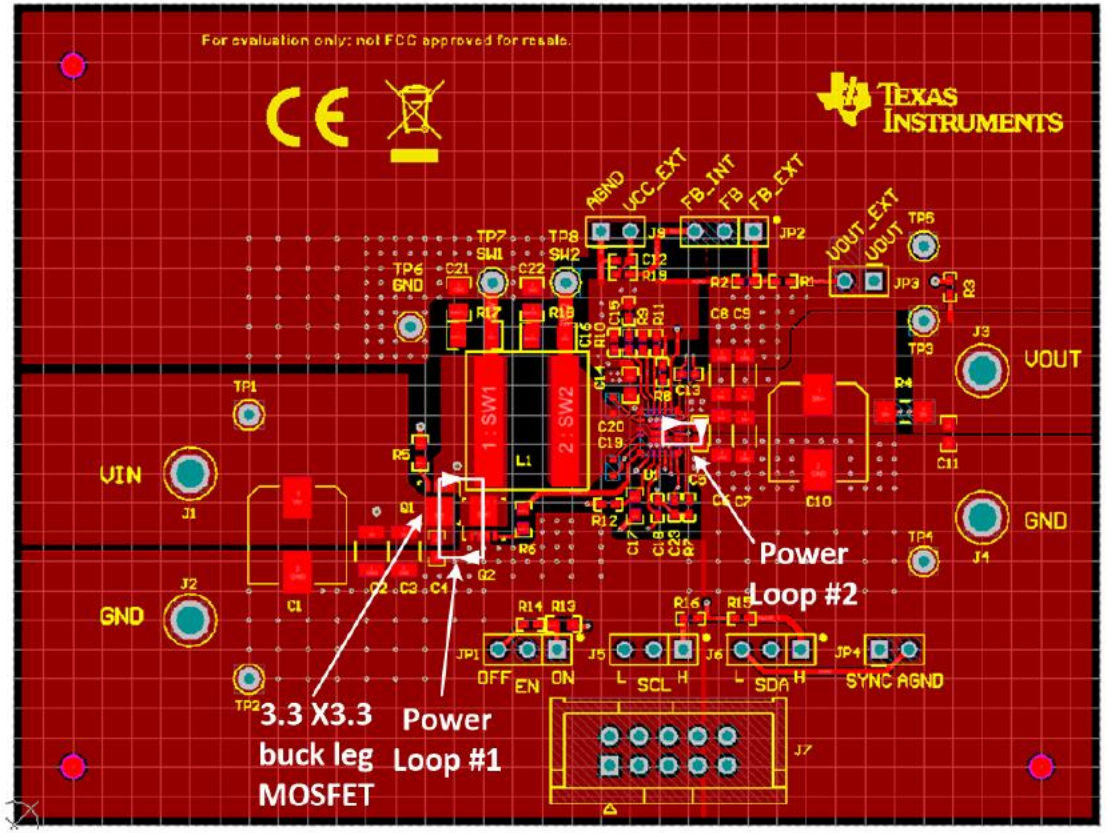
TPS55288 EVM Layout Guideline

SR-BCC

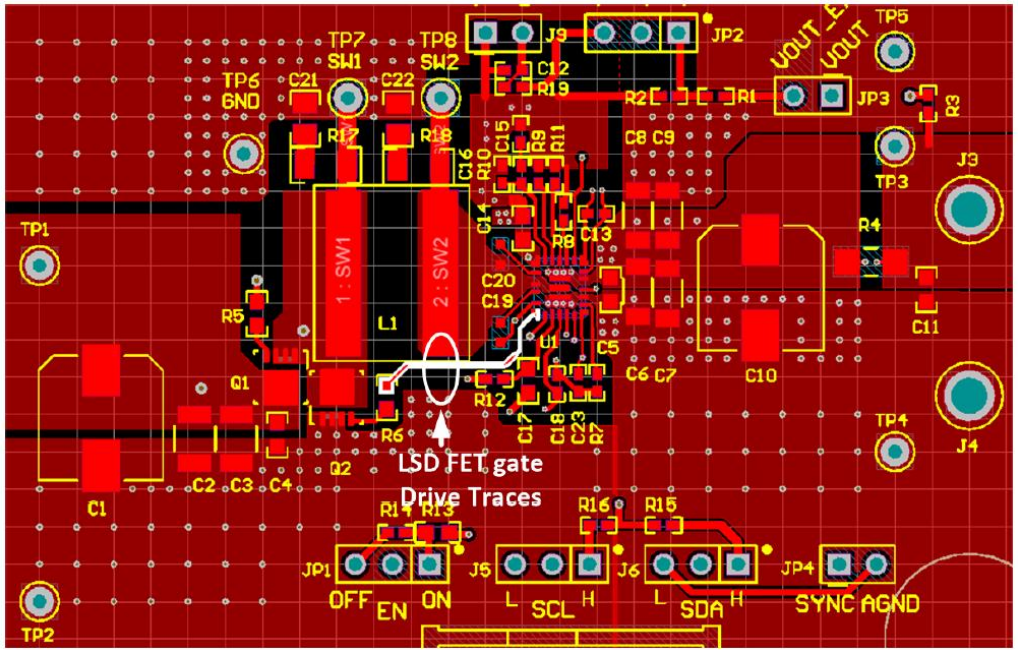
Sep, 2024

Power Components Placement

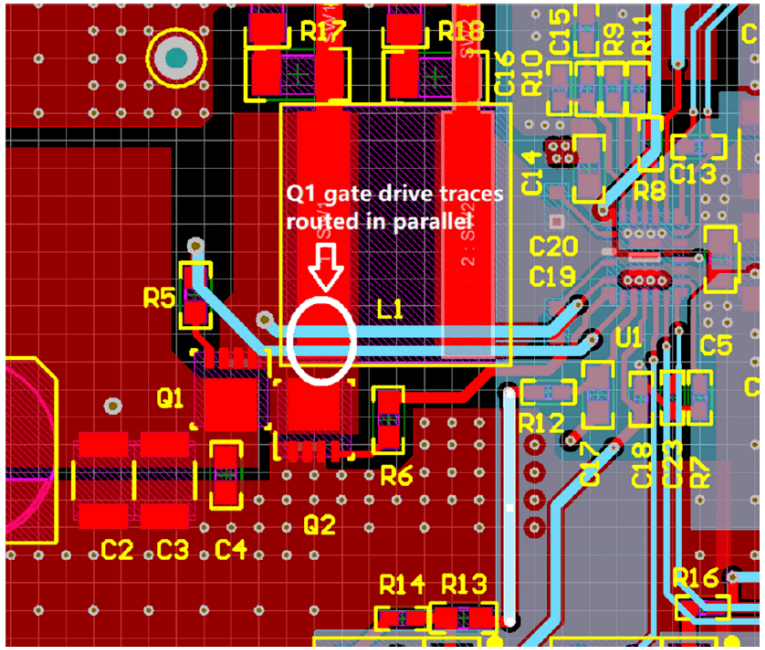


1. Input capacitors are placed close to the buck-leg MOSFETs.
2. Output capacitors are placed adjacent to the TPS55288's VOUT pin and PGND pin.
3. The main inductor L1 is placed between the buck-leg MOSFETs and the TPS55288 silicon. The SW node is poured with small copper plane.

Driver Circuit Routing



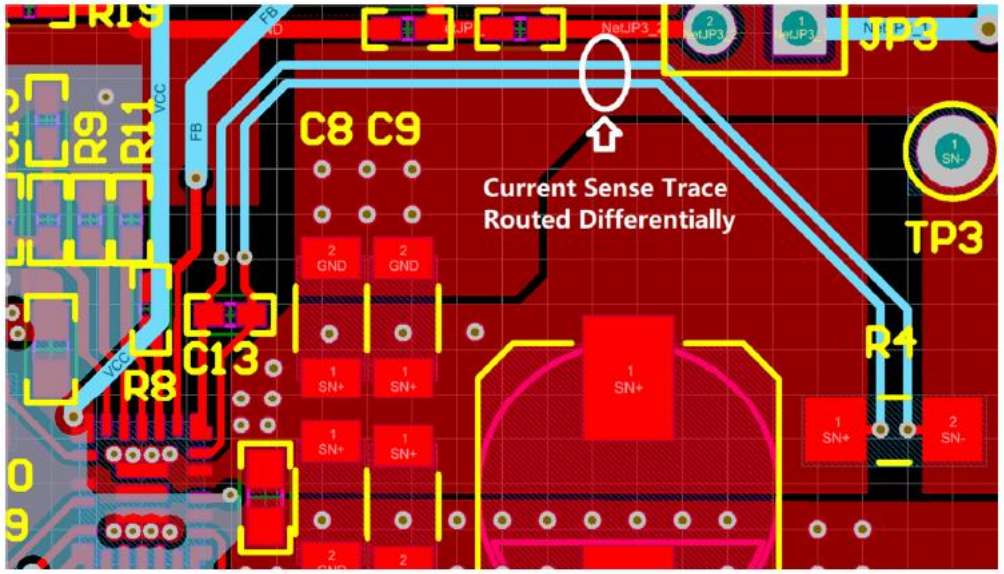
Low-Side-FET Drive Traces Routing



High-Side-FET Drive Traces Routing

1. Kelvin – connecting the gate drive return traces directly to the respective MOSFET sources minimize common-source inductance. To minimize gate-loop area, gate and source traces are routed side by side as differential pairs.
2. The gate drive resistors should be placed close to the gate terminal of each MOSFET.

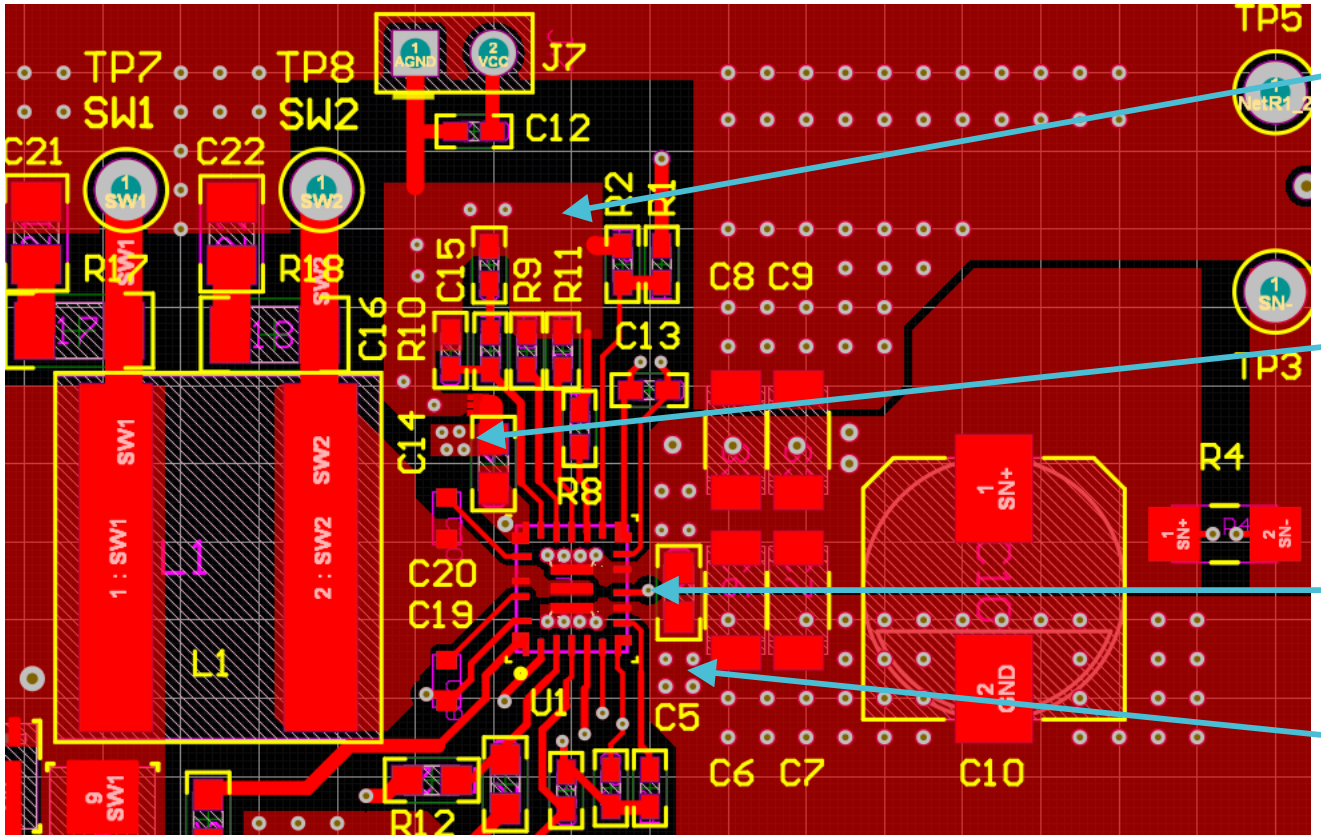
Output Current Sense Traces Routing



Output-Current-Sense Traces Routing

1. The traces were routed as a tightly-coupled differential pair from the shut resistor to the IC, which can enhance the noise immunity and the accuracy. Place the current-sense filter capacitor close to the IC.

AGND-PGND Connection



GND copper plane for the FB network and the compensation network – small island, separate with the power GND at top layer.

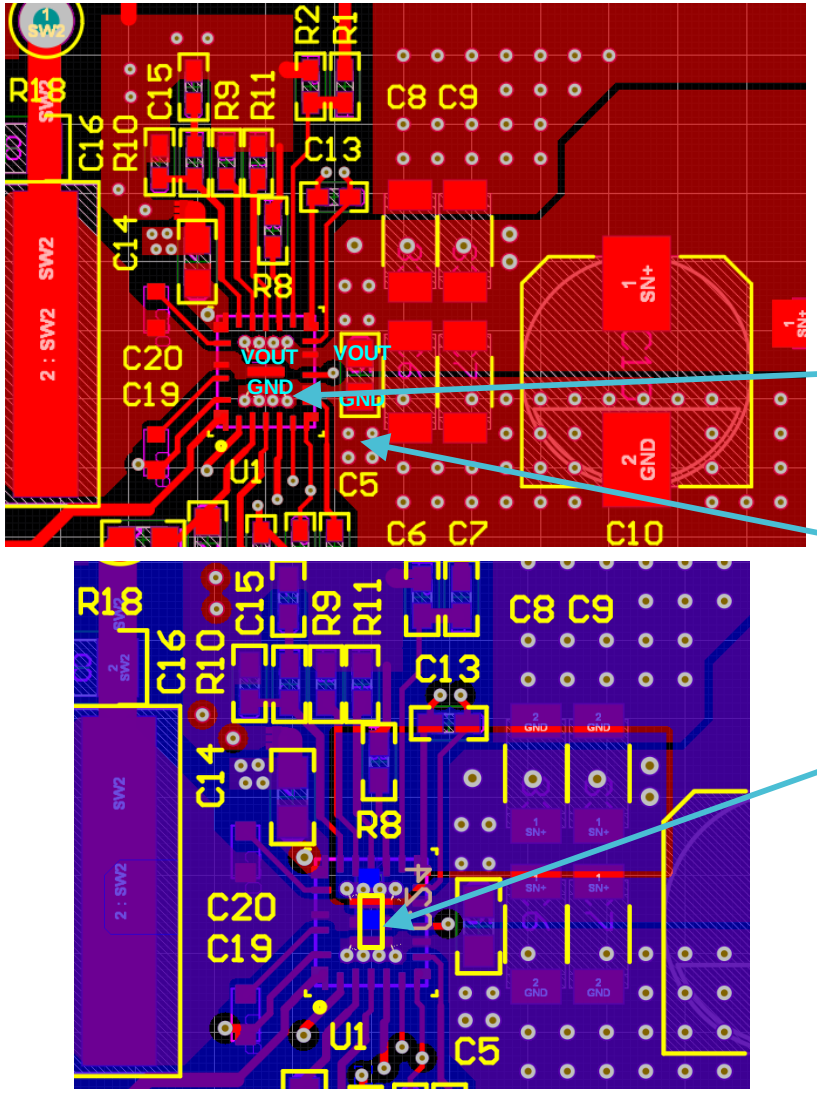
Add 3-4 vias around the GND net of the VCC cap.

The VCC capacitor should be placed as close to the IC as possible.

AGND and PGDN pour separately.

Add enough vias around the output cap.

Power and GND Plane Design



1. Place a whole layer GND copper plane under the switching loops establish a passive shielding for the circuit. -> EMI
2. Add thermal vias beneath the TPS55288 connecting PGND pin and VOUT pin to the PGND plane and a large VOUT area separately. -> Thermal
3. Add more vias close to VOUT pin and PGND pin to connect with VOUT plane and PGND plane separately.
4. Add one 0.1uF/0402 cap at the bottom layer to minimize the Boost power loop.