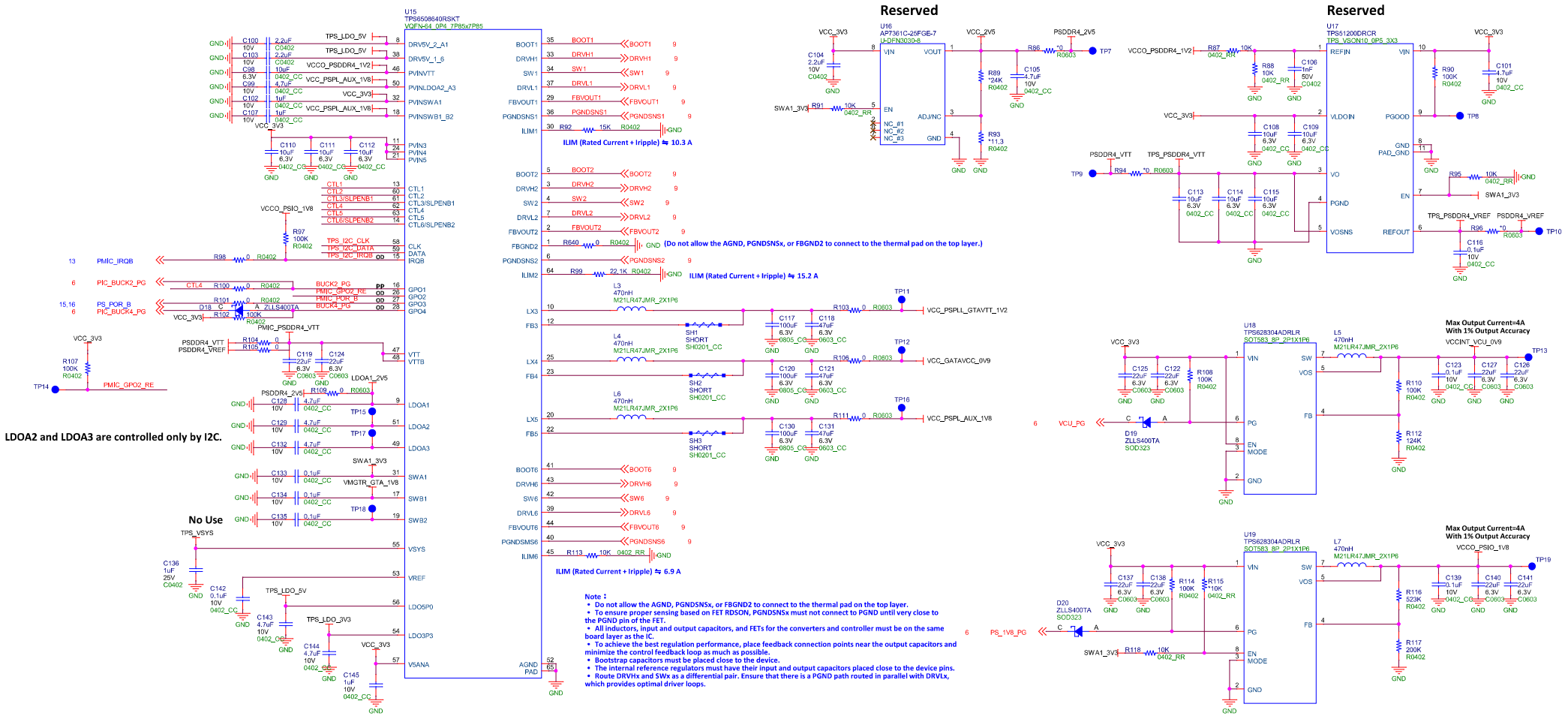
PMIC



Alternatively, the GPOs can be used as general purpose outputs controlled by the user through I2C. Refer to Section 8.13.37 for details on controlling the GPOs in I2C control mode. When configured as push-pull, LDO3P3 is used for logic-level high.

Name	Pin Function	Voltage configuration settings		
CTL1	DDR_EN	CTL1=0	LDOA1=0	
		CTL1=1	LDOA1=2.5V	
CTL2	DDR_SEL	CTL1=0	BUCK6=0V	
		CTL1=1	CTL2=0	BUCK6=1.2V
			CTL2=1	BUCK6=1.35V
CTL3	Main Sequence	CTL3=0	Disable	
		CTL3=1	Enable	
CTL4	VCCINT_PG (BUCK 1)	CTL4=0	Disable	
		CTL4=1	Enable	
CTL5	VTT EN	CTL1=0	CTL5=0	Disable
		CTL1=1	CTL2=0, CTL5=1	0.6V
			CTL2=1, CTL5=1	0.675V
CLT6	BUCK2_SEL	CTL6=0	BUCK2=0.85V	
		CTL6=1	BUCK2=0.9V	

Slew Rate

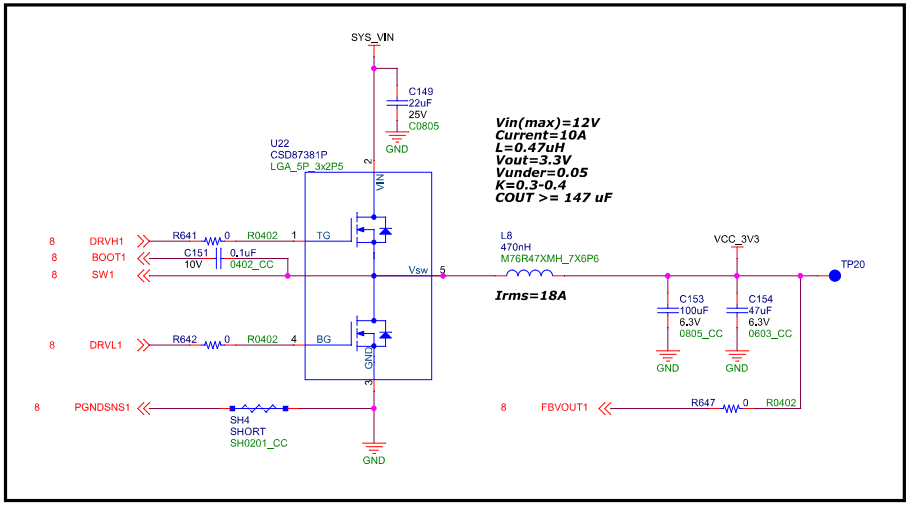
DV/DT	MODE	Slew Rate
Float	Float	3.8 V/ms

Limit Current

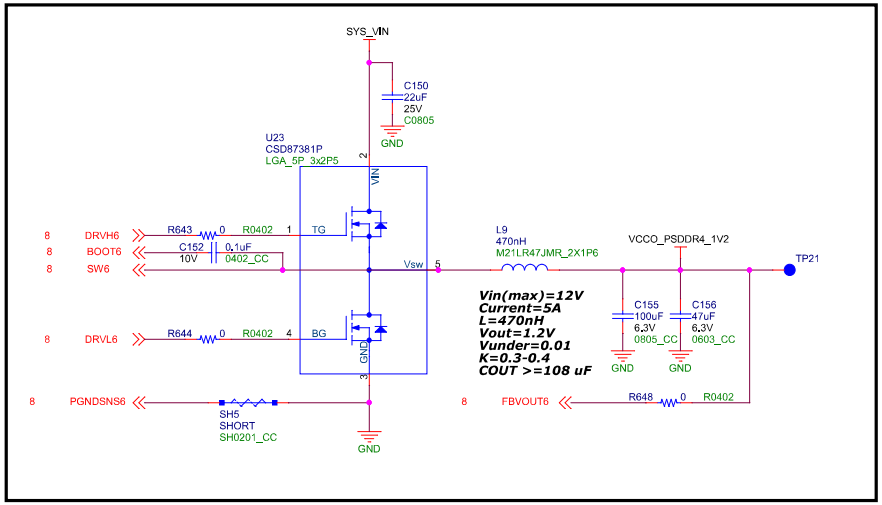
ILIMIT	Limit current
Float	2.5 A

PMIC

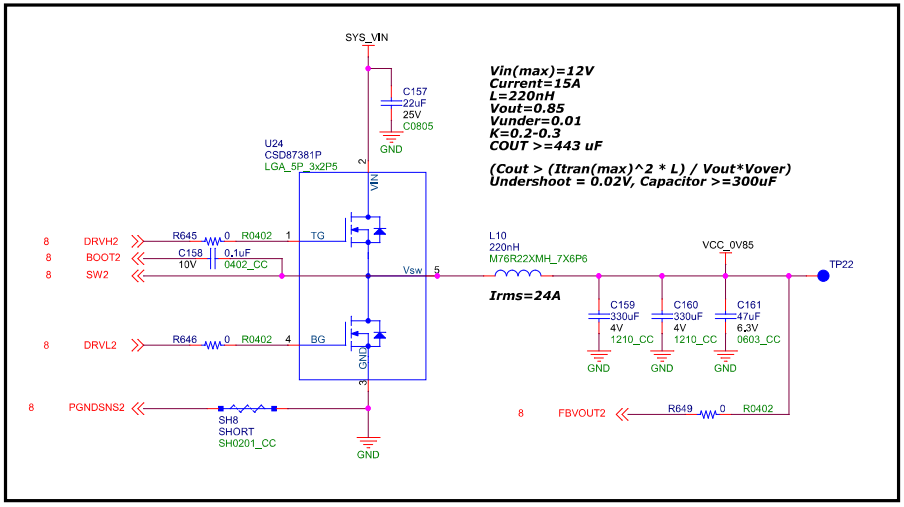
BUCK #1



BUCK #6

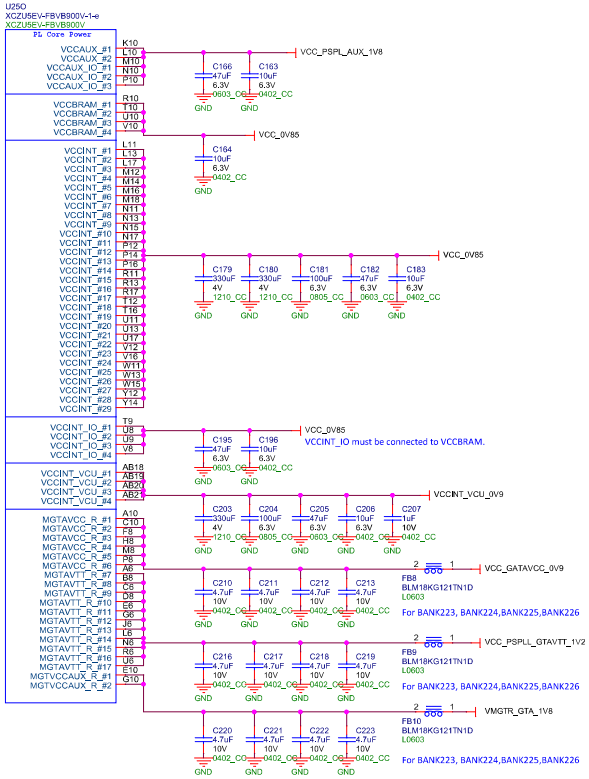


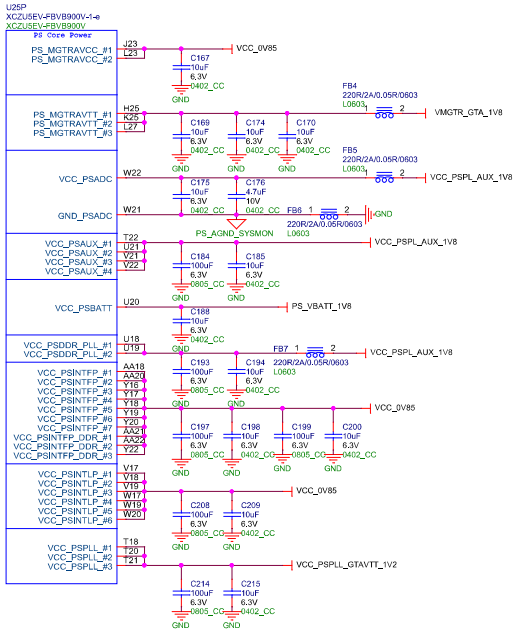
BUCK #2

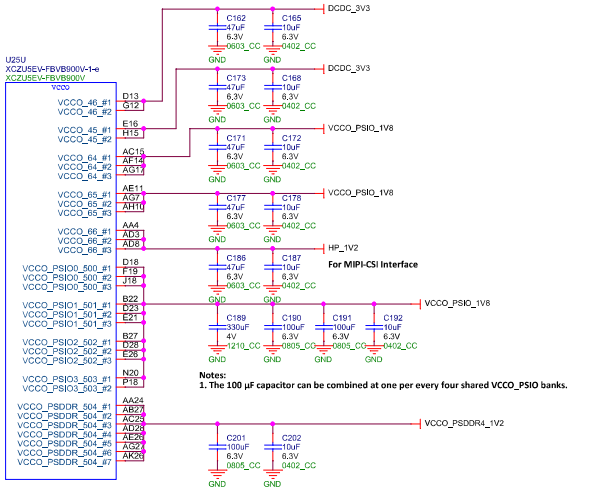


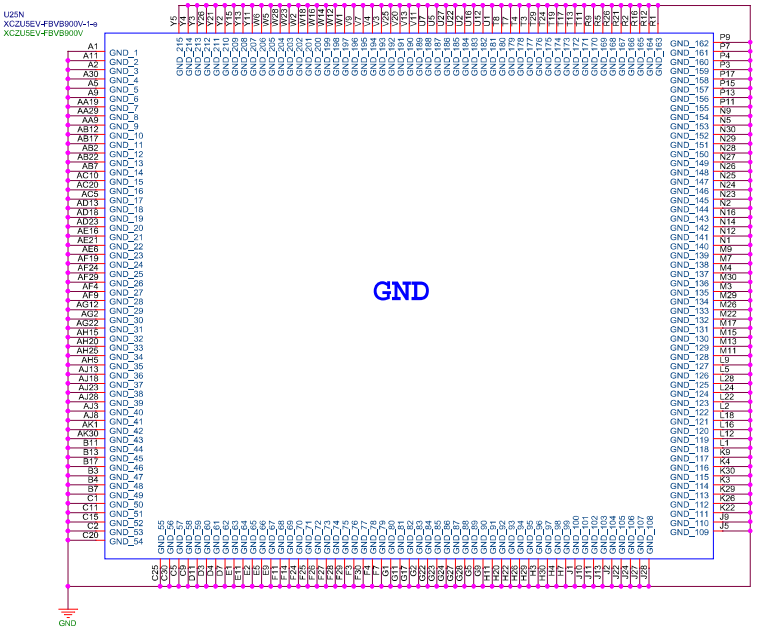
Part Number	Vds	Vgs	Id	Package	Remark
CSD85301Q2	20V	10V	5A	3X2.5 LGA	
CSD87331Q3D	30V	8V	15A	3.3X3.3 SON	
CSD87381P	30V	8V	15A	3X2.5 LGA	No Airflow = 15A With Airflow (200 LFM) = 20A With Airflow + Heat Sink = 25A
CSD87588N	30V	16V	25A	5X2.5 LGA	No Airflow = 25A With Airflow (200 LFM) = 30A With Airflow + Heat Sink = 35A
CSD87350Q5D	30V	8V	40A	5X6 SON	

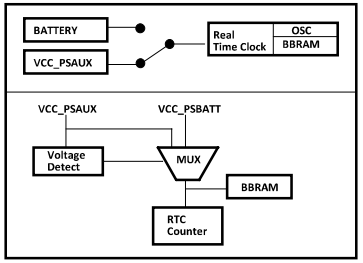
AMD Xilinx - PWR











Zynq UltraScale+ MPSoC Decoupling Capacitor Recommendations (UG583)

	VCCINT/VCCINT_IO				VCCBRAM/VCCINT_IO		VCCAUX/VCCAUX_IO		HDIO/HPIO (per bank)	
	330uF	100uF	47uF	10uF	47uF	10uF	47uF	10uF	47uF	10uF
XCZU4EV-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU5EV-FBVB900	1	4	1	1	1	1	1	1	1	1
XCZU7EV-FBVB900	1	4	1	1	1	1	1	1	1	1

1. Connect VCCINT and VCCINT_IO together on the PCB for -3, -2, and -1 speed grades. The capacitors listed are the total number of capacitors for the combined rail.
2. Connect VCCBRAM and VCCINT_IO together on the PCB for -2L and -1L speed grades. The capacitors listed are the total number of capacitors for the combined rail.
3. VCCAUX and VCCAUX_IO must share the same plane on the PCB. The capacitors listed are the total number of capacitors for the combined rail.
4. The 47 µF capacitor can be combined at one per every four shared HDIO/HPIO banks.

Zynq UltraScale+ MPSoC PS Decoupling Capacitor Recommendations (UG583)

	VCC_PSINTFP		VCC_PSINTLP		VCC_PSAUX		VCC_PSPLL		VCC_PSINTFP_DDR		VCCO_PSIOx		VCCO_PSDDR		VCC_PSBATT	
	100uF	10uF	100uF	10uF	100uF	10uF	100uF	10uF	100uF	10uF	100uF	10uF	100uF	10uF	10uF	
XCZU5EV-FBVB900	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Notes:
1. The 100 µF capacitor can be combined at one per every four shared VCCO_PSIO banks.
2. For PS_MGTRAVCC and PS_MGTRAVTT use one 10 µF capacitor each. See Chapter 4, PCB Guidelines for the PS Interface in the Zynq UltraScale+ MPSoC.

VCCINT_VCU Decoupling Guidelines for Zynq UltraScale+ MPSoC XC Devices (UG583)

	VCCINT_VCU				
	330uF	100uF	47uF	10uF	1uF
XCZU5EV-FBVB900	1	1	1	1	1

GTH Transceiver PCB Capacitor Recommendations (UG576)

Quantity Per Group			Capacitor	Tolerance	Type
MGTAVCC	MGTAVTT	MGTVCCAUX			
1	1	1	4.7uF	±10%	Ceramic

Note:
For optimal performance, power supply noise must be less than 10 mVpp.