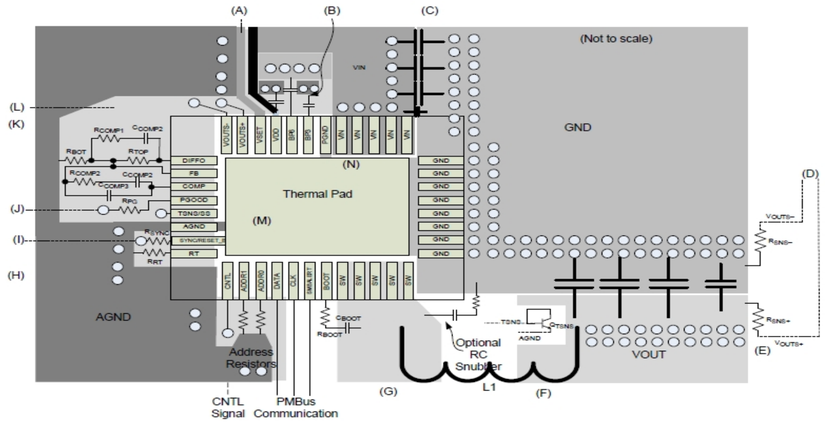
66AK2H14 ARM+DSP
Smart Reflex
0.8V – 1.1V

LAYOUT NOTES:

Place the LM10011 close to the regulator feedback pin to minimize the FB trace length.

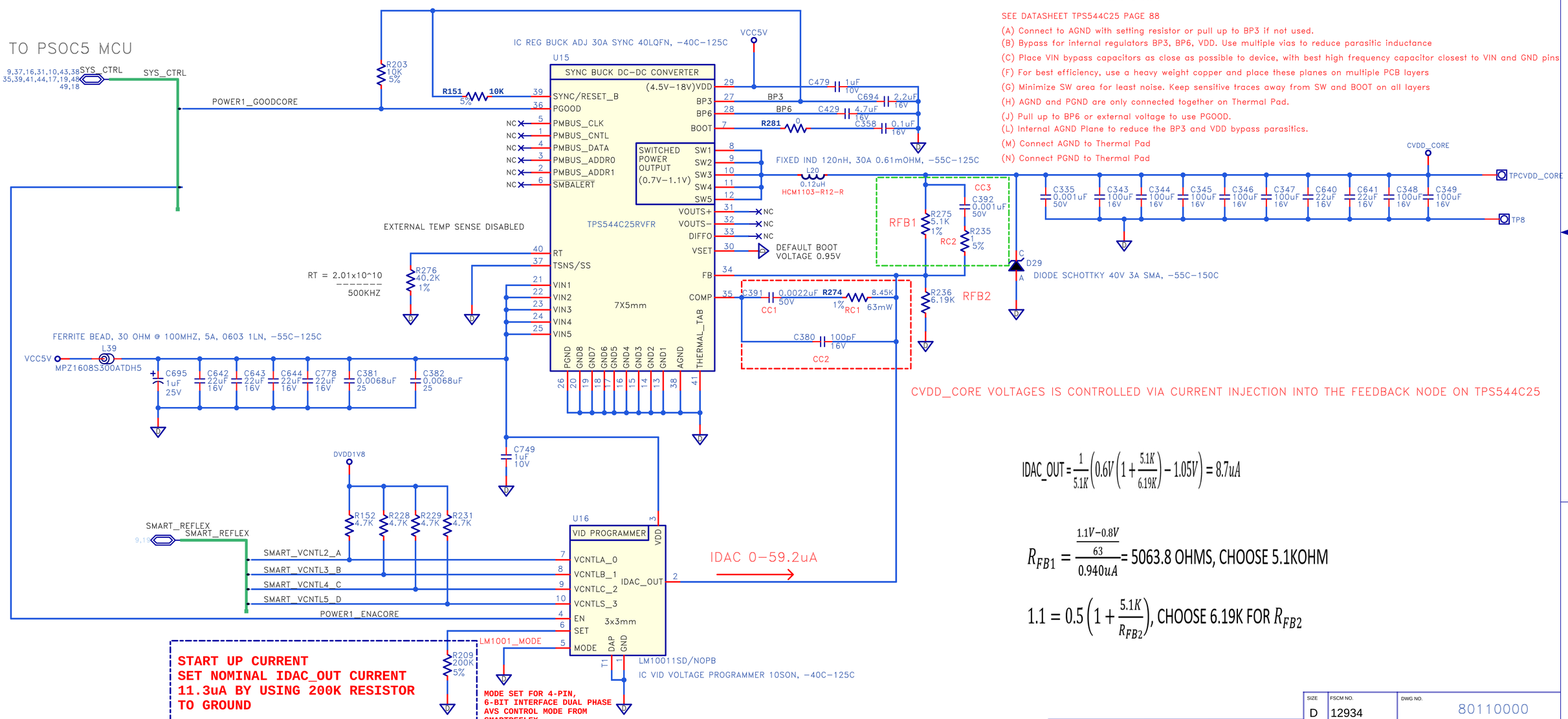
The high–current path from the board input to the load and the return path should be parallel and close to each other to minimize loop inductance.

The ground connections for the various components around the LM10011 should be connected directly to each other, and to the LM10011 GND pins, and then connected to the system ground at one point. Do not connect the various component grounds to each other through the high–current ground line.



SEE DATASHEET TPS544C25 PAGE 88

(A) Connect to AGND with setting resistor or pull up to BP3 if not used.
(B) Bypass for internal regulators BP3, BP6, VDD. Use multiple vias to reduce parasitic inductance
(C) Place VIN bypass capacitors as close as possible to device, with best high frequency capacitor closest to VIN and GND pins
(F) For best efficiency, use a heavy weight copper and place these planes on multiple PCB layers
(G) Minimize SW area for least noise. Keep sensitive traces away from SW and BOOT on all layers
(H) AGND and PGND are only connected together on Thermal Pad.
(J) Pull up to BP6 or external voltage to use PGOOD.
(L) Internal AGND Plane to reduce the BP3 and VDD bypass parasitics.
(M) Connect AGND to Thermal Pad
(N) Connect PGND to Thermal Pad



CVDD_CORE VOLTAGES IS CONTROLLED VIA CURRENT INJECTION INTO THE FEEDBACK NODE ON TPS544C25

$$IDAC\_OUT = \frac{1}{5.1K}\left(0.6V\left(1+\frac{5.1K}{6.19K}\right)-1.05V\right) = 8.7uA$$

$$R_{FB1} = \frac{\frac{1.1V-0.8V}{63}}{0.940uA} = 5063.8\ \text{OHMS, CHOOSE 5.1KOHM}$$

$$1.1 = 0.5\left(1+\frac{5.1K}{R_{FB2}}\right), \text{CHOOSE 6.19K FOR } R_{FB2}$$

SIZE D	FSCM NO. 12934	DWG NO. 80110000	
NEEDS COMPLETING	Rev AAAA	08/16/2018:10:07	SHEET 16 OF 50