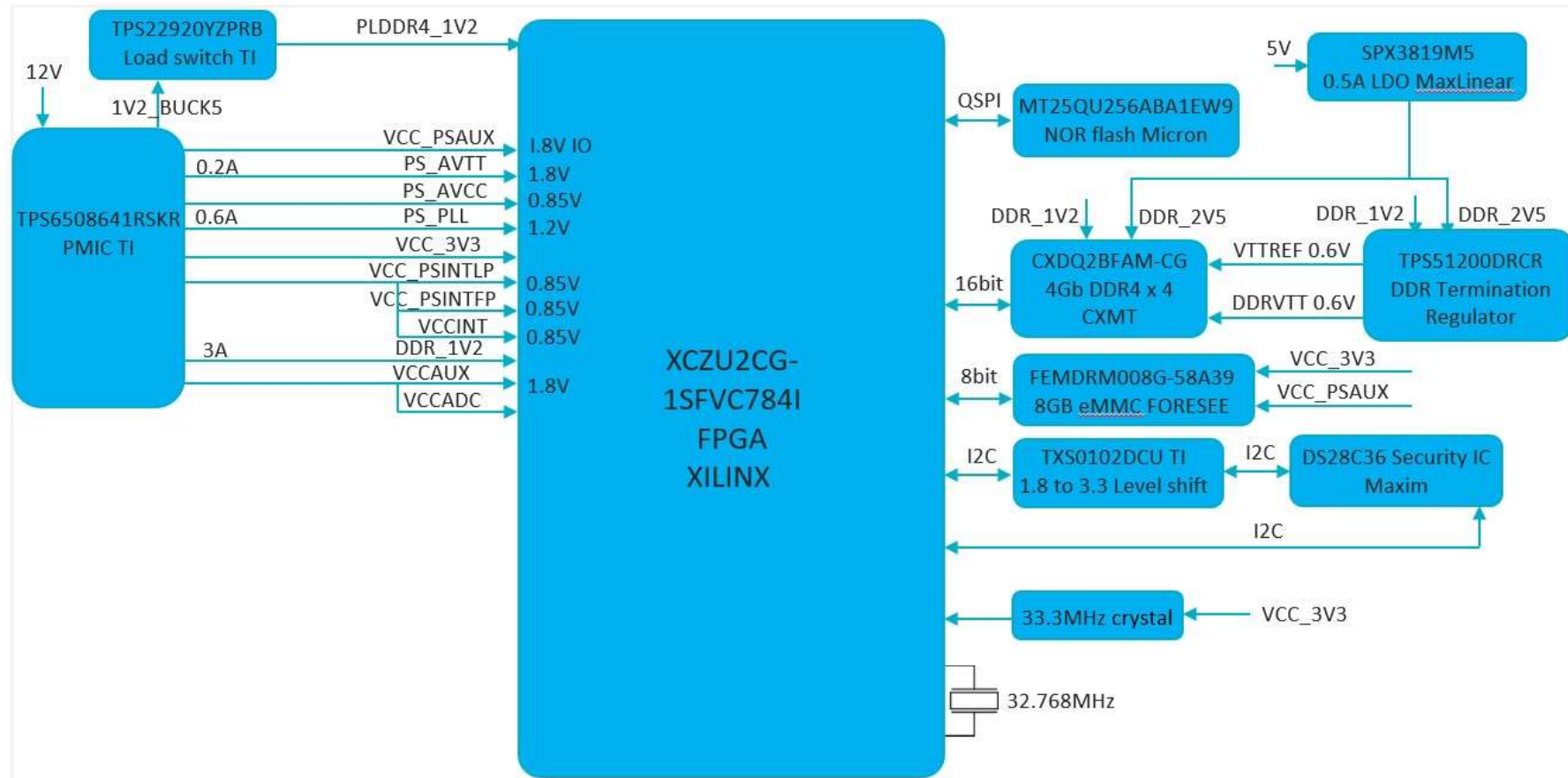


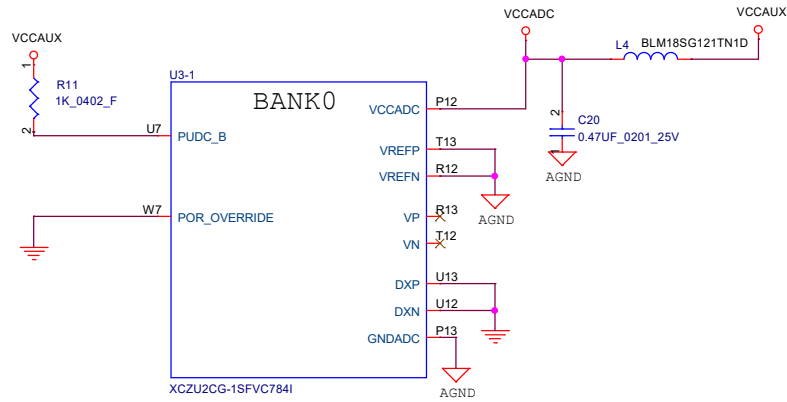
<b>Compal Electronics, Inc./SDBG</b>			
Title	SCHEMATIC, M/B GA-641 (Block Diagram)		
Size	Document Number	601K39	Rev
A3			B1
Date:	Monday, March 04, 2024	Sheet	3 of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

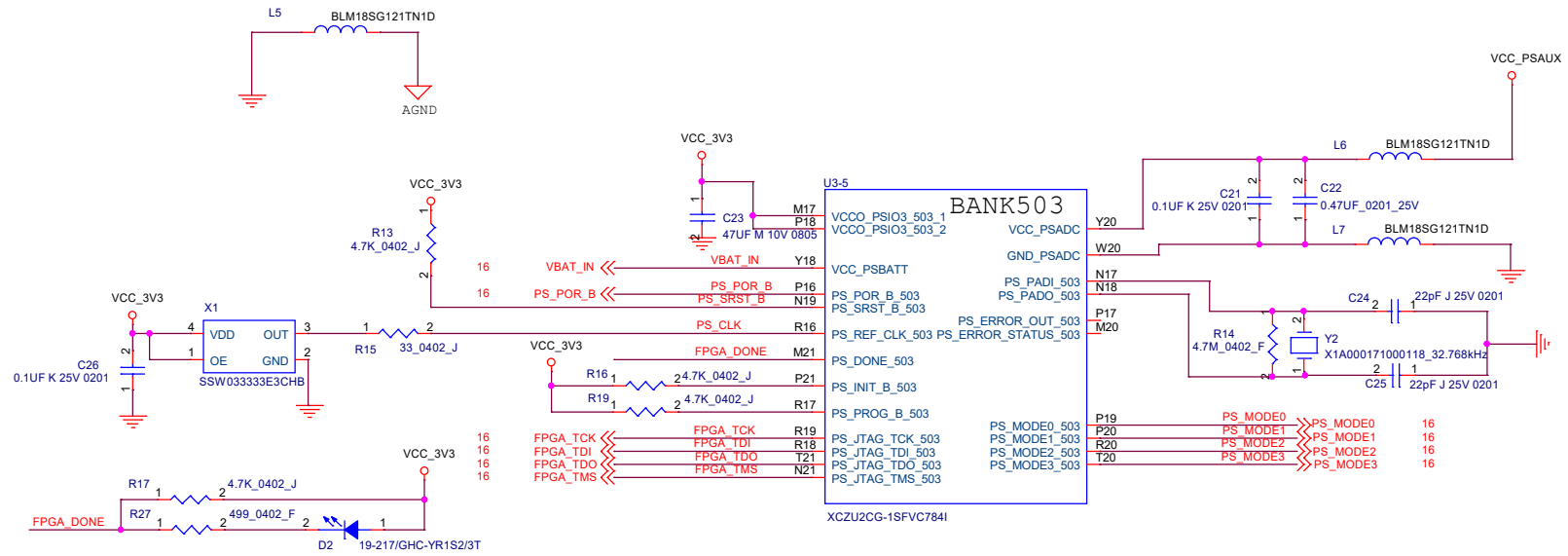


THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>			
Title	SCHEMATIC, M/B GA-641 (Power Tree)		
Size	Document Number	601K39	Rev BI
A3	Date:	Monday, March 04, 2024	Sheet 4 of 17



MODE[3:0]	BOOT MODE	Description
0000	PS JTAG	PS JTAG Interface
0001	Quad_SPI (24b)	24-Bit addresssing (QSPI24)
0010	Quad_SPI (32b)	32-Bit addresssing (QSPI32)
0011	SD0 (2.0)	SD2.0
0100	NAND	Requires 8-bit data bus width
0101	SD1 (2.0)	SD2.0
0110	eMMC (1.8V)	eMMC version 4.5 at 1.8V
0111	USB0 (2.0)	USB 2.0 only
1000	PJTAG (MIO #0)	PJTAG connection 0 option
1001	PJTAG (MIO #1)	PJTAG connection 1 option
1110	SD1 LS (3.0)	SD 3.0

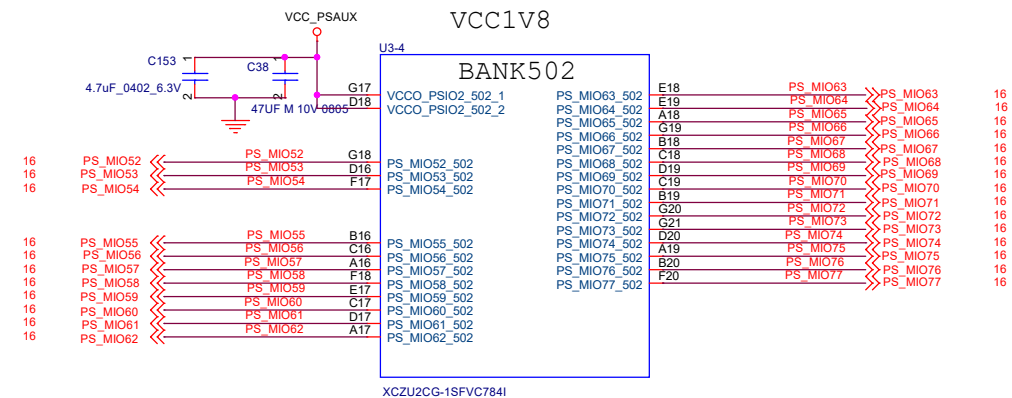
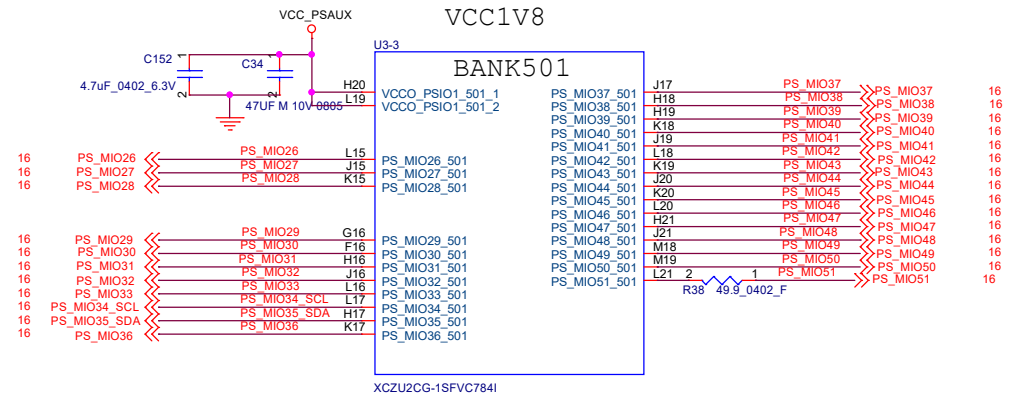
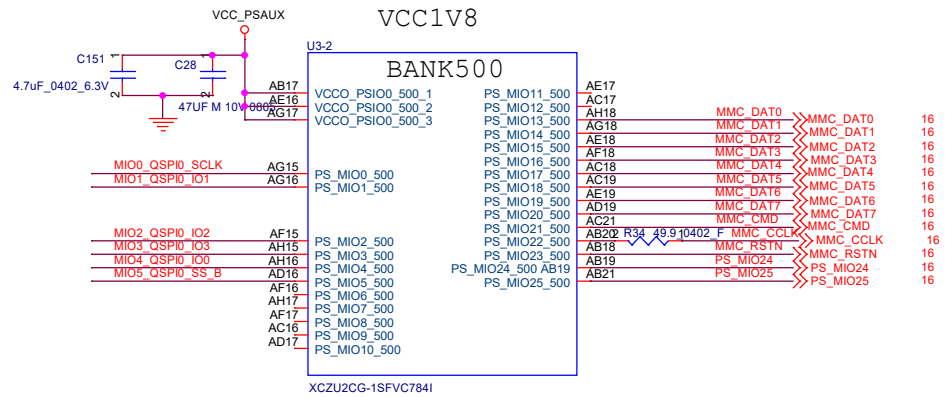
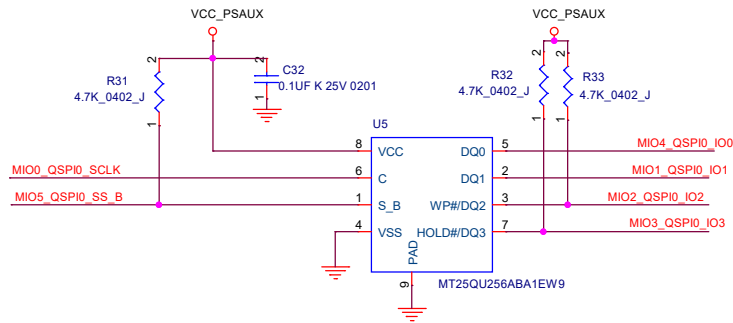


**Compal Electronics, Inc./SDBG**

**SCHEMATIC, M/B GA-641 (DBB-2)**

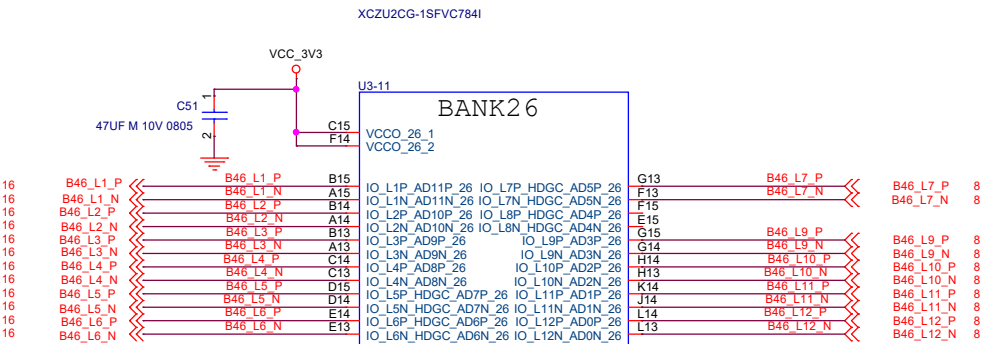
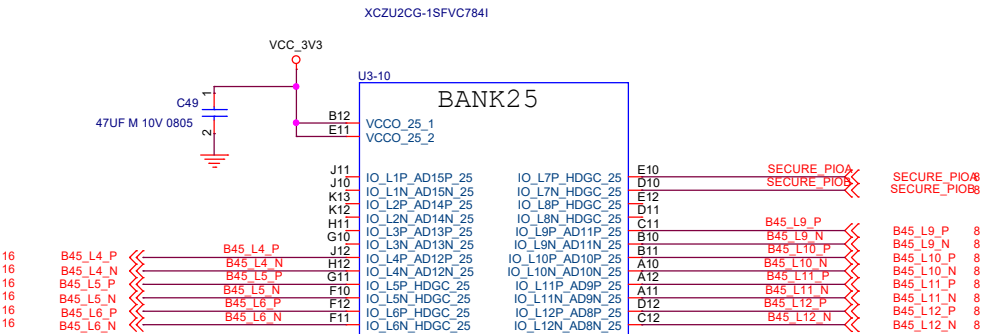
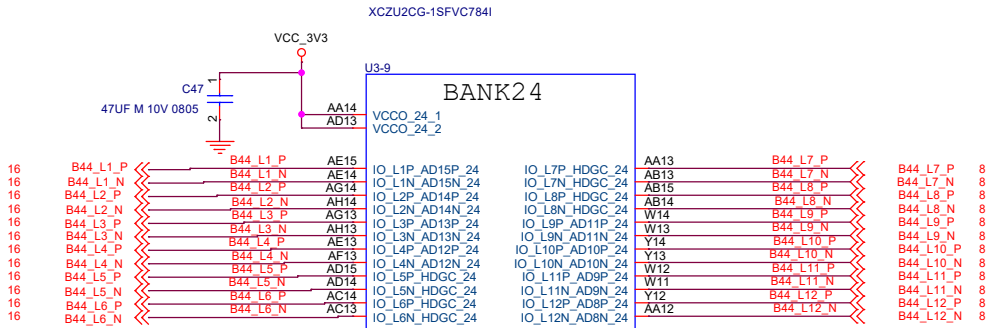
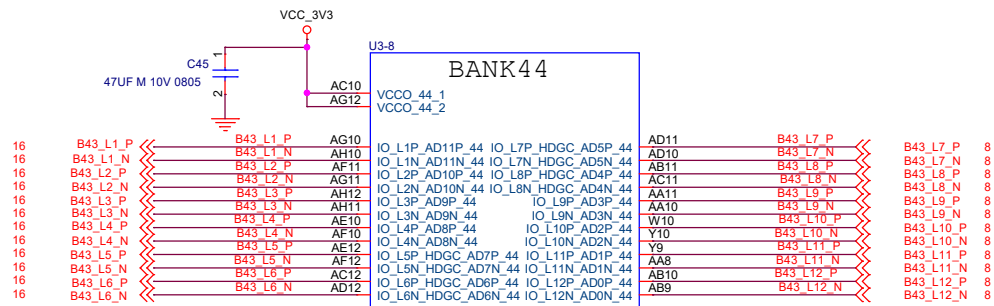
File	Document Number	Rev
	<b>601K99</b>	
Date	Murphy, March 04, 2024	Sheet 9 of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION (S) AND DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINED HEREIN BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSMITTED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>		
Title <b>SCHEMATIC, M/B GA-641 (DBB-2)</b>		
Size <b>A3</b>	Document Number <b>601K39</b>	Rev <b>BI</b>
Date: <b>Monday, March 04, 2024</b>	Sheet <b>6</b>	of <b>17</b>



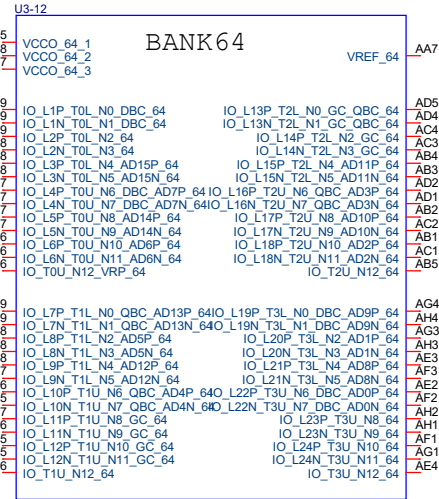
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

**Compal Electronics, Inc./SDBG**

Title: SCHEMATIC, M/B GA-641 (DBB-3)

Size: A3 Document Number: 601K39 Rev: B1

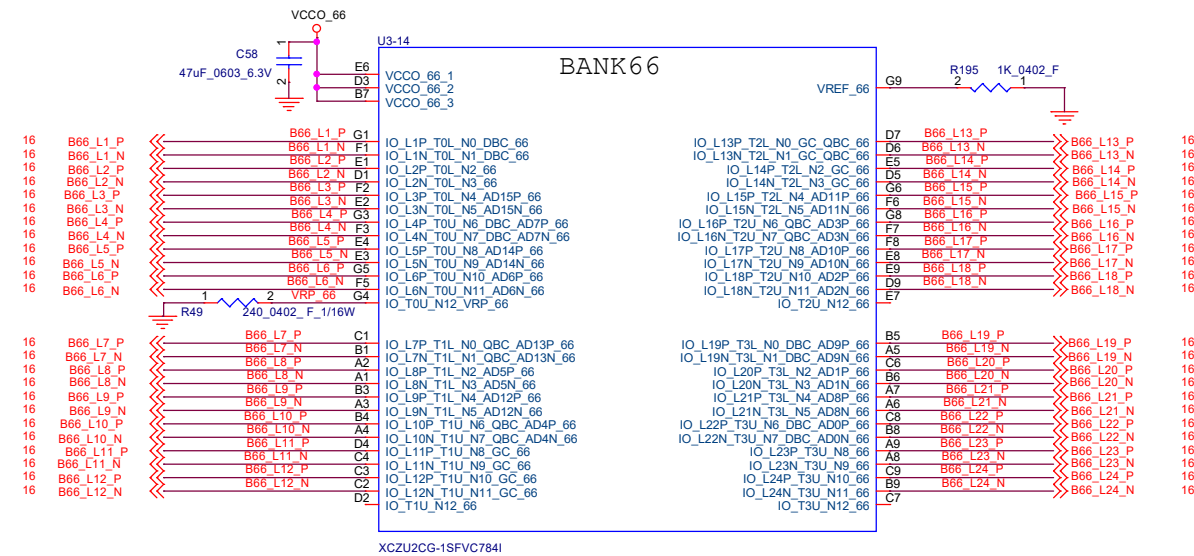
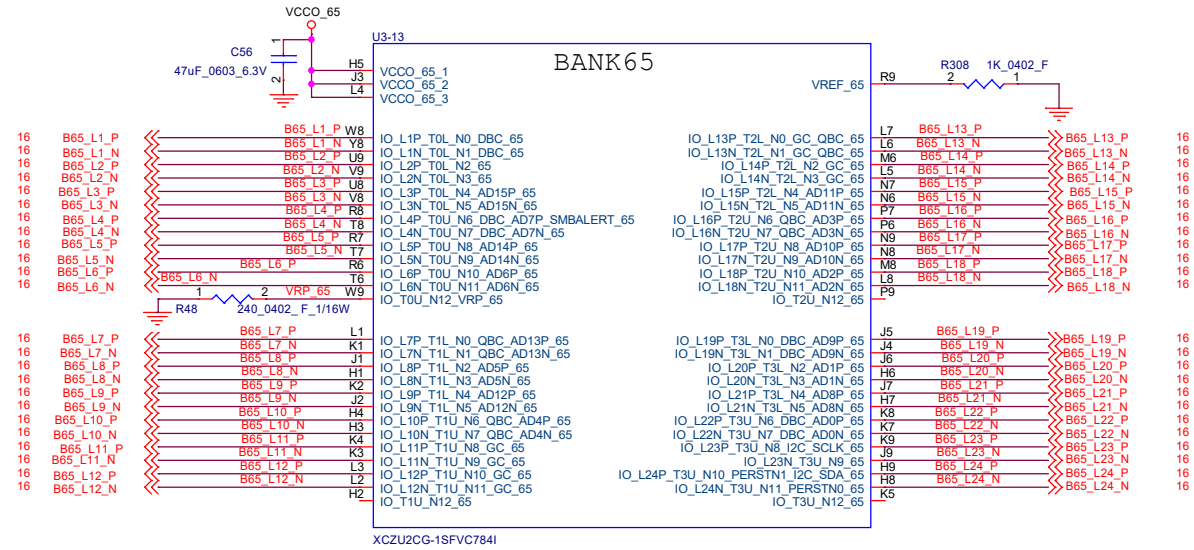
Date: Monday, March 04, 2024 Sheet: 7 of 17



XCZU2CG-1SFVC7841

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

Compal Electronics, Inc./SDBG			
Title	SCHEMATIC, M/B GA-641 (DBE3)		
Size	Document Number	601K39	Rev
A3			B1
Date:	Monday, March 04, 2024	Sheet	8 of 17



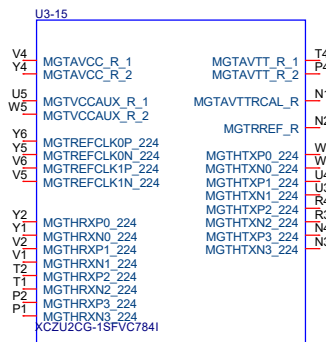
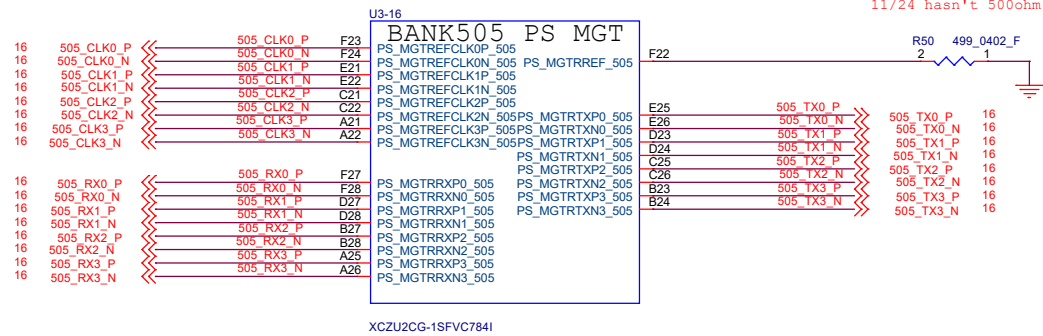
**Compal Electronics, Inc./SDBG**

File: SCHEMATIC, M/B GA-641 (P/R/C)

Size: A3 Document Number: 601K39 Rev: 31

Date: Monday, March 04, 2008 8:58:58 AM 5 of 107

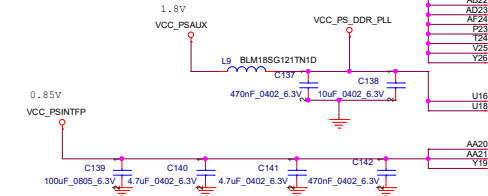
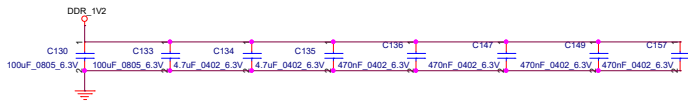
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



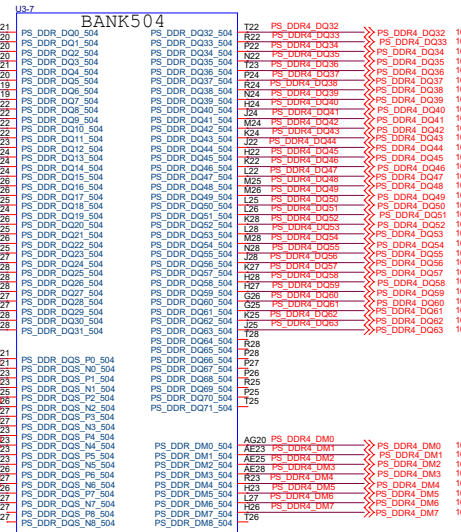
<b>Compal Electronics, Inc./SDBG</b>			
SCHEMATIC, M/B GA-641 (MEMORY-1)			
Size	Document Number	Rev	
A3	601K39	BI	
Date:	Monday, March 04, 2024	Sheet	10 of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

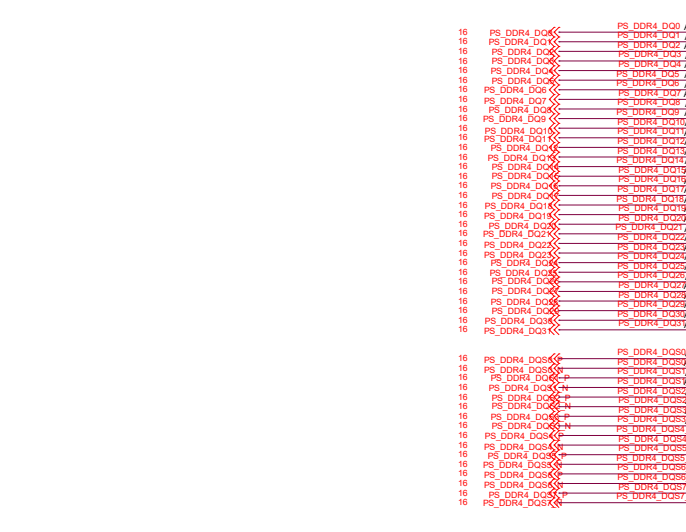


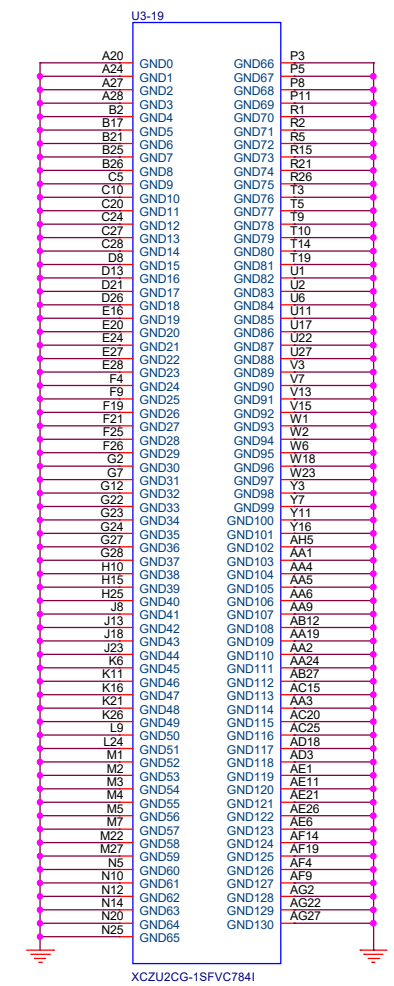
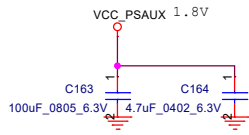
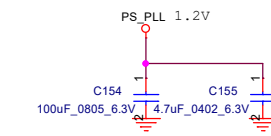
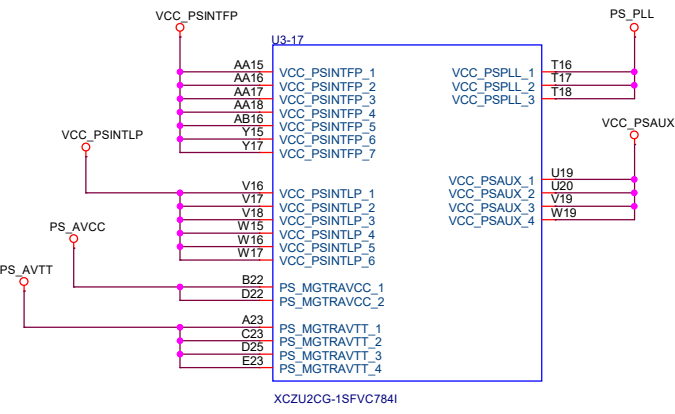
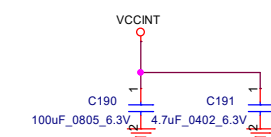
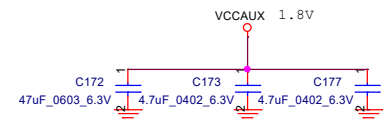
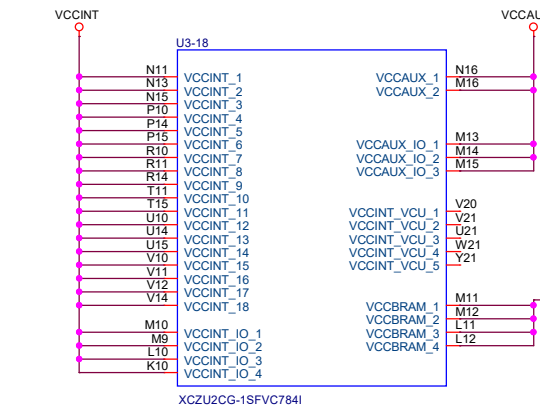
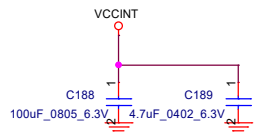
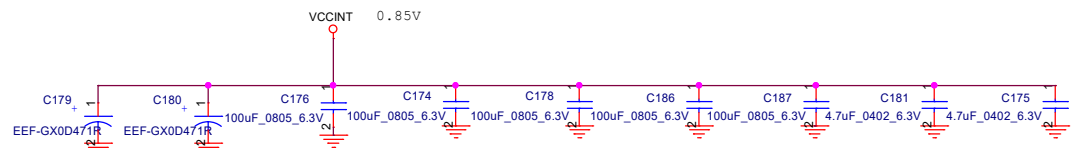
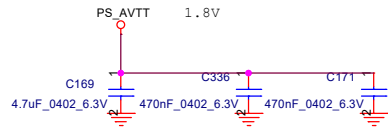
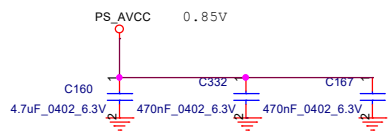
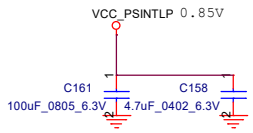
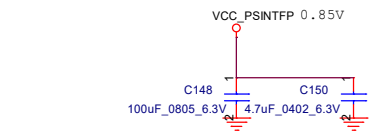


XCZU2CG-1SFVC7841



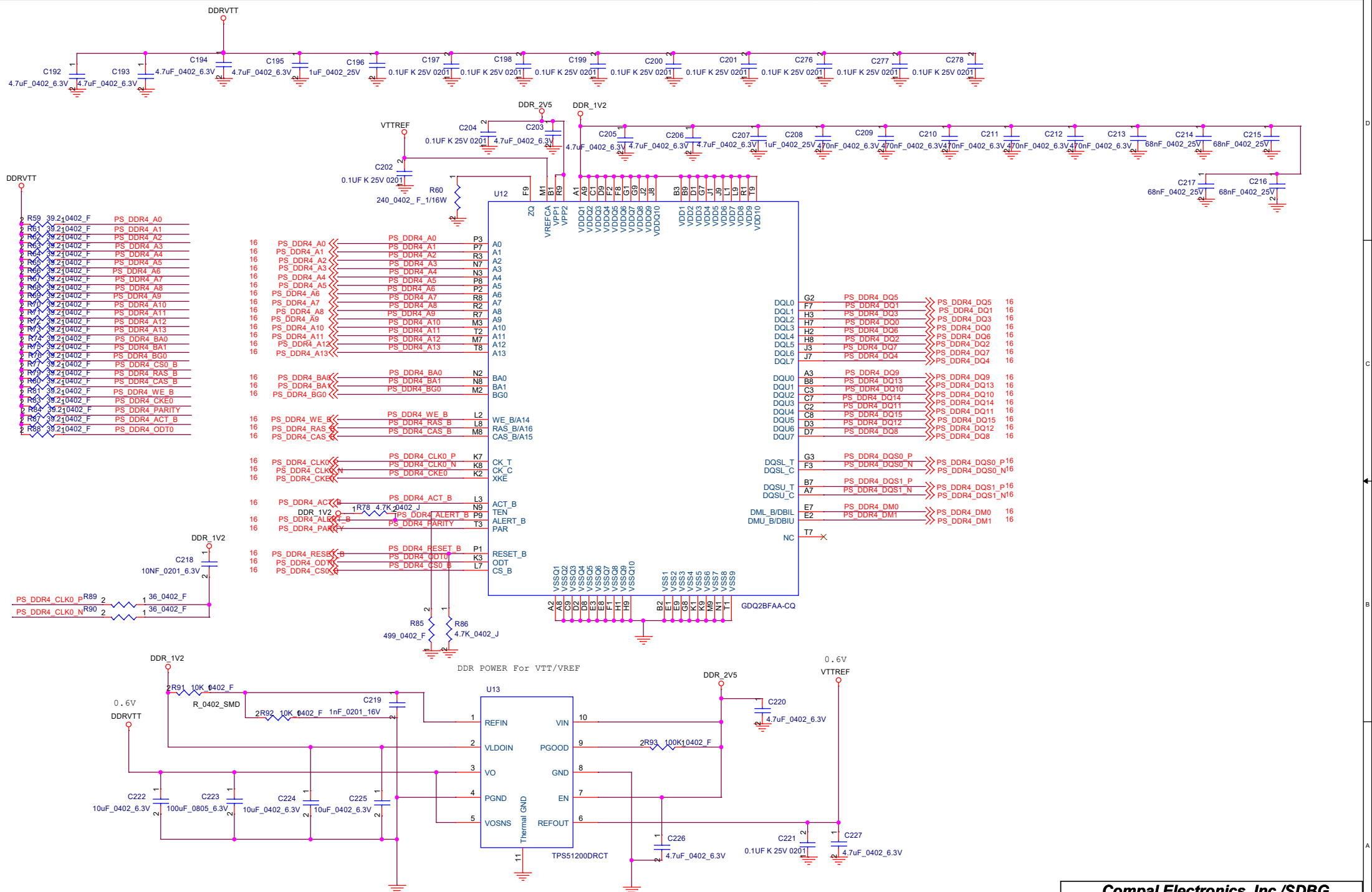
XCZU2CG-1SFVC7841





THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>			
SCHEMATIC, M/B GA-641 (BT/WIFI)			
Size	Document Number	Rev	BI
A3	601K39		
Date:	Monday, March 04, 2024	Sheet	13 of 17



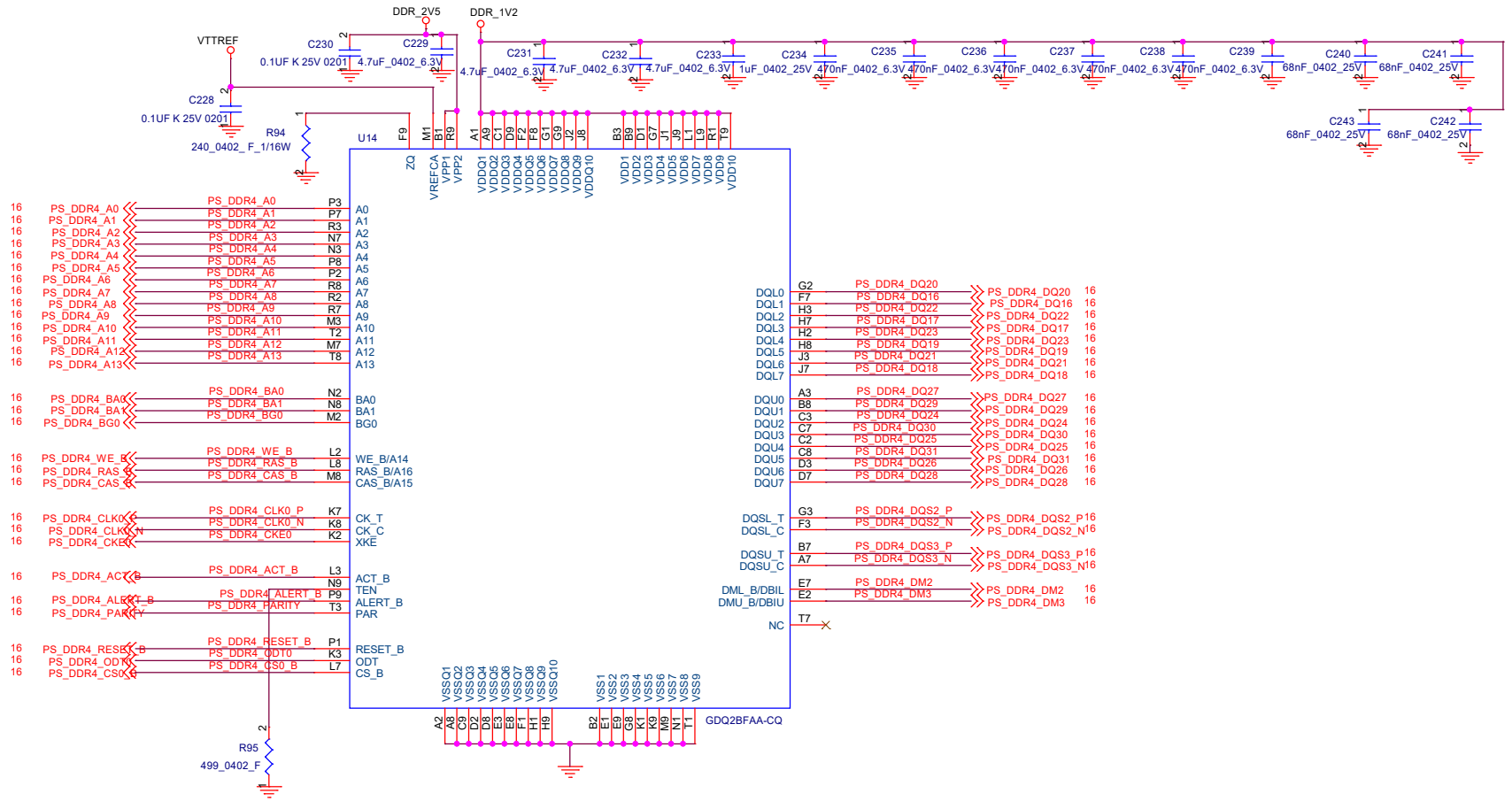
R59	39.2k_0402_F	PS_DDR4_A0
R60	39.2k_0402_F	PS_DDR4_A1
R61	39.2k_0402_F	PS_DDR4_A2
R62	39.2k_0402_F	PS_DDR4_A3
R63	39.2k_0402_F	PS_DDR4_A4
R64	39.2k_0402_F	PS_DDR4_A5
R65	39.2k_0402_F	PS_DDR4_A6
R66	39.2k_0402_F	PS_DDR4_A7
R67	39.2k_0402_F	PS_DDR4_A8
R68	39.2k_0402_F	PS_DDR4_A9
R69	39.2k_0402_F	PS_DDR4_A10
R70	39.2k_0402_F	PS_DDR4_A11
R71	39.2k_0402_F	PS_DDR4_A12
R72	39.2k_0402_F	PS_DDR4_A13
R73	39.2k_0402_F	PS_DDR4_BA0
R74	39.2k_0402_F	PS_DDR4_BA1
R75	39.2k_0402_F	PS_DDR4_BA2
R76	39.2k_0402_F	PS_DDR4_BA3
R77	39.2k_0402_F	PS_DDR4_BA4
R78	39.2k_0402_F	PS_DDR4_BA5
R79	39.2k_0402_F	PS_DDR4_BA6
R80	39.2k_0402_F	PS_DDR4_BA7
R81	39.2k_0402_F	PS_DDR4_BA8
R82	39.2k_0402_F	PS_DDR4_BA9
R83	39.2k_0402_F	PS_DDR4_BA10
R84	39.2k_0402_F	PS_DDR4_BA11
R85	39.2k_0402_F	PS_DDR4_BA12
R86	39.2k_0402_F	PS_DDR4_BA13
R87	39.2k_0402_F	PS_DDR4_CS0_B
R88	39.2k_0402_F	PS_DDR4_RAS_B
R89	39.2k_0402_F	PS_DDR4_CAS_B
R90	39.2k_0402_F	PS_DDR4_WE_B
R91	39.2k_0402_F	PS_DDR4_CKE0
R92	39.2k_0402_F	PS_DDR4_CKE1
R93	39.2k_0402_F	PS_DDR4_CKE2
R94	39.2k_0402_F	PS_DDR4_CKE3
R95	39.2k_0402_F	PS_DDR4_CKE4
R96	39.2k_0402_F	PS_DDR4_CKE5
R97	39.2k_0402_F	PS_DDR4_CKE6
R98	39.2k_0402_F	PS_DDR4_CKE7
R99	39.2k_0402_F	PS_DDR4_CKE8
R100	39.2k_0402_F	PS_DDR4_CKE9

16	PS_DDR4_A0	PS_DDR4_A0	P3	A0
16	PS_DDR4_A1	PS_DDR4_A1	P7	A1
16	PS_DDR4_A2	PS_DDR4_A2	R3	A2
16	PS_DDR4_A3	PS_DDR4_A3	N7	A3
16	PS_DDR4_A4	PS_DDR4_A4	R3	A4
16	PS_DDR4_A5	PS_DDR4_A5	P8	A5
16	PS_DDR4_A6	PS_DDR4_A6	R2	A6
16	PS_DDR4_A7	PS_DDR4_A7	R8	A7
16	PS_DDR4_A8	PS_DDR4_A8	R2	A8
16	PS_DDR4_A9	PS_DDR4_A9	R7	A9
16	PS_DDR4_A10	PS_DDR4_A10	M3	A10
16	PS_DDR4_A11	PS_DDR4_A11	T2	A11
16	PS_DDR4_A12	PS_DDR4_A12	M7	A12
16	PS_DDR4_A13	PS_DDR4_A13	T8	A13
16	PS_DDR4_BA0	PS_DDR4_BA0	N2	BA0
16	PS_DDR4_BA1	PS_DDR4_BA1	N8	BA1
16	PS_DDR4_BA2	PS_DDR4_BA2	M2	BA2
16	PS_DDR4_BA3	PS_DDR4_BA3	M2	BA3
16	PS_DDR4_BA4	PS_DDR4_BA4	M2	BA4
16	PS_DDR4_BA5	PS_DDR4_BA5	M2	BA5
16	PS_DDR4_BA6	PS_DDR4_BA6	M2	BA6
16	PS_DDR4_BA7	PS_DDR4_BA7	M2	BA7
16	PS_DDR4_BA8	PS_DDR4_BA8	M2	BA8
16	PS_DDR4_BA9	PS_DDR4_BA9	M2	BA9
16	PS_DDR4_BA10	PS_DDR4_BA10	M2	BA10
16	PS_DDR4_BA11	PS_DDR4_BA11	M2	BA11
16	PS_DDR4_BA12	PS_DDR4_BA12	M2	BA12
16	PS_DDR4_BA13	PS_DDR4_BA13	M2	BA13
16	PS_DDR4_WE_B	PS_DDR4_WE_B	L2	WE_B/A14
16	PS_DDR4_RAS_B	PS_DDR4_RAS_B	L8	RAS_B/A15
16	PS_DDR4_CAS_B	PS_DDR4_CAS_B	M8	CAS_B/A15
16	PS_DDR4_CLK0_P	PS_DDR4_CLK0_P	K7	CK_T
16	PS_DDR4_CLK0_N	PS_DDR4_CLK0_N	K8	CK_C
16	PS_DDR4_CKE0	PS_DDR4_CKE0	K2	XKE
16	PS_DDR4_ACT_B	PS_DDR4_ACT_B	L3	ACT_B
16	PS_DDR4_ALERT_B	PS_DDR4_ALERT_B	N9	TEN
16	PS_DDR4_PARITY	PS_DDR4_PARITY	P9	ALERT_B
16	PS_DDR4_RESET_B	PS_DDR4_RESET_B	P1	RESET_B
16	PS_DDR4_ODT0	PS_DDR4_ODT0	K3	ODT
16	PS_DDR4_CS0_B	PS_DDR4_CS0_B	L7	CS_B

G2	PS_DDR4_DQ5	PS_DDR4_DQ5	16
F7	PS_DDR4_DQ1	PS_DDR4_DQ1	16
H3	PS_DDR4_DQ3	PS_DDR4_DQ3	16
H7	PS_DDR4_DQ0	PS_DDR4_DQ0	16
H2	PS_DDR4_DQ6	PS_DDR4_DQ6	16
H8	PS_DDR4_DQ2	PS_DDR4_DQ2	16
J3	PS_DDR4_DQ7	PS_DDR4_DQ7	16
J7	PS_DDR4_DQ4	PS_DDR4_DQ4	16
A3	PS_DDR4_DQ9	PS_DDR4_DQ9	16
B8	PS_DDR4_DQ13	PS_DDR4_DQ13	16
C3	PS_DDR4_DQ10	PS_DDR4_DQ10	16
C7	PS_DDR4_DQ14	PS_DDR4_DQ14	16
C2	PS_DDR4_DQ11	PS_DDR4_DQ11	16
C8	PS_DDR4_DQ15	PS_DDR4_DQ15	16
D3	PS_DDR4_DQ12	PS_DDR4_DQ12	16
D7	PS_DDR4_DQ8	PS_DDR4_DQ8	16
G3	PS_DDR4_DQS0_P	PS_DDR4_DQS0_P	16
F3	PS_DDR4_DQS0_N	PS_DDR4_DQS0_N	16
B7	PS_DDR4_DQS1_P	PS_DDR4_DQS1_P	16
A7	PS_DDR4_DQS1_N	PS_DDR4_DQS1_N	16
E7	PS_DDR4_DM0	PS_DDR4_DM0	16
E2	PS_DDR4_DM1	PS_DDR4_DM1	16
T7	NC	NC	16

<b>Compal Electronics, Inc./SDBG</b>			
Title: SCHEMATIC, M/B GA-641 (MFI)			
Size: A3	Document Number: 601K39	Rev: B1	
Date: Monday, March 04, 2024	Sheet: 14	of 17	

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

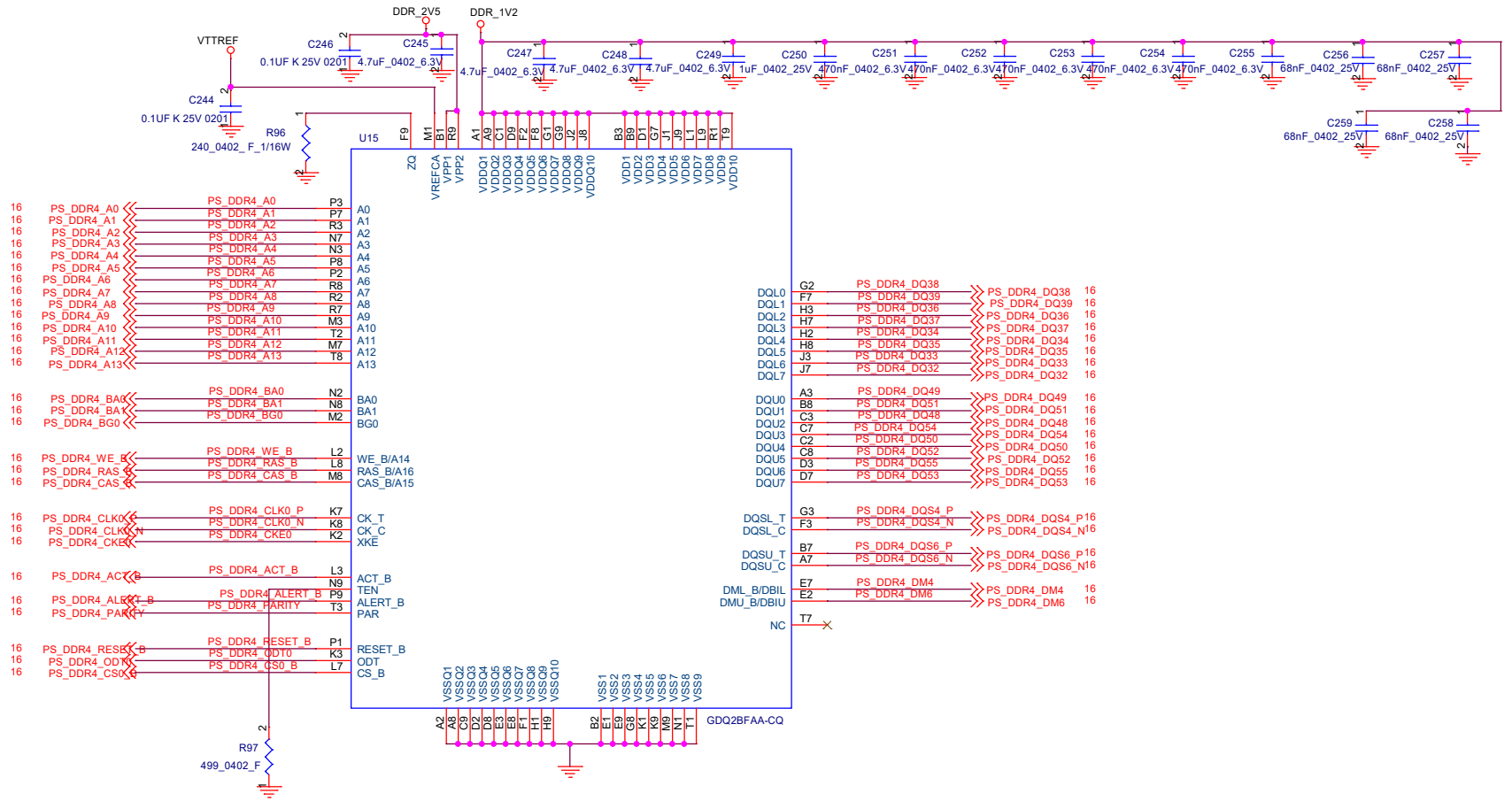


- 16 PS\_DDR4\_A0 <<> PS\_DDR4\_A0 P3 A0
- 16 PS\_DDR4\_A1 <<> PS\_DDR4\_A1 P7 A1
- 16 PS\_DDR4\_A2 <<> PS\_DDR4\_A2 R3 A2
- 16 PS\_DDR4\_A3 <<> PS\_DDR4\_A3 N7 A3
- 16 PS\_DDR4\_A4 <<> PS\_DDR4\_A4 N3 A4
- 16 PS\_DDR4\_A5 <<> PS\_DDR4\_A5 P8 A5
- 16 PS\_DDR4\_A6 <<> PS\_DDR4\_A6 P2 A6
- 16 PS\_DDR4\_A7 <<> PS\_DDR4\_A7 R8 A6
- 16 PS\_DDR4\_A7 <<> PS\_DDR4\_A8 R2 A7
- 16 PS\_DDR4\_A8 <<> PS\_DDR4\_A9 R7 A9
- 16 PS\_DDR4\_A9 <<> PS\_DDR4\_A10 M3 A10
- 16 PS\_DDR4\_A10 <<> PS\_DDR4\_A11 Y2 A11
- 16 PS\_DDR4\_A11 <<> PS\_DDR4\_A12 M7 A12
- 16 PS\_DDR4\_A12 <<> PS\_DDR4\_A13 T8 A13
- 16 PS\_DDR4\_A13 <<> PS\_DDR4\_A13 T8 A13
  
- 16 PS\_DDR4\_BA0 <<> PS\_DDR4\_BA0 N2 BA0
- 16 PS\_DDR4\_BA1 <<> PS\_DDR4\_BA1 N8 BA1
- 16 PS\_DDR4\_BG0 <<> PS\_DDR4\_BG0 M2 BG0
  
- 16 PS\_DDR4\_WE <<> PS\_DDR4\_WE\_B L2 WE\_B/A14
- 16 PS\_DDR4\_RAS <<> PS\_DDR4\_RAS\_B L8 RAS\_B/A16
- 16 PS\_DDR4\_CAS <<> PS\_DDR4\_CAS\_B M8 CAS\_B/A15
  
- 16 PS\_DDR4\_CLK0 <<> PS\_DDR4\_CLK0\_P K7 CK\_T
- 16 PS\_DDR4\_CLK0 <<> PS\_DDR4\_CLK0\_N K8 CK\_C
- 16 PS\_DDR4\_CKE <<> PS\_DDR4\_CKE0 K2 CKE
  
- 16 PS\_DDR4\_ACT <<> PS\_DDR4\_ACT\_B L3 ACT\_B
- 16 PS\_DDR4\_ALERT <<> PS\_DDR4\_ALERT\_B P9 TEN
- 16 PS\_DDR4\_PAR <<> PS\_DDR4\_PARITY T3 ALERT\_B
  
- 16 PS\_DDR4\_RESET <<> PS\_DDR4\_RESET\_B P1 RESET\_B
- 16 PS\_DDR4\_ODT <<> PS\_DDR4\_ODT0 K3 ODT
- 16 PS\_DDR4\_CS <<> PS\_DDR4\_CS0\_B L7 CS\_B

- DQ00 G2 PS\_DDR4\_DQ00 <>> PS\_DDR4\_DQ00 16
- DQ01 F7 PS\_DDR4\_DQ01 <>> PS\_DDR4\_DQ01 16
- DQ02 H3 PS\_DDR4\_DQ02 <>> PS\_DDR4\_DQ02 16
- DQ03 H7 PS\_DDR4\_DQ03 <>> PS\_DDR4\_DQ03 16
- DQ04 H2 PS\_DDR4\_DQ04 <>> PS\_DDR4\_DQ04 16
- DQ05 H8 PS\_DDR4\_DQ05 <>> PS\_DDR4\_DQ05 16
- DQ06 J3 PS\_DDR4\_DQ06 <>> PS\_DDR4\_DQ06 16
- DQ07 J7 PS\_DDR4\_DQ07 <>> PS\_DDR4\_DQ07 16
- DQ08 A3 PS\_DDR4\_DQ08 <>> PS\_DDR4\_DQ08 16
- DQ09 B8 PS\_DDR4\_DQ09 <>> PS\_DDR4\_DQ09 16
- DQ10 C3 PS\_DDR4\_DQ10 <>> PS\_DDR4\_DQ10 16
- DQ11 C7 PS\_DDR4\_DQ11 <>> PS\_DDR4\_DQ11 16
- DQ12 C2 PS\_DDR4\_DQ12 <>> PS\_DDR4\_DQ12 16
- DQ13 C8 PS\_DDR4\_DQ13 <>> PS\_DDR4\_DQ13 16
- DQ14 D3 PS\_DDR4\_DQ14 <>> PS\_DDR4\_DQ14 16
- DQ15 D7 PS\_DDR4\_DQ15 <>> PS\_DDR4\_DQ15 16
- DQ16 G3 PS\_DDR4\_DQ16 <>> PS\_DDR4\_DQ16 16
- DQ17 F3 PS\_DDR4\_DQ17 <>> PS\_DDR4\_DQ17 16
- DQ18 B7 PS\_DDR4\_DQ18 <>> PS\_DDR4\_DQ18 16
- DQ19 A7 PS\_DDR4\_DQ19 <>> PS\_DDR4\_DQ19 16
- DQ20 E7 PS\_DDR4\_DQ20 <>> PS\_DDR4\_DQ20 16
- DQ21 E2 PS\_DDR4\_DQ21 <>> PS\_DDR4\_DQ21 16
- DQ22 T7 X

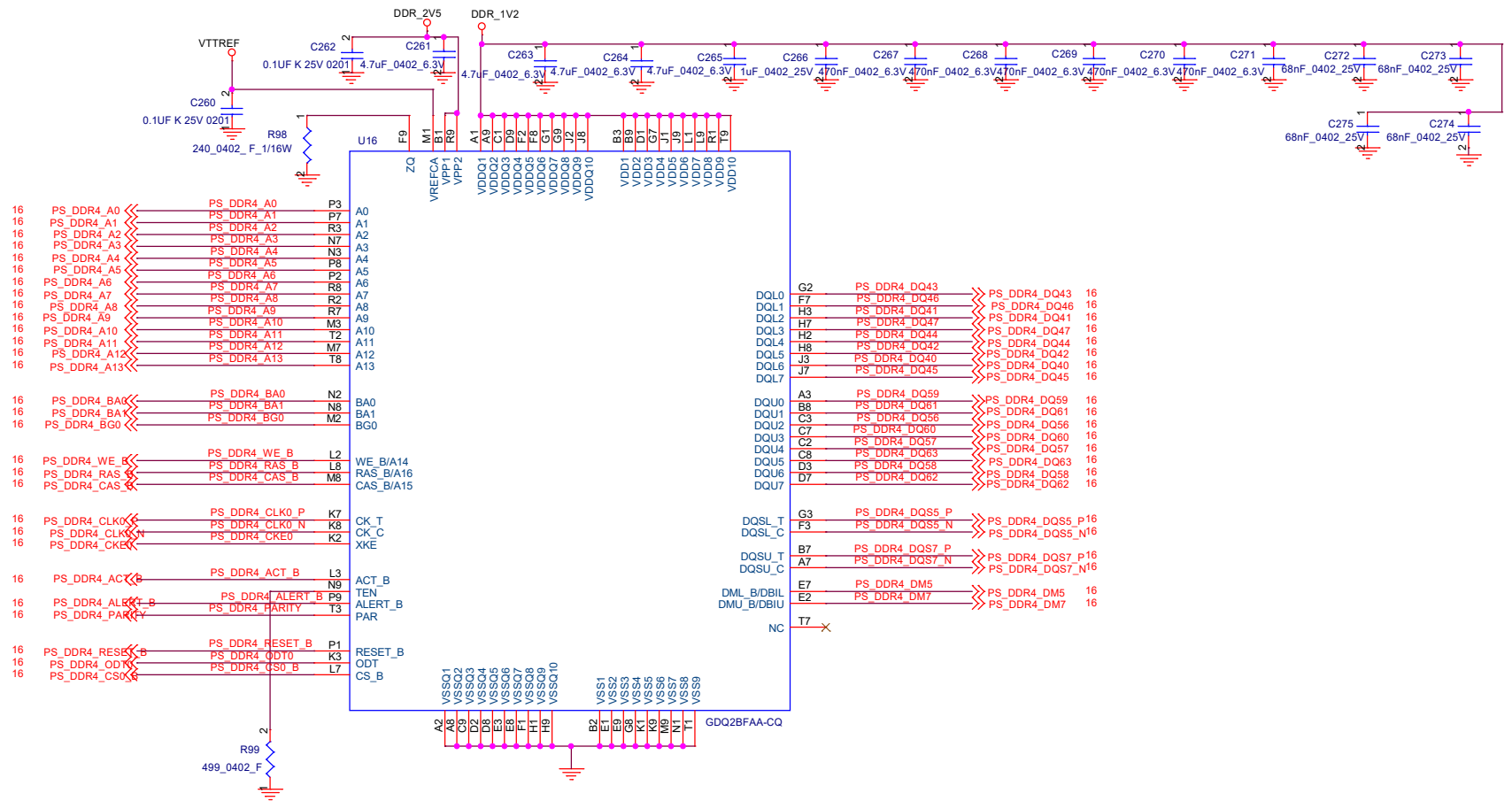
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>			
Title <b>SCHEMATIC, M/B GA-641 (MFI)</b>			
Size <b>A3</b>	Document Number <b>601K39</b>	Rev <b>B1</b>	
Date: <b>Monday, March 04, 2024</b>	Sheet <b>14</b>	of <b>17</b>	



<b>Compal Electronics, Inc./SDBG</b>		
Title SCHEMATIC, M/B GA-641 (MFI)		
Size A3	Document Number 601K39	Rev B1
Date: Monday, March 04, 2024	Sheet 14	of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



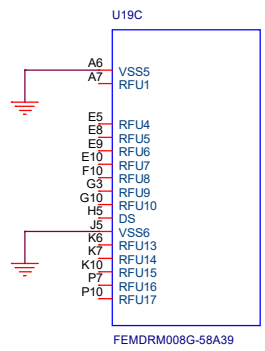
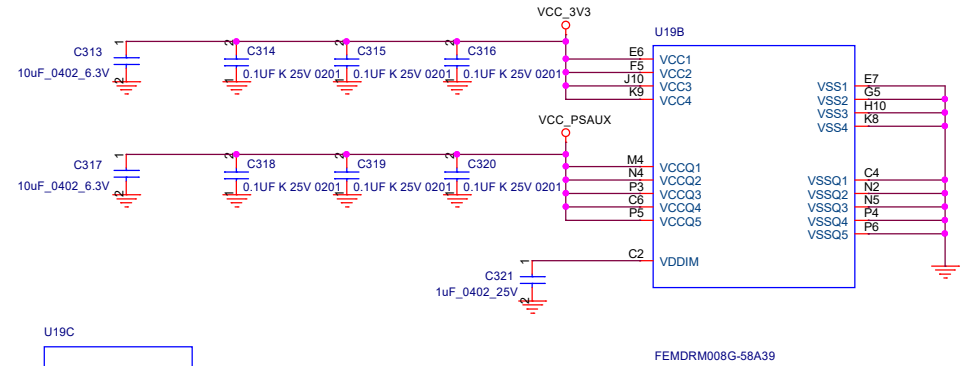
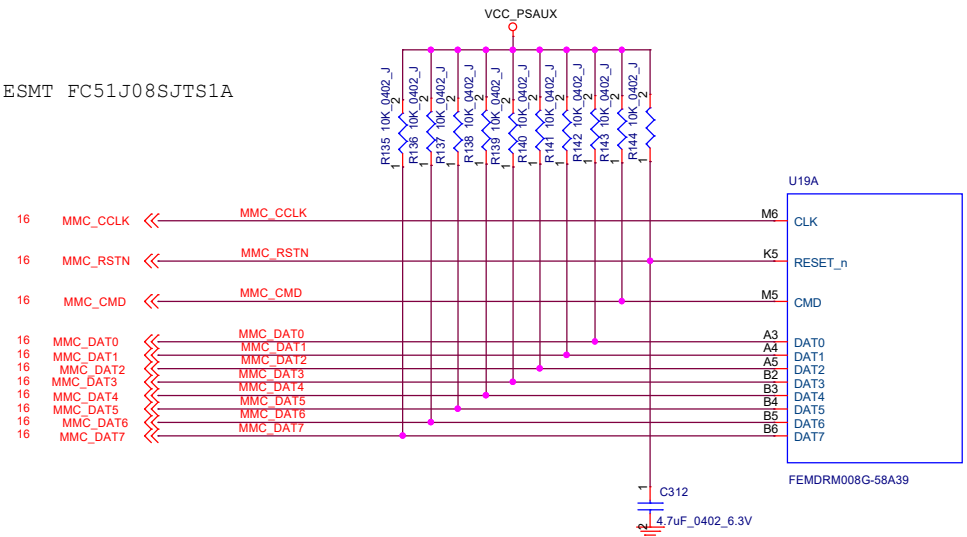
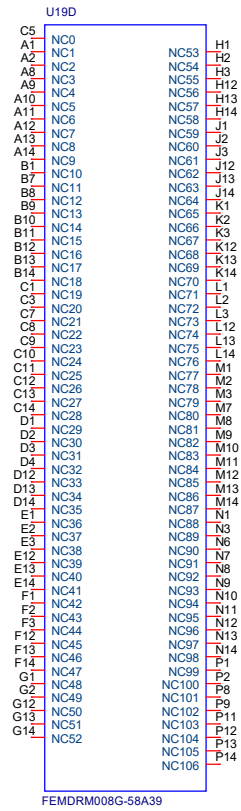
- 16 PS\_DDR4\_A0 <-> PS\_DDR4\_A0 P3 A0
- 16 PS\_DDR4\_A1 <-> PS\_DDR4\_A1 P7 A1
- 16 PS\_DDR4\_A2 <-> PS\_DDR4\_A2 R3 A2
- 16 PS\_DDR4\_A3 <-> PS\_DDR4\_A3 N7 A3
- 16 PS\_DDR4\_A4 <-> PS\_DDR4\_A4 N3 A4
- 16 PS\_DDR4\_A5 <-> PS\_DDR4\_A5 P8 A5
- 16 PS\_DDR4\_A6 <-> PS\_DDR4\_A6 P2 A6
- 16 PS\_DDR4\_A7 <-> PS\_DDR4\_A7 R8 A7
- 16 PS\_DDR4\_A8 <-> PS\_DDR4\_A8 R2 A8
- 16 PS\_DDR4\_A9 <-> PS\_DDR4\_A9 R7 A9
- 16 PS\_DDR4\_A10 <-> PS\_DDR4\_A10 M3 A10
- 16 PS\_DDR4\_A11 <-> PS\_DDR4\_A11 T2 A11
- 16 PS\_DDR4\_A12 <-> PS\_DDR4\_A12 M7 A12
- 16 PS\_DDR4\_A13 <-> PS\_DDR4\_A13 T8 A13
  
- 16 PS\_DDR4\_BA0 <-> PS\_DDR4\_BA0 N2 BA0
- 16 PS\_DDR4\_BA1 <-> PS\_DDR4\_BA1 N8 BA1
- 16 PS\_DDR4\_BG0 <-> PS\_DDR4\_BG0 M2 BA0
  
- 16 PS\_DDR4\_WE <-> PS\_DDR4\_WE\_B L2 WE\_B/A14
- 16 PS\_DDR4\_RAS <-> PS\_DDR4\_RAS\_B L8 RAS\_B/A16
- 16 PS\_DDR4\_CAS <-> PS\_DDR4\_CAS\_B M8 CAS\_B/A15
  
- 16 PS\_DDR4\_CLK0 <-> PS\_DDR4\_CLK0\_P K7 CK\_T
- 16 PS\_DDR4\_CLK0 <-> PS\_DDR4\_CLK0\_N K8 CK\_C
- 16 PS\_DDR4\_CKE <-> PS\_DDR4\_CKE0 K2 XKE
  
- 16 PS\_DDR4\_ACT <-> PS\_DDR4\_ACT\_B L3 ACT\_B
- 16 PS\_DDR4\_ALERT <-> PS\_DDR4\_ALERT\_B P9 TEN
- 16 PS\_DDR4\_PARK <-> PS\_DDR4\_PARK\_T3 PAR
  
- 16 PS\_DDR4\_RESET <-> PS\_DDR4\_RESET\_B P1 RESET\_B
- 16 PS\_DDR4\_ODT <-> PS\_DDR4\_ODT0 K3 ODT
- 16 PS\_DDR4\_CS0 <-> PS\_DDR4\_CS0\_B L7 CS\_B

- G2 PS\_DDR4\_DQ43 <-> PS\_DDR4\_DQ43 16
- F7 PS\_DDR4\_DQ46 <-> PS\_DDR4\_DQ46 16
- H3 PS\_DDR4\_DQ41 <-> PS\_DDR4\_DQ41 16
- H7 PS\_DDR4\_DQ47 <-> PS\_DDR4\_DQ47 16
- H2 PS\_DDR4\_DQ44 <-> PS\_DDR4\_DQ44 16
- H8 PS\_DDR4\_DQ42 <-> PS\_DDR4\_DQ42 16
- J3 PS\_DDR4\_DQ30 <-> PS\_DDR4\_DQ30 16
- J7 PS\_DDR4\_DQ45 <-> PS\_DDR4\_DQ45 16
  
- A3 PS\_DDR4\_DQ59 <-> PS\_DDR4\_DQ59 16
- B8 PS\_DDR4\_DQ61 <-> PS\_DDR4\_DQ61 16
- C3 PS\_DDR4\_DQ56 <-> PS\_DDR4\_DQ56 16
- C7 PS\_DDR4\_DQ60 <-> PS\_DDR4\_DQ60 16
- C2 PS\_DDR4\_DQ57 <-> PS\_DDR4\_DQ57 16
- C8 PS\_DDR4\_DQ63 <-> PS\_DDR4\_DQ63 16
- D3 PS\_DDR4\_DQ58 <-> PS\_DDR4\_DQ58 16
- D7 PS\_DDR4\_DQ62 <-> PS\_DDR4\_DQ62 16
  
- G3 PS\_DDR4\_DQS5\_P <-> PS\_DDR4\_DQS5\_P16
- F3 PS\_DDR4\_DQS5\_N <-> PS\_DDR4\_DQS5\_N16
  
- B7 PS\_DDR4\_DQS7\_P <-> PS\_DDR4\_DQS7\_P16
- A7 PS\_DDR4\_DQS7\_N <-> PS\_DDR4\_DQS7\_N16
  
- E7 PS\_DDR4\_DM5 <-> PS\_DDR4\_DM5 16
- E2 PS\_DDR4\_DM7 <-> PS\_DDR4\_DM7 16

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

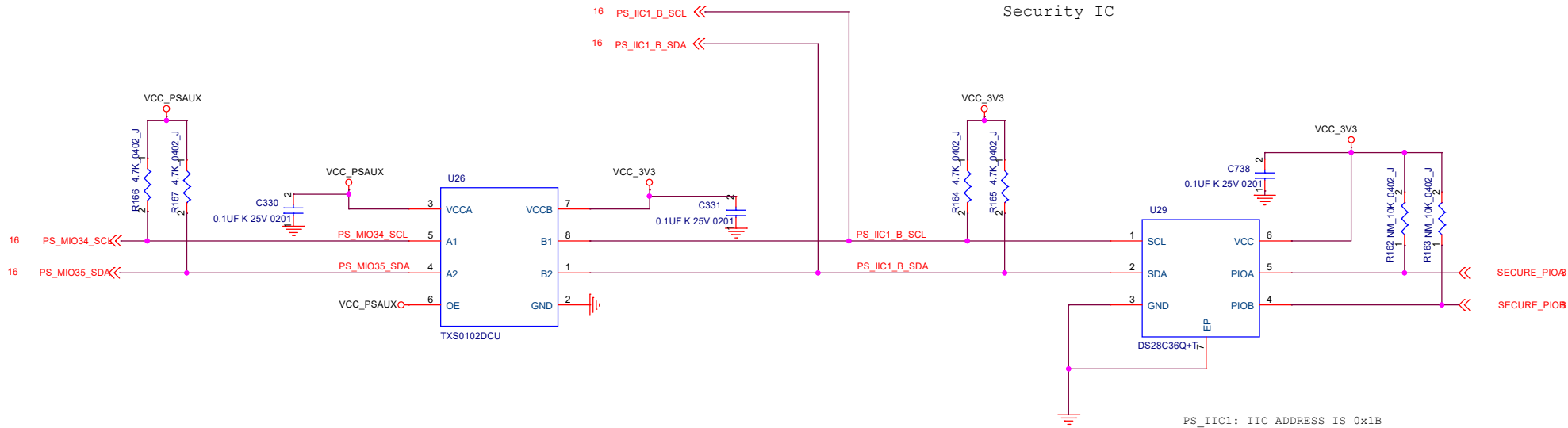
<b>Compal Electronics, Inc./SDBG</b>			
Title <b>SCHEMATIC, M/B GA-641 (MFI)</b>			
Size <b>A3</b>	Document Number <b>601K39</b>	Rev <b>B1</b>	
Date: <b>Monday, March 04, 2024</b>	Sheet <b>14</b>	of <b>17</b>	

11/16 reference use FORESEE FEMDRM008G, it's not AVL, PUR syggest ESMT FC51J08SJS1a



Compal Electronics, Inc./SDBG			
Title			
SCHEMATIC, M/B GA-641 (MFI)			
Size	Document Number	Rev	
A3	601K39	B1	
Date:	Monday, March 04, 2024	Sheet	14 of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



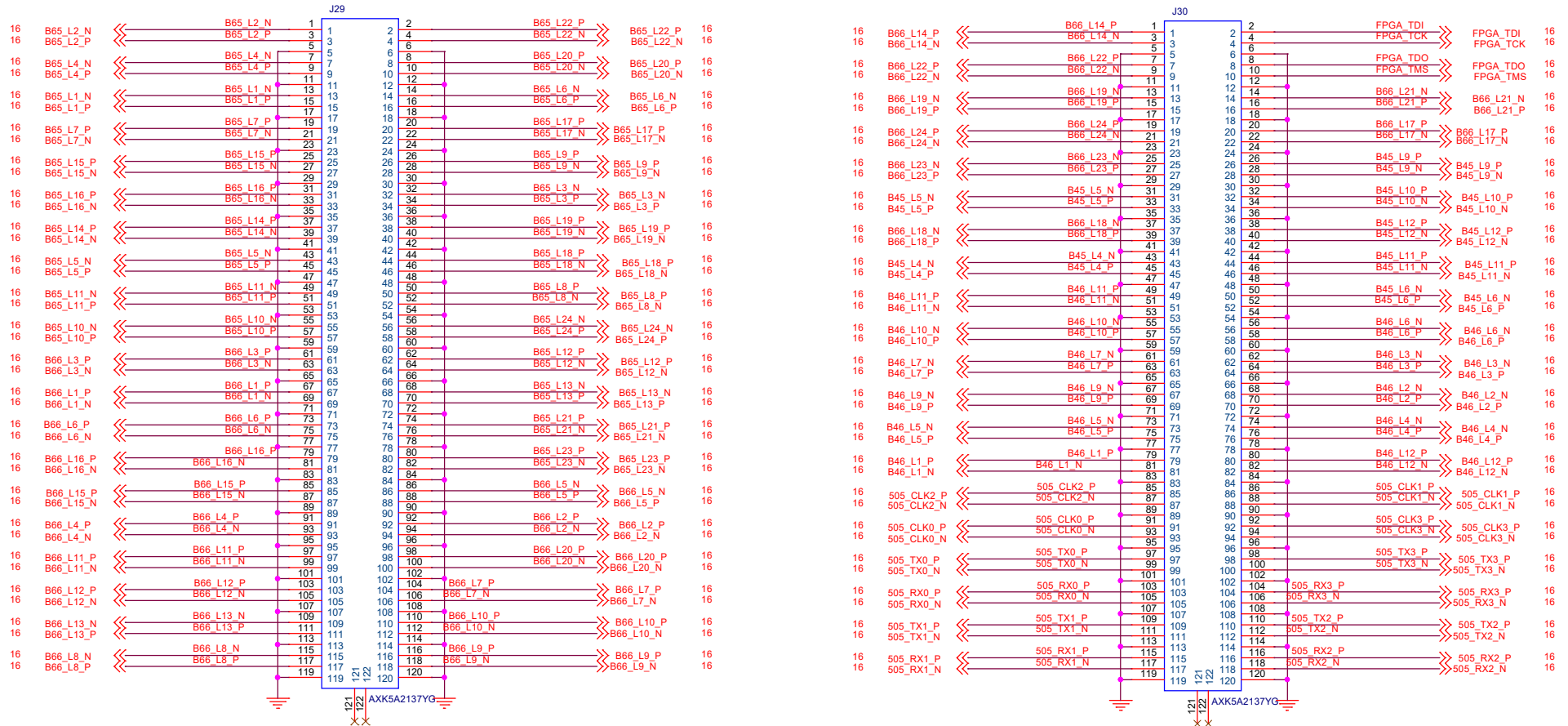
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>			
Title <b>SCHEMATIC, M/B GA-641 (MFI)</b>			
Size <b>A3</b>	Document Number <b>601K39</b>	Rev <b>B1</b>	
Date: <b>Monday, March 04, 2024</b>	Sheet <b>14</b> of <b>17</b>		



BANK65, BANK66 IO Voltage can not exceed +1.8V

BANK45, BANK46 IO Voltage is +3.3V Standard

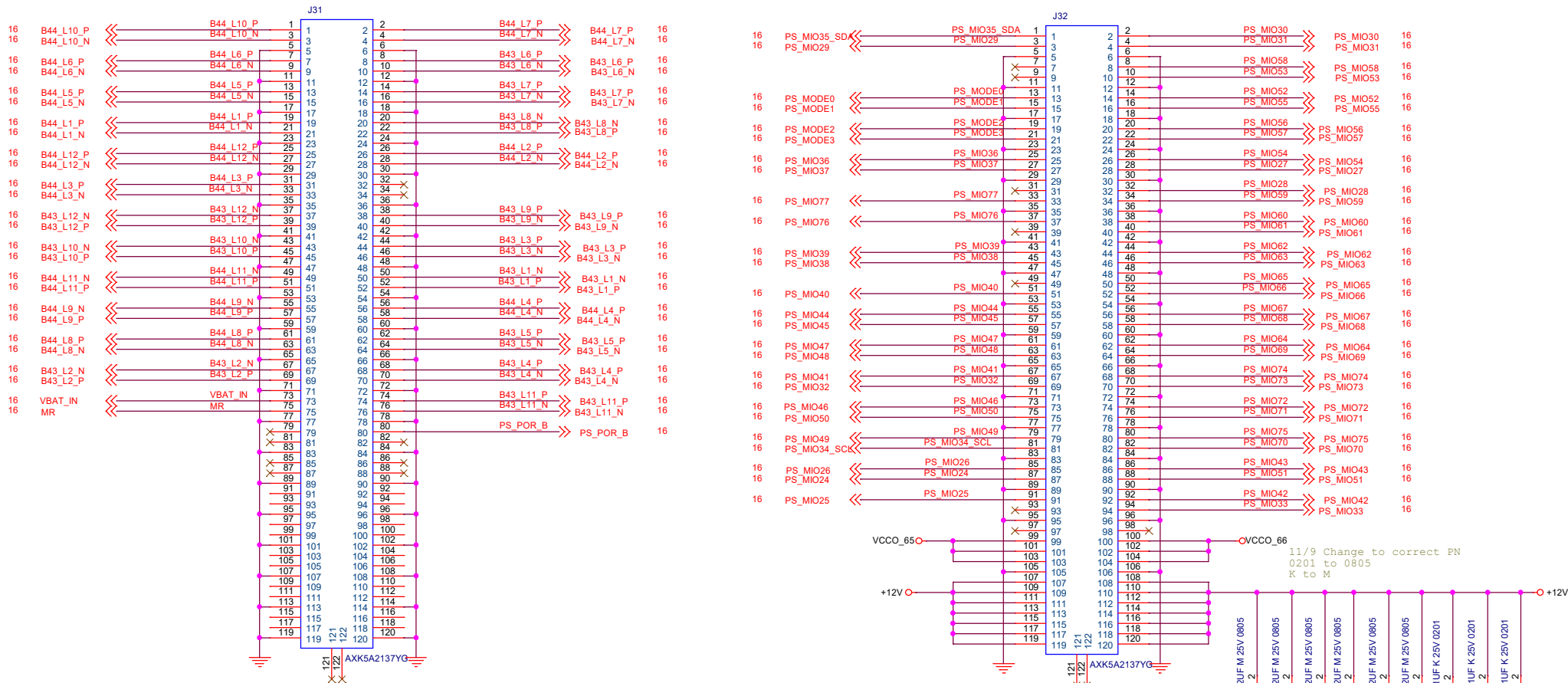


<b>Compal Electronics, Inc./SDBG</b>			
SCHEMATIC, M/B GA-641 (MFI)			
Size	Document Number	Rev	
A3	601K39	BI	
Date:	Monday, March 04, 2024	Sheet	14 of 17

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

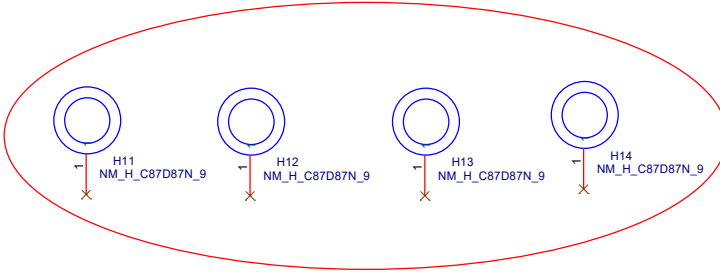
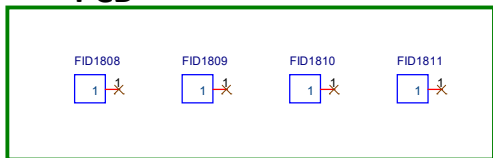
BANK43, BANK44 IO Voltage is +3.3V Standard

The MIO Voltage is +1.8V Standard



**ORIENTATION HOLE**

**PCB**



VCCO\_65 VCCO\_66 Power supply can not exceed 1.8V

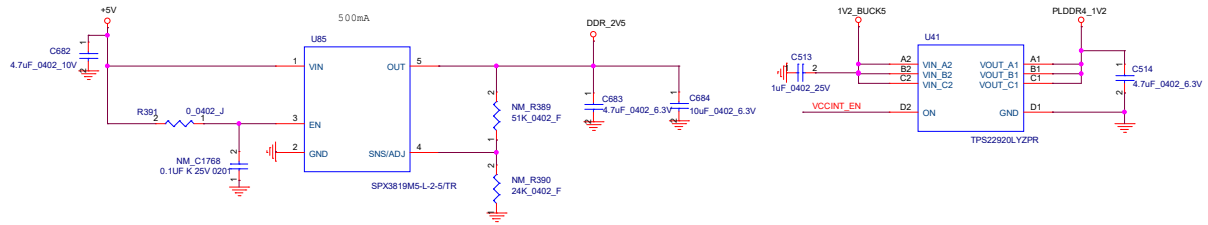
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

<b>Compal Electronics, Inc./SDBG</b>			
Title SCHEMATIC, M/B GA-641 (MFI)			
Size A3	Document Number 601K39	Rev B1	
Date Monday, March 04, 2024	Sheet 14	of 17	

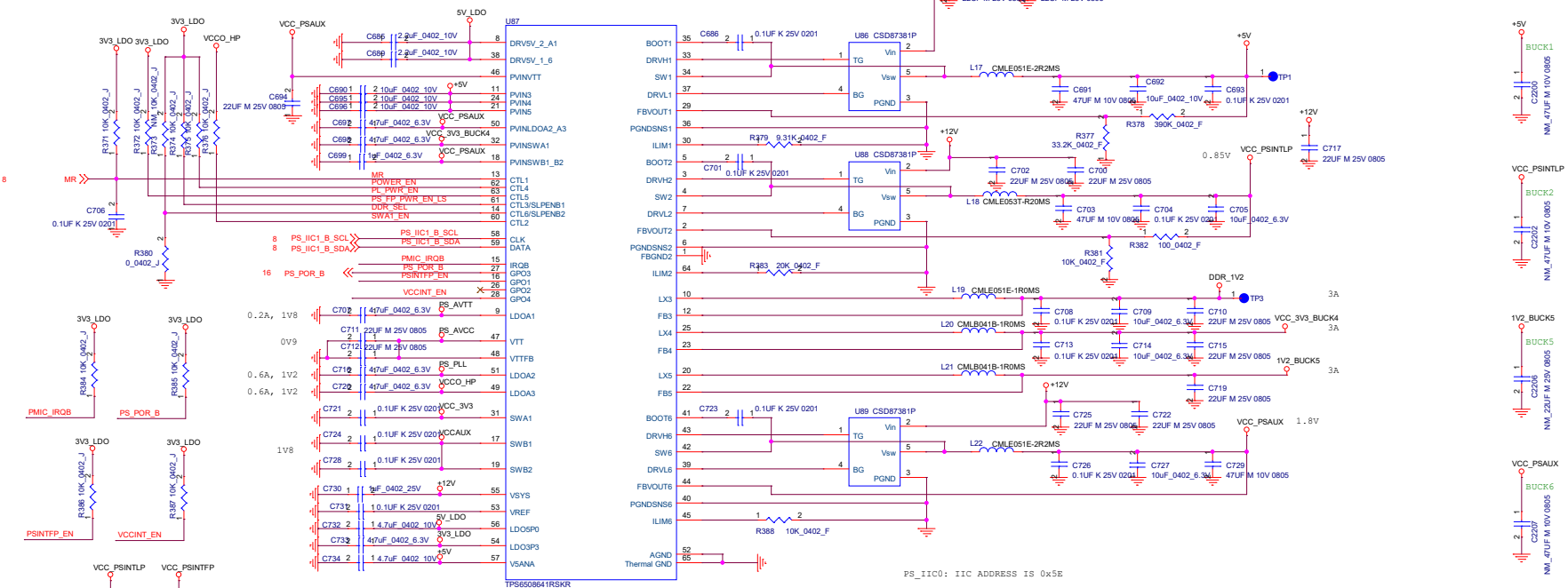
UBS select

	R389	R390	R391	C1768
RT9080N-08GJ5	51K	24K	10K	0.1uF
SPX3819M5-L-2-5	NM	NM	0	NM

11/24 原本是SPX3819M5-L-2-5不是我們AVL, PUR建議用RT9080N-08GJ5 performance差不多且pin to pin



GP01-----BUCK1\_L\_PG  
 GP04-----BUCK4\_PG  
 CTL2-----enable and disable SWA1  
 CTL14-----enable BUCK1  
 CTL13-----PS\_PP\_PWR\_EN\_LS  
 CTL15-----PL\_PWR\_B



- PS\_AVTT 1 TP5
- VCC\_3V3 1 TP6
- PS\_AVCC 1 TP10
- DDR\_2V5 1 TP11

PS\_IIC0: IIC ADDRESS IS 0x5E

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL COMMUNICATIONS, INC. NEITHER THIS SHEET NOR THE INFORMATION CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.