Active Clamp Flyback Using GaN Power IC for Power Adapter Applications

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Abstract— **Both high switching frequency and high efficiency are critical in reducing power adapter size. The active clamp flyback (ACF) topology allows zero voltage soft switching under all line and load conditions, eliminating all leakage inductance and snubber losses. Using enhanced mode GaN switches, an optimized active clamp flyback can enable 5-10x higher switching frequency, while improving efficiency. This paper analyzes a high frequency ACF operating in critical conduction mode. Detailed equivalent circuits and analytical models are provided to explain operation principles and current waveforms. A novel secondary side resonant concept is presented to shape the clamp current waveform in a way that significantly reduces rms current and improves synchronous rectifier operation. Using monolithic GaN power ICs, a high density 45W adapter prototype is demonstrated with excellent efficiency and EMI performance.**

Keywords— Gallium Nitride; GaN; Active Clamp Flyback; ACF; Power Adapter; Soft Switching; High Frequency; Critical Conduction Mode; Zero Current Switching; Synchronous Rectifier

I. INTRODUCTION

With the rapid market adoption of fast charging and USB-PD standards, there is a growing need for significant power density improvement for travel adapters. In a fully-enclosed adapter, any size reduction through package innovation or high frequency switching must be accompanied by efficiency improvement to maintain low component and adapter case temperatures. The single-switch quasi-resonant (QR) flyback [1][2] has been popular in power adapter applications. It operates in discontinuous current conduction mode, achieving zero voltage soft switching (ZVS) at low line and partial hard switching at high line. However, as transformer leakage energy is not recovered, snubbers or clamps are needed to protect primary and secondary switches, and reduce voltage ringing to contain EMI. As snubber loss is proportional to switching frequency, QR flyback typically operates below 150 kHz, which sets a hard ceiling to power density and adapter size.

Active clamp flyback (ACF) is a two-switch topology that achieves soft switching and recovers leakage inductance energy. Traditional ACF operates in continuous conduction mode (CCM) [3], which maintains positive magnetizing current. As leakage inductance alone doesn't store enough energy to achieve full ZVS, QR usually requires an additional, external inductor. Output rectifier diode or synchronous rectifier (SR) turn-off is hard switched, which generates voltage ringing across the rectifier and requires a snubber to contain noise or voltage overshoot. Another issue with CCM is that ZVS energy stored in resonant inductor reduces with load. At light load, ZVS is lost, resulting in poor efficiency. Due to these limitations, it is difficult to use CCM ACF at high switching frequency.

Critical conduction mode (CrCM) ACF [4] allows magnetizing current to become negative during each switching cycle. Unlike CCM flyback that relies on leakage inductance, CrCM utilizes the magnetizing inductance to store ZVS energy. As magnetizing inductance is much larger than leakage inductance, only small amount of negative magnetizing current is needed to achieve full ZVS soft switching. By controlling the amount of negative magnetizing current, ZVS can easily be achieved from zero to full load. With proper design, the output rectifier will achieve zero current switching (ZCS) during turn-off, which means zero rectifier current before reverse voltage is applied. When leakage inductance energy is fully recovered and the rectifier snubber is no longer needed, CrCM ACF can switch very efficiently at 1 MHz using GaN switches and a planar transformer [5][6].

Optimal design and operation of CrCM ACF have not been widely discussed, especially when SR is used. Analytical expressions of ACF operation have been documented in [9][10], ignoring the output capacitance of SR MOSFET. In reality, large output capacitance of SR MOSFET can significantly alter converter operation. A thorough study of CrCM ACF operation, including parasitic effects is given in Section II. As traditional ACF resonant schemes cannot achieve secondary SR ZCS consistently, a secondary side resonant method is proposed in Section III to re-shape transformer current in a way that reduces rms current and allows easy SR implementation.

Another reason that ACF has not yet been adopted in compact and cost sensitive adapter market is the need for a high speed half-bridge driver and fast switches. Recent developments in GaN Power IC [7][8] solve the 'ease-of-use' problem for ACF. This paper provide an example showing highly-integrated GaN IC that includes all essential power stage functions in a small package to enable efficient, high frequency, high density adapter design (Sections IV).

II. Analysis of ACF Considering Parasitic Capacitances

A. Steady-State Operation of Active Clamp Flyback

An ACF is drawn in Fig. 1. L_m is the transformer magnetizing inductance. L_r is the resonant inductor, which may be the transformer's leakage inductance. S1 and S2 are switches with their output capacitance C_{oss} shown. S3 is the secondary SR switch with C_j representing its output capacitance. C_p is the transformer winding capacitance. C_r and C_o are the primary clamp capacitor and output capacitor.

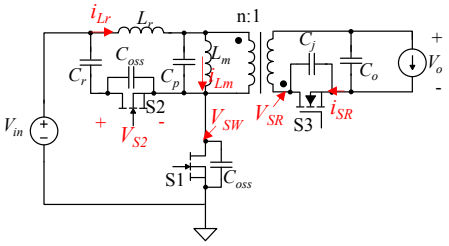


Fig. 1. Active clamp flyback with parasitic capacitors

Fig. 2 shows ACF waveforms. The power delivery is similar to a traditional single-switch flyback, which can be divided into two intervals (S1 ON and S1 OFF). The magnetizing inductance L_m is charged during S1 ON interval, and discharged during S1 OFF interval, delivering power to the load. The voltage conversion ratio is derived as (1)

$$D = \frac{nV_o}{nV_o + V_{in}} \tag{1}$$

where D is the duty cycle of S1, V_o is output voltage, V_{in} is input voltage, and n is the transformer turns ratio as shown in Fig. 1.

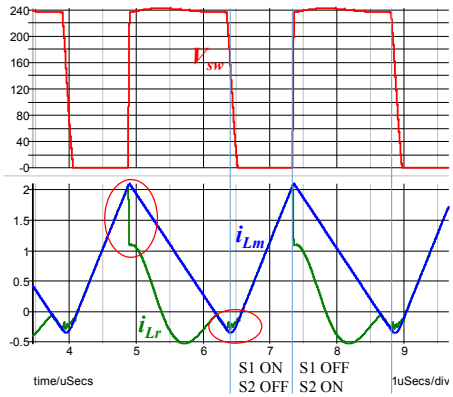


Fig. 2. Simulated primary current with secondary parasitic capacitance considered

The clamping switch S2 toggles complementarily with respect to S1, storing L_r energy to C_r after S1 turns off and allowing L_r and L_m current to flow in negative direction (as defined in Fig. 1) to allow ZVS turn-on of S1. As magnetizing current drops below zero (as illustrated in Fig. 2), majority ZVS energy is contributed from magnetizing inductance. Therefore, the L_r value can be minimized as the transformer leakage inductance. In the following derivations, $L_r << L_m$ is assumed to simplify expressions. The average value of magnetizing current equals

$$I_{Lm(avg)} = I_{Lr(avg)} + I_{S3(avg)} = \frac{P_o}{\eta V_{in}} + \frac{I_o}{n} \tag{2}$$

where P_o is output power, I_o is output current, and η is ACF efficiency. The peak and valley values of magnetizing current are obtained as

$$I_{Lm(\max)} = I_{Lm(avg)} + \frac{V_{in}D}{2f_sL_m} \tag{3}$$

$$I_{Lm(\min)} = I_{Lm(avg)} - \frac{V_{in}D}{2f_sL_m} \tag{4}$$

The negative magnetizing current is usually controlled to provide just enough energy to achieve ZVS to minimize rms current. L_m selection is documented in [12].

The steady state clamping capacitor C_r voltage is given by

$$V_{Cr} = nV_o + V_{in} \cdot \frac{L_r}{L_r + L_m} \cdot \frac{D}{1-D} \approx nV_o \tag{5}$$

In most analysis, V_{Cr} voltage can be approximated as a constant voltage source.

B. Primary Transformer Current Dip at S1 Turn-off

From Fig. 2, we can see the primary current i_{Lr}, has a dip immediately after S1 turns off. This dip sets an initial condition of the resonant process during S1 OFF period, impacting both i_{Lr} rms value and ZCS condition of SR S3, which will be discussed later. This section focuses on the current dip phenomenon.

At S1 turn-off, primary current i_{Lr} equals to the peak of magnetizing current $i_{Lm(max)}$, which stays constant during this transition period. Assuming $L_r << L_m$, inductor current i_{Lr} can be solved as

$$i_{Lr} \approx I_{Lm(\max)} \cdot \frac{2C_{oss}}{2C_{oss} + C_{pj}} + (I_{Lm(\max)} \cdot \frac{C_{pj}}{2C_{oss} + C_{pj}}) \cdot \cos(\omega_r t) \tag{6}$$

$$\omega_r = 1/\sqrt{\frac{2C_{oss}C_{pj}}{2C_{oss} + C_{pj}} \cdot L_r} \tag{7}$$

$$C_{pj} = C_p + C_j / n^2 \tag{8}$$

According to (6), the primary current i_{Lr} will resonate away from a peak following a cosine function towards a steady-state current determined by the divider effect between primary capacitances ($2C_{oss}$) and secondary capacitances (C_{pj}). The maximum possible current dip can be obtained as

$$I_{dip(\max)} = I_{Lm(\max)} \cdot \frac{2C_{pj}}{2C_{oss} + C_{pj}} \tag{9}$$

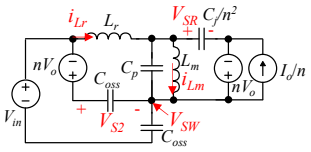


Fig. 3. Equivalent circuit of the resonant process after S1 turns off

The maximum dip in (9) happens when resonance lasts longer than half of the resonant period. In fact, this resonant process ends under one of the following conditions: 1) C_{oss} of S2 fully discharged and S2 starts freewheeling, 2) C_j is fully discharged and S3 starts freewheeling. In order to determine which happens first, the voltage of V_{S2} and V_{SR} are derived as

$$V_{S2} = V_{S,lin} - I_{Lm(\max)} \cdot \frac{C_{pj}}{2C_{oss} + C_{pj}} \cdot \frac{1}{\omega_r \cdot 2C_{oss}} \sin(\omega_r t) \tag{10}$$

$$nV_{SR} = V_{S,lin} + I_{Lm(\max)} \cdot \frac{C_{pj}}{2C_{oss} + C_{pj}} \cdot \frac{1}{\omega_r C_{pj}} \sin(\omega_r t) \tag{11}$$

$$V_{S,lin} = V_{in} + nV_o - I_{Lm(\max)} \cdot \frac{t}{2C_{oss} + C_{pj}} \tag{12}$$

Typical waveforms of V_{S2} and V_{SR} governed by (10)-(12) are plotted in Fig. 4. A complete resonant cycle is shown for clearer explanation but the resonance in fact ends when either voltage drops to zero. The resonant voltage waveforms center around the linear term in (12). Three waveforms intersect with each other at every half resonant period ($T_r/2 = \pi/\omega_r$). V_{S2} slews faster than V_{SR} initially because of the assistance of L_r current. Without the inductance L_r, C_{oss} and C_j would be effectively in parallel and discharged linearly following $V_{S,lin}$ in (12). The time required before the voltages reduce to zero can be solved as T_x by making (12) to zero. From Fig. 4, we can see that if $T_x < T_r/2$, primary voltage V_{S2} will be discharged to zero first; if $T_x > T_r/2$, the secondary voltage V_{SR} will reach zero first. In either case, a new resonant process starts from the current state of initial conditions, with reduced number of resonant elements, and continues until both primary and secondary capacitances are fully discharged. Some special cases are given below.

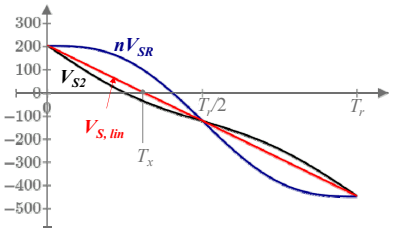


Fig. 4. Voltage transition curves of S2 and S3 during the current dip

Typical current dip waveforms are simulated with different T_x and $T_r/2$ relationship in Fig. 5(a). Three are simulated with different C_{oss} and C_{pj} values but the same C_{oss}/C_{pj} ratio in order to ensure identical maximum current dip in (9). Note the maximum current dip only occurs when the resonance lasts longer than half of the resonant period ($T_x \geq T_r/2$). If $T_x < T_r/2$, the current dip is lower, in fact if T_x is small enough ($<T_r/8$), $\sin(\omega_r t) \approx \omega_r t$, equation (10) can be simplified into

$$V_{S2} = V_{in} + nV_o - I_{Lm(\max)} \cdot \frac{t}{2C_{oss}} \tag{13}$$

which means the primary capacitance is charged linearly without participating in the resonance. The resonance expressions can be simplified into

$$i_{Lr,simp}(t) = I_{Lm(\max)} - \frac{V_{in} + nV_o}{Z_{r1}} \sin(\omega_{r1} t) \tag{14}$$

$$nV_{SR,simp}(t) = (V_{in} + nV_o)\cos(\omega_{r1} t) \tag{15}$$

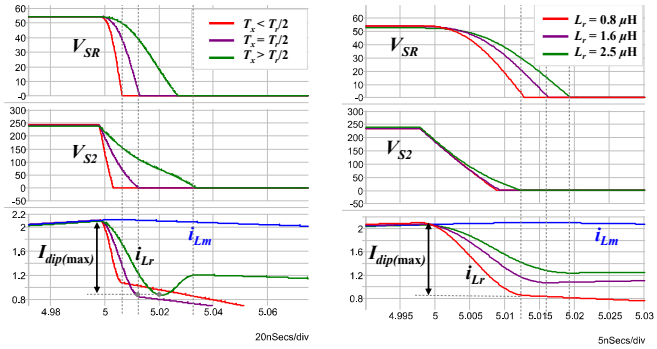
$$Z_{r1} = \sqrt{L_r / C_{pj}}\,,\ \omega_{r1} = 1/\sqrt{C_{pj} L_r} \tag{16}$$

The current dip under this condition can be solved as

$$I_{dip,simp} = (V_{in} + nV_o)/Z_{r1} \tag{17}$$

Please note that (17) can only be used under $T_x < T_r/2$ condition for estimation, $T_x > T_r/2$ should use (9).

Leakage inductance L_r impacts the current dip by changing the resonant period T_r. As shown in Fig. 5 (b), larger L_r value leads to a deeper ($T_x < T_r/2$) condition and smaller current dip, which also verifies (17).



(a) (b)

Fig. 5. Typical waveforms of primary current dip: (a) with different relationship of T_x and $T_r/2$, which indicates whether V_{S2} or V_{SR} discharges to zero first; (b) with different leakage inductance L_r

In summary, the primary current dip is caused by the current divider effect between primary and secondary capacitance, with the maximum determined by the capacitance ratio. The larger equivalent capacitance C_{pj} with respect to primary switch C_{oss}, the bigger the current dip. This phenomenon is more pronounced when GaN primary switches are used, as GaN C_{oss} is very small.

This current dip significantly affects transformer primary side rms current. This effect can be utilized to reduce conduction losses of transformer and clamp switch. Fig. 6 shows the simulated primary and secondary conduction losses that are normalized at C_j=100 pF, assuming the resistances stay constant. We can see that by changing the secondary capacitance from 100 pF to 2 nF, the primary loss reduced by 40% while the secondary loss increases by only 10%. To take advantage of this effect, ACF can use low Rdson SR MOSFET that has large Coss.

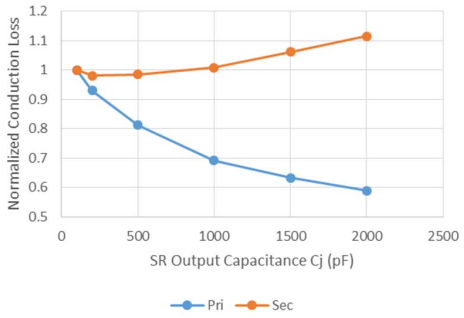


Fig. 6. Simulated normalized conduction loss vs. SR output capacitance

C. Primary Current Ripple at S2 Turn-off

A similar current dip occurs during the ZVS transition after S2 turns off, as observed in Fig. 2. The resonance equivalent circuit is the same as S1 turn-off (Fig. 3), but with different initial conditions. Similar solutions are obtained:

$$i_{Lr} \approx I_{Lm(\min)} \cdot \frac{2C_{oss}}{2C_{oss}+C_{pj}} + (I_{Lm(\min)} \cdot \frac{C_{pj}}{2C_{oss}+C_{pj}}) \cdot \cos(\omega_r t) \quad (18)$$

$$V_{sw} = V_{S,lin} + I_{Lm(\min)} \cdot \frac{C_{pj}}{2C_{oss}+C_{pj}} \cdot \frac{1}{\omega_r \cdot 2C_{oss}} \sin(\omega_r t) \quad (19)$$

$$nV_{SR} = \frac{-I_{Lm(\min)} t}{2C_{oss}+C_{pj}} + \frac{I_{Lm(\min)}}{(2C_{oss}+C_{pj})\omega_r} \cdot \sin(\omega_r t) \quad (20)$$

$$V_{S,lin} = V_{in} + nV_o + I_{Lm(\min)} \cdot \frac{t}{2C_{oss}+C_{pj}} \quad (21)$$

Again, L_r current reduces due to the current divider effect between primary and secondary capacitance. High ratio of C_{pj}/C_{oss} raises the current and increases the ringing amplitude. As $i_{Lm(min)}$ value is usually small during this transition, the maximum dip with high C_{pj}/C_{oss} ratio may make L_r current positive, changing V_{sw} slope, as shown in Fig. 7 (green curve). Smaller capacitance ratio lowers the ringing magnitude and the voltage transition becomes almost linear with C_{pj}/C_{oss}=0.5.

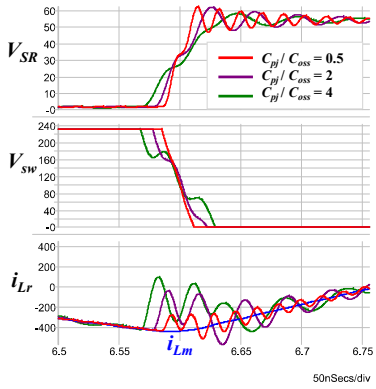


Fig. 7. Primary current dip after S2 turns off at different primary-secondary capacitance ratios

Though ZVS transition may not look clean, this Vsw ringing does not slow down ZVS transition or create switching loss. Due to very low i_{Lm}, the voltage transition takes multiple resonant cycles to complete, so it is less sensitive to the phase of the resonance and more dominated by the linear term of (19) and (20). In contrast, the voltage transition of S1 turn-off edge, where i_{Lm} is high, usually complete within one resonant cycle (T_r), making ZVS transition smooth and clean.

D. Primary Side Resonant Process

This section will analyze the resonant process during S1 OFF (S2 ON) period in Fig. 2. At the end of current dip when both primary and secondary capacitances (C_{oss} and C_{pj}) have been fully charged or discharged, S2 and S3 start conducting currents. L_r resonates with C_r and the difference between L_r current i_{Lr} and magnetizing current i_{Lm} is delivered to the secondary side (i_{SR}). The equivalent circuit is drawn in Fig. 8.

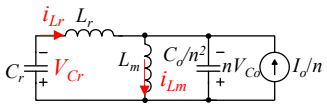


Fig. 8. Equivalent circuit of L_r and C_r resonant process

The initial primary current $I_{Lr(ini)}$ can be solved by (9) when $T_x > T_r/2$ and (17) when $T_x < T_r/2$. Inductor current can be solved as

$$i_{Lr}(t) = I_{Lr(ini)} \cos(\omega t) + \frac{nV_o - V_{Cr(ini)}}{Z} \cdot \sin(\omega t) \quad (22)$$

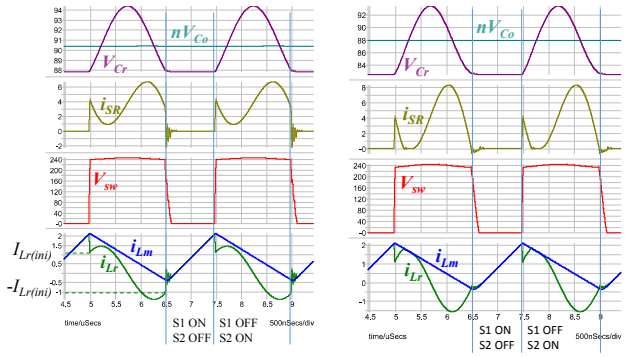
$$\omega = \frac{1}{\sqrt{C_r \cdot L_r}}, \; Z = \sqrt{\frac{L_r}{C_r}} \quad (23)$$

where $V_{Cr(ini)}$ is the initial voltage of the resonant capacitor C_r, which can be solved as (3) according to charge balance of C_r

$$V_{Cr(ini)} = nV_o - \frac{I_{Lr(ini)} Z}{\tan(\theta)}, \theta = \pi - \frac{1-D}{2f_s\sqrt{L_r C_r}} \quad (24)$$

By combining with (22), (23) and implementing the law of charge balance, we know that at the end of this interval, i_{Lr} should be $-I_{Lr(ini)}$, as shown in Fig. 9 (a).

If i_{Lr} is more negative than i_{Lm}, S3 current (i_{SR}) will be positive, when S2 is turned off. SR FET S3 will be forced off still with current conducting. Unless SR controller is extremely fast and precise, SR may be forced to turn off early and allow its body diode to conduct current, resulting in reverse recovery loss and voltage ringing; or SR may be turned off late and allow shoot through current, resulting in large voltage overshoot and power loss. Ideally SR commutating scheme is to reduce SR current gradually to zero before primary side ZVS transition, thus providing ample time for SR controller to turn off S3. This control scheme is called zero current switching (ZCS), which makes SR control easier and allows clean SR waveform without need for a snubber.



(a) (b)

Fig. 9. ACF waveforms: (a) without secondary ZCS; (b) with secondary ZCS

For high frequency ACF, SR ZCS turn-off is preferred. Reducing the C_r capacitance shortens the resonant period and accelerates i_{Lr} to merge with i_{Lm}, achieving ZCS for the SR switch S3, as shown in Fig. 9 (b). However, i_{Lr} sometimes oscillates too high and touches i_{Lm} shortly after the resonance begins, reducing SR current to zero temporarily during the "S1 OFF" interval. This effect can confuse SR controller to turn off SR early, resulting in long body diode conduction and instability of control feedback or circuit operation. This current double dipping effect is hard to contain through SR controller's blanking circuit. More importantly, to achieve ZCS at end of switching cycle, the resonant current i_{Lr} amplitude is higher in Fig. 9 (b) than that in Fig. 9 (a), which leads to higher rms current and increases the conduction losses of clamp switch S2 and transformer. This effect gets worse with larger leakage inductance L_r, which reduces transformer design flexibility.

In summary, to achieve ZCS for secondary side SR switch, existing ACF topology with primary side resonance has drawbacks of SR double switching and high primary rms current, which leads to high SR loss and high conduction loss.

III. Secondary Side Resonance Scheme

The proposed secondary side resonance scheme uses a small-capacitance C_o as the resonant element. The topology is the same as Fig. 1. The voltage ripple across C_o will be high, so a second stage LC filter may be needed. The C_o capacitor in this scheme should be a high-quality ceramic capacitor with low ESR. Clamp capacitor is large in this case, and clamp voltage is considered constant.

The secondary-resonant ACF waveforms are shown in Fig. 10. The operation waveforms are the same during S1 ON period. When S2 and S3 start conducting, L_r resonates with the output capacitor C_o and C_r, with the equivalent circuit in Fig. 8. Since C_r has a very large capacitance, the resonant will be dominated by C_o, so this scheme is named as a secondary-resonant scheme.

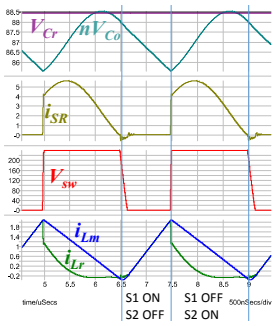


Fig. 10. ACF waveforms with secondary resonant scheme

The inductor current i_{Lr} can be solved as

$$i_{Lr}(t)=\left(\frac{nV_o}{\omega L_m}+\frac{nV_{o(ini)}-V_{Cr}}{Z}\right)\cdot\sin(\omega t) -\left(I_{Lm(\max)}-\frac{I_o}{n}-I_{Lr(ini)}\right)\cdot\cos(\omega t)+\left(I_{Lm(\max)}-\frac{I_o}{n}-\frac{nV_o}{L_m}\cdot t\right) \tag{25}$$

$$\omega=\frac{1}{\sqrt{L_{lk}\cdot C_o/n^2}},\quad Z=\sqrt{\frac{L_{lk}}{C_o/n^2}} \tag{26}$$

where V_{Cr} is the voltage across C_r, and is treated as constant, $V_{o(ini)}$ is the initial voltage of the output capacitor, whose solution depends on when the i_{Lr} current meets i_{Lm} and can be very complicated. In real applications, it is preferred to let i_{Lr} touch i_{Lm} as close as possible to the end of the "S1 OFF" period in order to minimize rms current and conduction loss. Therefore, it is reasonable to assume i_{Lr} touches i_{Lm} right at the end of the "S1 OFF" period. Then $V_{o(ini)}$ can be solved as (27) by implementing the charge balance of C_r

$$nV_{o(ini)}-V_{Cr}=\frac{\left(I_{Lm(\max)}-\frac{I_o}{n}-I_{Lr(ini)}\right)\cdot Z\cdot\sin[\omega(1-D)T_s]-\omega DT_sI_oZ/n}{1-\cos[\omega(1-D)T_s]}-\frac{nV_oL_r}{L_m} \tag{27}$$

Substituting (27) into (25), the resonant inductor current can be obtained as

$$i_{Lr}(t)\approx\frac{-\omega DT_sI_o/n}{1-\cos[\omega\cdot(1-D)T_s]}\cdot\sin(\omega t) -\left(I_{Lm(\max)}-\frac{I_o}{n}-I_{Lr(ini)}\right)\cdot\cos(\omega t)+\left(I_{Lm(\max)}-\frac{I_o}{n}-\frac{nV_o}{L_m}\cdot t\right) \tag{28}$$

From Fig. 10, i_{Lr} is always lower than i_{Lm} until the end of the "S1 OFF" interval. Accordingly, the secondary current i_{S3} will not double dip to zero, comparing to the traditional primary-resonant scheme, as shown in Fig. 9(b). This secondary-resonant scheme can thereby eliminate the double-turn-off issue of SR switch, achieving reliable SR operation and improving ACF efficiency.

In (28), the first two terms constitute a resonant function superimposed to the last term, a linear-reducing function. Equation (28) is plotted in Fig. 11 with magnetizing current i_{Lm}. The dashed green line represents the linear reducing term in (28). i_{Lr} resonance is centered around the linear decreasing term, makes the current "flat" at the bottom, which reduces rms current.

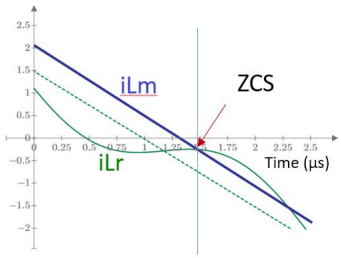


Fig. 11. In the secondary resonant scheme, i_{Lr} resonates around a linear decreasing line, therefore has lower rms value.

Primary-resonant and secondary resonant schemes are simulated at 20 V / 2.25 A output, transformer turns ratio=26:6, and L_r = 900 nH. Four cases (a-d) with different primary and secondary resonant capacitances are compared. The parameters are summarized in TABLE IThe equivalent resonant capacitance C_{eq} is defined as

$$C_{eq} = \frac{C_r \cdot C_o / n^2}{C_r + C_o / n^2} \tag{28}$$

The waveforms shown in Fig. 12 are summarized in TABLE I.

TABLE I COMPARISON OF PRIMARY AND SECONDARY RESONANT SCHEMES

	Resonant Type	***C_r (μF)***	***C_o (μF)***	***C_{eq} (μF)***	***$I_{Lr,rms}$ (mA)***	***$I_{SR,rms}$ (A)***	***ZCS***
(a)	Primary	0.08	1880	0.08	1157	3.72	Yes, optimal
(b)	Secondary	100	1.5	0.08	744	4.13	Yes, not optimal
(c)	Primary	0.213	1880	0.213	--	--	No
(d)	Secondary	100	4	0.213	727	3.23	Yes, optimal

Fig. 12 (a) shows a primary resonant case (C_r = 80 nF, C_o = 1.88 mF) with optimal ZCS in which i_{Lr} touches i_{Lm} at the end of S2 conduction interval, minimizing rms current. With the same equivalent capacitance C_{eq}, secondary resonant in Fig. 12 (b) has achieved ZCS much earlier. This means the secondary resonant scheme is more consistent than the primary scheme in realizing ZCS. This is also proved by the comparison of cases (c) and (d) with C_{eq} = 213 nF, when secondary resonant case (d) achieves optimal ZCS in Fig. 12 (d), case (c) loses ZCS.

The primary and secondary rms currents $I_{Lr,rms}$ and $I_{SR,rms}$ are also compared in TABLE IFrom case (a) to case (b), the primary rms current has reduced by 36% while the secondary rms current has increased by 11% due to non-optimized ZCS. Case (d) with optimal ZCS achieves 37% and 13% reduction on $I_{Lr,rms}$ and $I_{SR,rms}$, respectively.

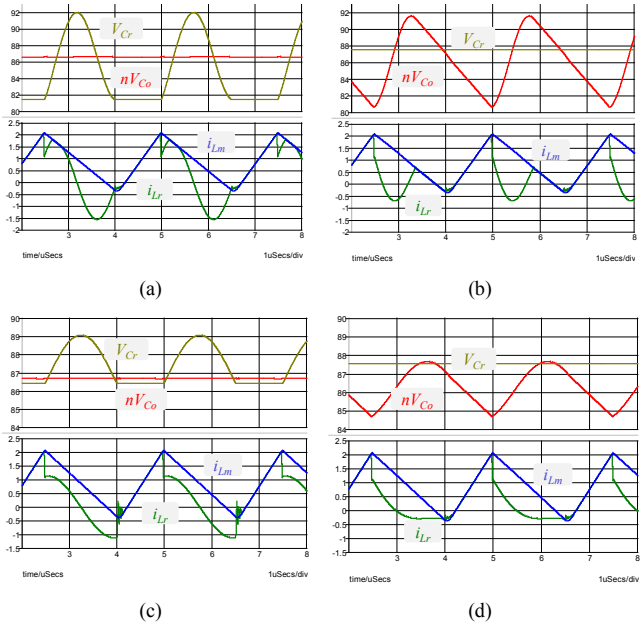


Fig. 12. Waveform comparison between primary-resonance and secondary-resoant schemes. Simulation parameters are listed in TABLE I

More simulations were carried out at different input voltages. Fig. 13 plots the rms current reduction achieved by using secondary-resonant scheme over the conventional primary-resonant scheme. We can see the reduction of resonant current i_{Lr} is above 30% over wide input voltage range, and the reduction of secondary SR current i_{SR} is about 15% over wide input voltage range. This rms current savings will directly translate into conduction loss reductions.

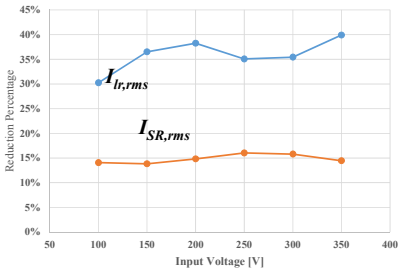


Fig. 13. Rms current reduction by using secondary-resonant scheme over primary-resonant scheme

If the C_r capacitance is comparable to C_o/n^2, both capacitors will participate in the resonant process with inductor L_r. Since this scheme has both primary resonance and secondary resonance, it is named as mixed-resonant scheme. A mixed-resonant scheme provides additional freedom to shape the current waveform to improve efficiency.

IV. EXPERIMENTAL RESULTS

A 45W, 20V adapter was built using GaN Power ICs and bobbin-based transformers using an off shelf ACF controller.

The major components are listed in TABLE II, with simplified schematic shown in Fig. 14.

Discrete eMode GaN FETs are very fast, and are ideal for high frequency ACF [5, 6] but are difficult to drive, especially in half-bridge configuration. Often, daughter cards are used, with additional supporting components such as digital isolators, floating bias supplies and buffer drivers to make eMode GaN work properly. A GaN Power IC monolithically-integrates all power stage functions (FET, driver and logic) in a small footprint, allowing the use of low-cost, single-sided SMD assembly process. NV6260 is a 150mΩ half bridge GaN IC from Navitas Semiconductor. It will be used to prototype a 45W ACF adapter using the secondary side resonance scheme.

TABLE II MAJOR COMPONENTS

	Part Number
Primary FETs	NV6260 (160 mΩ eMode GaN half-bridge Power IC)
Secondary SR FET	BSC160N15NS5ATMA1 (150V, 16 mΩ)
Bulk Capacitors	UCY2G390MHD9 (400 V, 39 μF) x2
Transformer	RM8/LP, N49, 21:4
ACF Controller	UCC2894PW

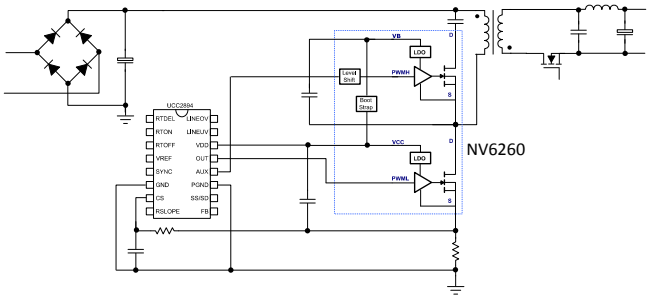


Fig. 14. 45W adapter simplified schematics

The measured waveforms are shown in Fig. 15(a). Whenever primary current dips below the magnetizing current, the secondary winding outputs current. The shape of the secondary current is the area below the imagined L_m current in dashed line. When the primary current recovers to the magnetizing current, secondary winding current reduces to zero, and the SR FET turns off under ZCS. The bottom two figures show the zoomed-in waveforms of the switching transition. In the middle figure, V_{sw} and V_{SR} complete transition simultaneously at the point where the maximum current dip happens, which matches with the $T_x = T_r/2$ case in Fig. 5. From the bottom figure, we can see only 200 mA negative current is enough to achieve ZVS, due to extremely low output capacitance of GaN switches.

In order to verify the current dip theory, an external 2.2 nF capacitor was paralleled to the SR FET to increase the C_{pj}/C_{oss} ratio. The measured waveforms under the same operating condition in Fig. 15 (b) show much bigger current dips at both S1 turn-off edge and S2 turn-off edge, as more current is diverted to the secondary side during the resonance. The bigger current dip reduces the i_{Lr} rms value from 744 mA to 660 mA.

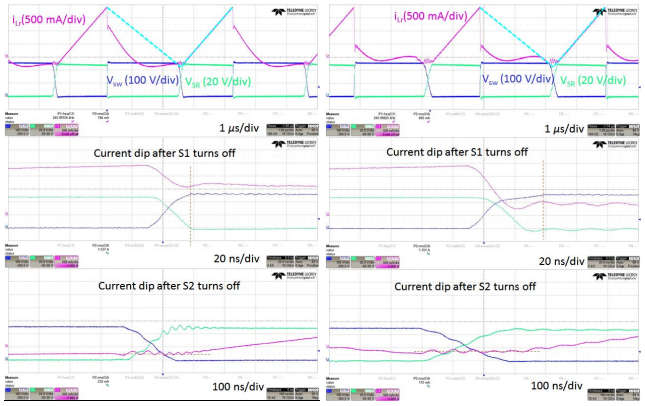


Fig. 15. Active clamp flyback waveforms tested at 150 Vdc: (a) without external C_j; (b) with 2.2 nF external C_j

Primary and secondary resonant schemes were also compared experimentally. For the primary resonant, C_r =100 nF and C_o = 110 μF. For the secondary resonant, C_r = 330 nF and C_o = 10 μF, with a 1 μH inductor and 100 μF bulk capacitor inserted to filter output voltage ripple. In all the testing conditions, duty-cycle and switching frequency are constant for fair comparison. Waveforms in Fig. 16 show that secondary resonant scheme has lower primary rms current. By using secondary resonant scheme, efficiency improvement is up to 1.5%, as shown in Fig. 17.

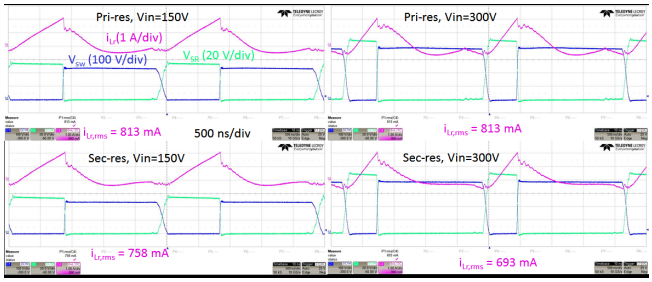


Fig. 16. Primary and secondary resonant schemes lead to different primary rms current

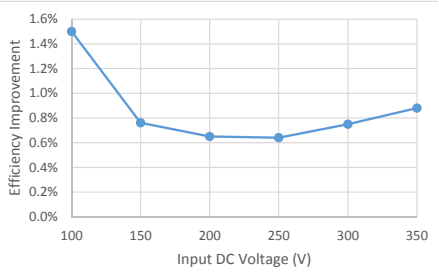


Fig. 17. Efficiency improvement by using secondary resonant scheme over primary resonant scheme. Measured from 45W ACF converter at different input DC voltages.

Fig. 18 shows the full-load efficiency at different AC input voltages. Switching frequency was adjusted with ac line

voltage to achieve best efficiency. The worst-case efficiency at 90 V_{ac} is 93.1%. Fig. 19 shows the prototype photos. Power density of 25 W/in^3 (uncased) is achieved. Thermal images in Fig. 20 show the worst case temperature was 68.1 °C at the diode bridge. Conductive peak EMI was measured with max hold enabled (Fig. 21).

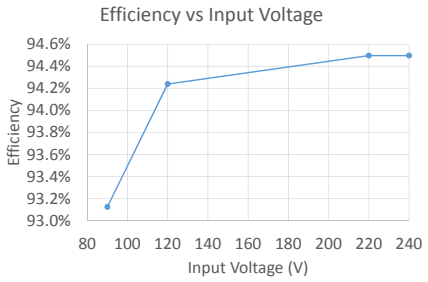


Fig. 18. Efficiency at differnet input voltage

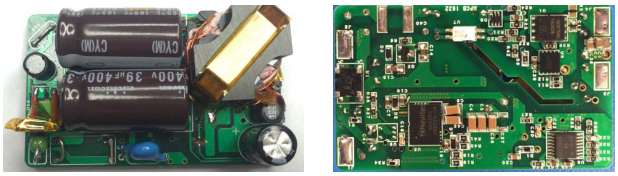


Fig. 19. 45W adapter with 2.22 x 1.32 x 0.62 in: power density 25 W/in^3

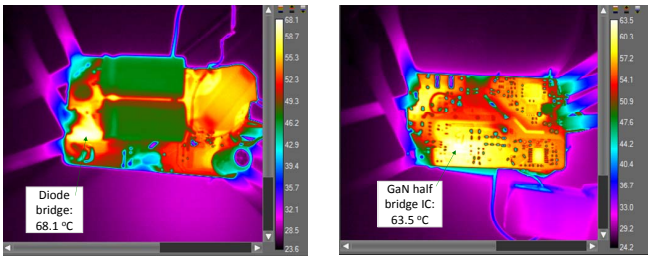


Fig. 20. Thermal performance at 90V_{ac} (no thermal compound, heatsink or spreader)

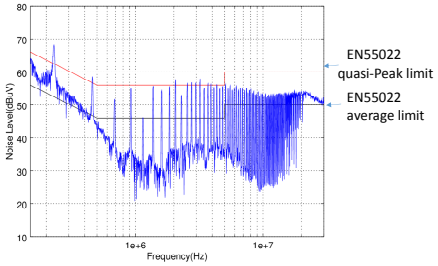


Fig. 21. Conductive EMI (peak max hold)

V. CONCLUSION

Active clamp flyback is analyzed and optimized, and performance is demonstrated in a 45 W adapter. Detailed equivalent circuits are provided to model the transformer current waveforms including the effect from secondary side SR output capacitance. New secondary side resonance scheme reduces rms current and improves SR operation. GaN Power ICs, with monolithic-integration of FET, drive and logic, simplifies ACF design and layout, achieving 25 W/in^3 power density and 93% efficiency with a cost-effective PCB and assembly.

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