1 Introduction

This document provides system design information for the TI Active Cell Balancing chipset. The information provided here should be used in addition to the device datasheets.

2 Table of Contents

3 Conventions and Acronyms

This section describes the conventions and acronyms used in this document.

3.1 Conventions

'0'	Binary digit zero; a logic low level (a low voltage for active high logic, and a high voltage for active low logic)
'1'	Binary digit one; a logic high level (a high voltage for active high logic, and a low voltage for active low logic)
"d…"	A binary number with more than one digit (d is 0-1)
d…	A decimal number (d is 0-9)
0xd…	A hexadecimal number (d is 0-F)
d..h	A hexadecimal number (d is 0-F)
k	kilo; 1000
K	kilo; 1024 (note: this is not official SI usage)
b	bit
B	byte

3.2 Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front End
BMS	Battery Management System
BSP	Battery Stack Protection
CAN	Controller Area Network
DAC	Digital to Analog Converter
EEPROM	Electrically Erasable Programmable Read Only Memory
GPIO	General Purpose Input Output
MCU	Micro-Controller Unit
OC	Over Current
OV	Over Voltage
OVP	Over Voltage Protection
PWM	Pulse Width Modulation
Stack	Series connection of cells managed by the BMS
SPI	Serial Peripheral Interface
UV	Under Voltage
UVP	Under Voltage Protection

3.3 Chipset Components

The core active balancing components are shown in Table 1.

IC	Description	Quantity Required		Order number
		up to 7 cells	8 to 14 cells	
EMB1432	Analog Front End (AFE)	1	1	EMB1432QSQ
EMB1426	ADC	1	1	EMB1426QMM
EMB1428	Gate Controller	1	2	EMB1428QSQ
EMB1499	PWM Controller	1	2	EMB1499QMH
EMB1412	Gate Driver	1	2	EMB1412MY
EMB1433	Battery Stack Protection	1	1	EMB1433QSQ

Table 1 - Active Chipset IC List

Additional components that are part optional are listed in Table 2.

IC	Description	Quantity Required		Order number
		up to 7 cells	8 to 14 cells	
EMB1420	Flyback Controller (12V)	1	1	EMB1420MM
EMB1437	12V LDO	1	2	EMB1437MP
EMB1487	-5V Chargepump	1	1	EMB1487MM
EMB1466	Dual 5V LDO	1	1	EMB1466MM
EMB1464	Dual Switching Regulator	1	1	EMB1464MH
EMB1402	12-bit ADC (temp sense)	1	1	EMB1402QMT

Table 2 - Active Chipset Optional Items

3.4 External Hardware Dependencies

Typically an external microcontroller is used to initialize the EMB1432 and EMB1428, initiate new actions by these devices, and collect data from these integrated circuits. It may also be necessary to report data and provide a command and/or control protocol on an isolated communications interface.

3.5 Microcontroller

A microcontroller is suggested to provide the peripheral interfaces and IO required to control the system. The required peripherals are:

- SPI
- 2x DAC or timers with PWM output capability
- External communications interface for control command and measurement data
- Sufficient data memory for desired communications protocol layer and data buffering
- Sufficient non-volatile program memory for the system initialization routines, peripheral drivers and control algorithms
- Non-volatile memory (Flash or external EEPROM) for system configuration and calibration parameters

- 14+ GPIO (depending on cell count and system options, see Appendix C for a complete list of chipset interface signals)

Other optional features:

- Non-volatile memory (Flash or EEPROM) for long-term data log retention
- ADC for additional system fail-safe monitoring and/or temperature sensors with the pack
- Additional GPIO may also be required to control the power supplies if advanced features are required (see Section 13.1)

The EM1401 Battery Management System Evaluation Board has used the TI Stellaris LM3S5R31-IQC.

It is recommended to also use an external reset controller to provide a reliable power-on and brown-out reset signal. The EMB1424MF is recommended.

3.5.1 Isolation

Any connection from battery modules to a central pack controller will need to be isolated to withstand the maximum working voltage of the entire pack in compliance with any system standards.

3.5.2 Transceivers

Depending on the desired communications protocol, and to achieve robust, error-free communication, transceivers may be required.

4 System Critical Circuits

This section describes circuits that are global in nature and require by more than one device in the chipset.

4.1 Zener Diodes

Zener diodes are required to be placed close to the external battery connection on the system PCB, with one zener diode across each cell. The zener diodes are necessary to the system and serve 2 functions:

1. Provide overvoltage protection to the AFE inputs
2. Provide a path for in-rush currents during hot plug-in

The zener diode schematic can be seen in Figure 1 and shows the direct connection to the battery connection header.

The zener diodes should be selected to ensure the following conditions are met:

1. The EMB1432 and EMB1433 inputs are protected from input voltage transients and kept below 6V.
2. The zener current (I_z) at normal battery cell voltage levels is as low as possible to keep the quiescent current low.

For example, the zener diodes used in the active chipset reference schematic are 5.6V, which has a Iz ≈ 7uA at 4.2V.

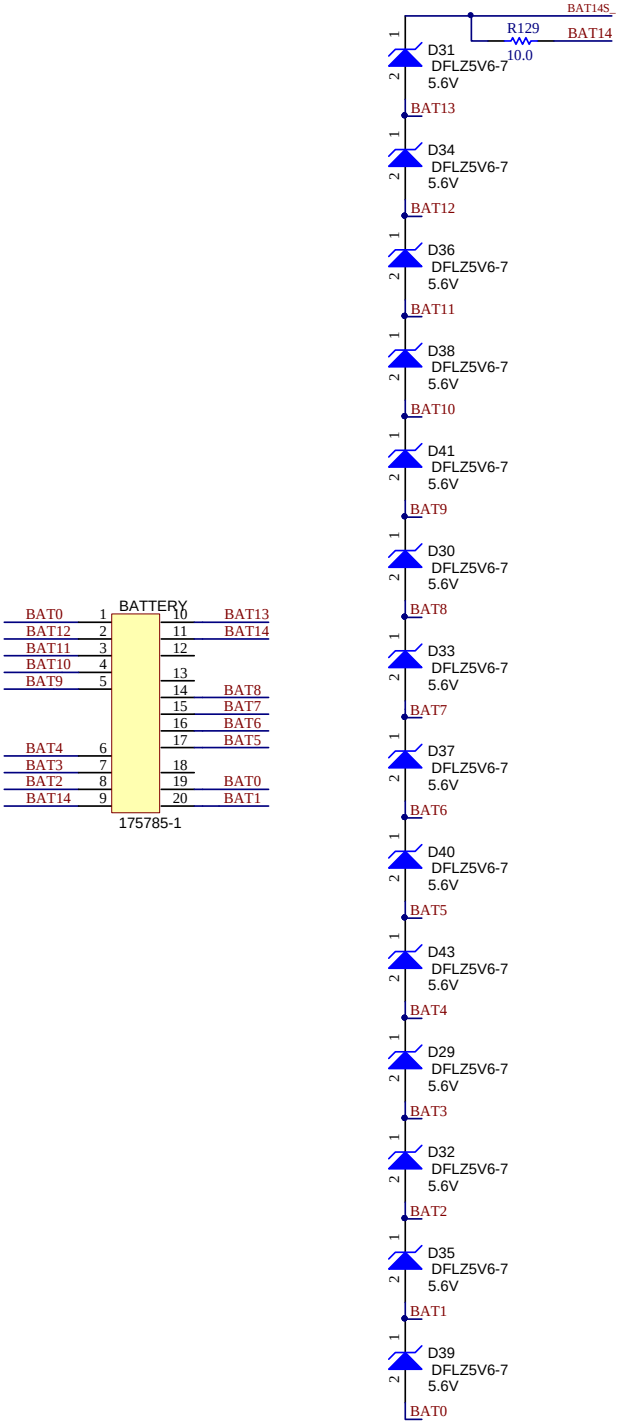


Figure 1 - Zener Diode Schematic

4.2 In-Rush Protection

Protection circuits are required to limit the in-rush circuit which will occur when the battery connections are first made to the system. There are 2 circuits required in the system:

1. In-rush current limit to protect the internal ESD protection diodes in EMB1432 and EMB1433.
2. In-rush current limiting for the FET switch-matrix.

The in-rush current protection for the EMB1432 can be seen in Figure 1, as R129 on the EMB1432 BAT14 pin.

There is also a need to limit the in-rush current into the FET switch matrix which occurs when the system in first plugged in to battery pack. The schematic for this circuit can be found in Figure 2. The basic operation is that at first power-up, all in-rush current will pass through R166 (22Ω), until R166 is bypassed by the FET Q46. The system microcontroller is expected to enable Q46 before any active cell balancing is enabled.

4.3 Battery Connection Fuses

For safety purposes, it is recommended to include a 12A fuse on cell 7+ (BAT7), and 8A fuses on all other cell connections. Cell 7 requires a higher fuse value as it is possible for cell 7 to see a sum of 10A, with 5A of current from the top half-stack and 5A of current from the bottom half-stack. These fuses can be seen as F1 – F15 in Figure 2.

4.4 Stack Transient Suppression Diode

The transient suppression diode (TVS) can be seen as D42 in Figure 2.

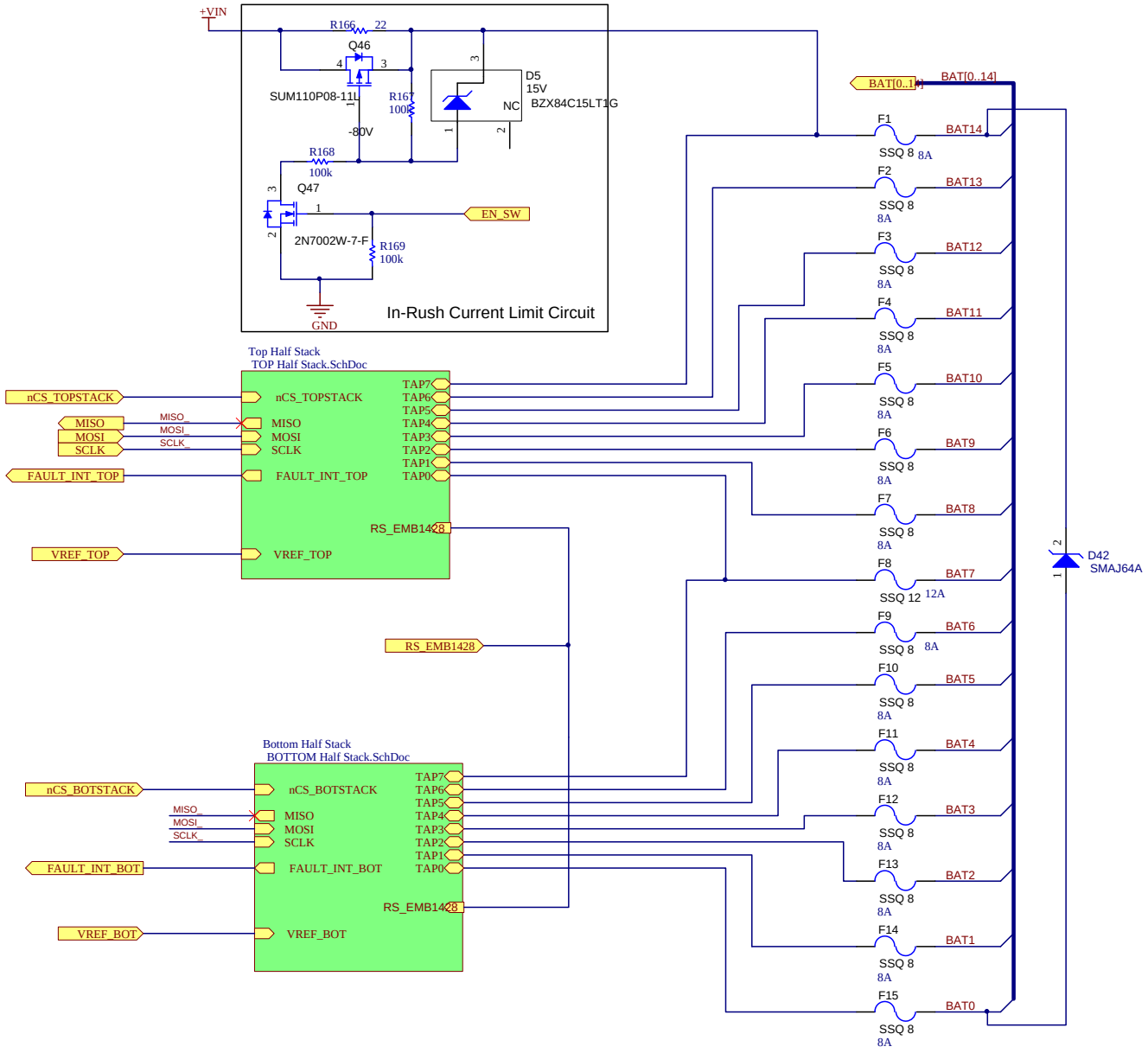


Figure 2 - In-Rush Current Limit and Battery Fuses Schematic

5 EMB1432 AFE

The EMB1432 Analog Front End (AFE) is a high voltage analog interface able to monitor a lithium battery stack. It is able to select and level shift the voltage across any of 14 stacked batteries plus other 2 low voltage auxiliary inputs, multiplexing the signals to an output pin.

5.1 Hardware Overview

The major stages of the AFE signal path are shown in Figure 3. The battery terminal voltage is first fed into a low pass RC filter (user-defined Hz). The filtered differential signal is sent to a 14 channel analog front end (AFE) where it is buffered and level translated to the AFE ground. Finally the signal is converted to a 14-bit digital word by an external ADC controlled by the microcontroller.

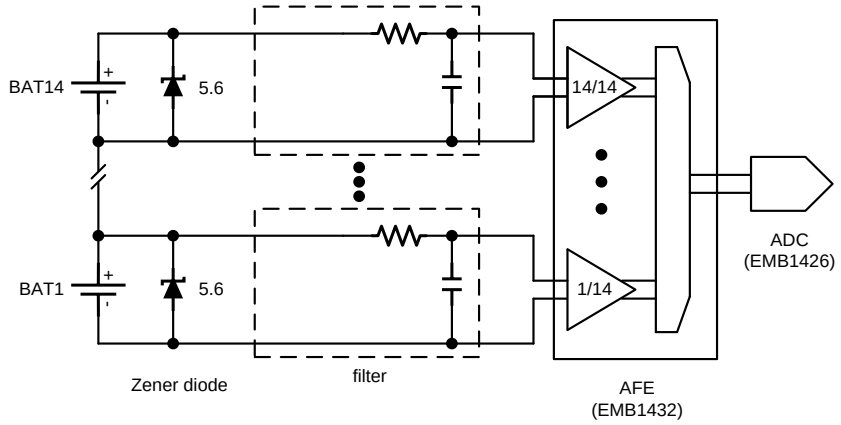


Figure 3 - Battery Cell Monitoring Simple Diagram

5.2 Interface Signals

The EMB1432 is designed with two control interfaces. One of these interfaces is the Serial Peripheral Interface (SPI). The other is a proprietary I/O based interface (MUX[0:3]). The MUX line interface provides a means to control cell selection at a faster rate than the SPI allows. The proper MUX pin configuration or SPI command to select any specific channel on the EMB1432 AFE can be found in the AFE Channel selection tables in Appendix A.

Table 3 describes the interface signals required by the EMB1432 and their general requirements.

Signal	IC	Pin number	Description	Type
CLK	EMB1432	43	SPI Clock	Microcontroller SPI peripheral or GPIO
SDI	EMB1432	41	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
SDO	EMB1432	44	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
nCS	EMB1432	42	SPI chip select	Microcontroller GPIO (output)
MUX0	EMB1432	1	MUX selection bit 0	Microcontroller GPIO (output)
MUX1	EMB1432	48	MUX selection bit 1	Microcontroller GPIO (output)

MUX2	EMB1432	47	MUX selection bit 2	Microcontroller GPIO (output)
MUX3	EMB1432	46	MUX selection bit 3	Microcontroller GPIO (output)
nSD	EMB1432	40	Shutdown (active low)	Microcontroller GPIO (output)
nRS	EMB1432	39	Reset (active low)	Microcontroller GPIO (output)

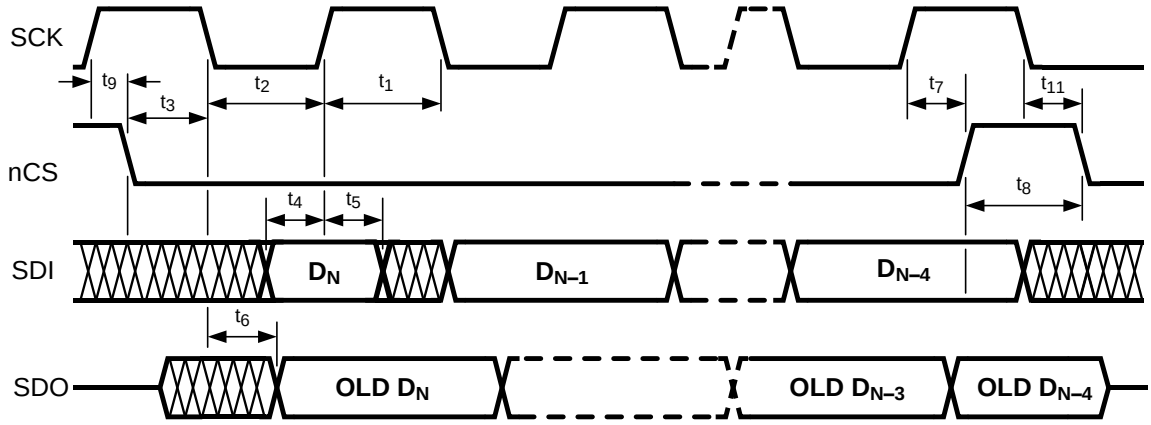
Table 3 - EMB1432 Interface Signals

To maximize the speed of multiplexing the 14 battery inputs, the EMB1432 should be set up in direct multiplexer addressing mode: multiplexing is controlled by four dedicated MUX lines (MUX0 through MUX3) instead of through the SPI interface. Please refer to the source selection table in Appendix A or the EMB1432 datasheet for each source address. When using the MUX line interface as the primary interface to the EMB1432, there is no access to AUX1 or AUX2 data. When using the SPI as the primary interface to the EMB1432, the MUX lines must be tied high.

If the primary communication method between the EMB1432 and the system microcontroller is via Serial Peripheral Interface (SPI), this serial interface can be configured in a variety of standard ways.

The proper host SPI peripheral settings for the EMB1432 are:

1. CPOL = High (CLK high when idle)
2. CPHA = 2nd Clock Edge (The second clock transition is the first data capture edge)
3. Data Bit Order = Least Significant Bit first



Where:
D_N = B3, D_{N-1} = B2, D_{N-2} = B1, D_{N-3} = B0, D_{N-4} = FB

Figure 4 - Basic AFE SPI Timing Diagram

Battery input channels may be selected in any order. However, most applications scan through all channels in order to get a “snapshot” of the battery pack cell voltages. When implementing a scan of all channels, due to the internal design of the EMB1432 it is recommended to scan from the highest channel to the lowest channel.

The fastest rate at which battery cell data can be read accurately from the EMB1432 is dependent in part on the ADC timing characteristics and the external RC filter components implemented along with the chosen ADC (EMB1426). Since the EMB1426 is a sample and hold ADC, to minimize the delay associated with selecting a new AFE channel it is recommended to make the channel selection as soon

as possible after the start of conversion. This allows the ADC filter for the next channel's data to stabilize while the previous channel's data is converted. A stable ADC input at the beginning of conversion is essential.

5.3 Open-Wire Sense

Setting to 1 the force current bit (FB=1) would sink 100uA from the negative terminal of the selected node, allowing for a fast settling of any node left floating (broken wire to the battery stack). Next, a normal mode reading of the 14 cells will be able to detect a broken wire through the finding of one below-minimum-voltage cell adjacent to one exceeding the maximum voltage.

The FB bit is only configurable when controlling EMB1432 via the SPI interface.

5.4 Power Supply Requirements

-5V can be supplied with the internal charge pump or with an external supply. To achieve the most accurate results an external precision -5V supply should be implemented. Special care should be taken to keep this supply as noise free and isolated from other switching circuits as possible.

The voltage reference and EMB1432 (VP) should be on a clean 5V power supply, shared only with the EMB1426 (VA). VIO should be the same supply used by the microcontroller and can be 2.7 – 5.5V.

5.5 EMB1432 Circuit Schematic

The schematic for the AFE circuit is provided in Appendix E, Section 14.1.2. The EMB1432 in the provided schematic is setup to use an external -5V supply and the internal charge pump is disabled. The following devices are shown in the schematic:

- EMB1432
- EMB1426 (described in Section 5.8)
- REF5025 (described in Section 5.8.2)

5.5.1 Front-End In-Rush Protection and RC Filter

The series resistors on the EMB1432 sense inputs (R1 – 15 in the schematic provided in Appendix , Section 14.1.2) are necessary to the system and serve 2 functions:

1. They protect the AFE inputs from in-rush currents during hot plug-in. This requirement limits the input series R to a minimum of 100Ω. This resistance should be kept as low as possible to minimize input voltage offset which will also be subject to drift over temperature. For this reason, they should be kept below 1kΩ.
2. Together with the capacitors on each input they provide an RC filter for high-frequency noise on the AFE inputs. The tuning of this filter cutoff is up to the customer and the noise which may be present in the end application.

5.5.2 AFE Output RC Filter

To maximize measurement accuracy the AFE output needs to settle within <1/2 of the ADC LSB. As a worst case, the AFE output could have to move the full-range that is possible in the system, for example 4.2V when the AFE output is coming up on the first cell, very high ADC sample rates are desired, when there are extreme imbalance conditions, or there is a broken cell sense connection. The RC filter must be tuned to allow the AFE output to be settled before the ADC sample is taken. From experience, the user should allow up to 11 RC time-constants. However, in typical conditions where cell to cell variation will

only be within 100mV, the AFE output will not need as much time to settle, therefore only the first cell sampled will need the extra time allowed to let the AFE output settle.

5.6 AFE Calibration

To provide maximum accuracy, the system will need to be factory calibrated for voltage offset and gain on each input channel. The system will need to be calibrated with accurate voltage references applied to the battery connection input. In the end application the user should also have an external harness attached to the battery connection header which sits in between the system and the target cells, as it presents a small series resistance to the connection from the target cell and the system AFE. There are small leakage currents due to the onboard circuits that, due to this additional external resistance in the AFE to cell connection, will present a small additional error offset. The procedure described here will allow the user to adjust the calibration offsets to return accuracy to the system.

The method to adjust the AFE offset calibration is as follows:

1. Read current cell measurement from the system.
2. Take measurement at the cell with external precision meter and calculate difference from system measurement.
3. Write AFE offset calibration value found in step 2 to a non-volatile data memory area (Flash or EEPROM).
4. Repeat this procedure for all channels.
5. Apply the stored calibration value to all cell measurements.

5.7 EMB1432 PCB Layout Guidelines

To ensure the best possible accuracy performance, it is recommended to follow some basic layout guidelines for the EMB1432 AGND and RGND signal planes, but can be on the same layer as the GND plane for the rest of the board, as long as they are separated and connected as close to BAT0 as possible. Please refer to the schematic in Appendix , Section 14.1.2 for a description of the EMB1432 AGND and RGND signals and connections.

Figure 5 shows a basic diagram of the AGND and RGND planes and the star connection at the BAT0 pin (Battery Connection header) to the GND plane. AGND and RGND should be on different layers.

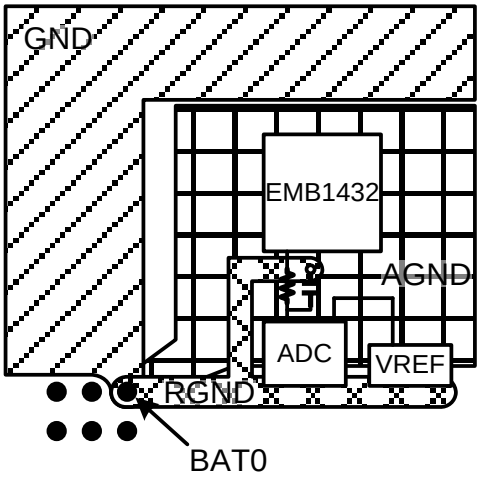


Figure 5 - AFE AGND and RGND Layout Example

5.8 EMB1426 ADC

5.8.1 Hardware Overview

A 14-bit ADC (EMB1426) is employed to achieve the highest possible voltage measurement accuracy.

5.8.2 ADC Voltage Reference

The important voltage reference electric characteristic parameters have been, from experience, the regulation performance over the temperature range and the long term drift performance. Stability is critical.

The recommended precision voltage reference is the REF5025 (from Texas Instruments). The schematic in Appendix , Section 14.1.2 includes the circuit required for the recommended voltage reference.

5.8.3 REF5025

Temperature drift: down to 3ppm/°C max
Accuracy: 0.05% (max)
Noise: 3µVPP/V

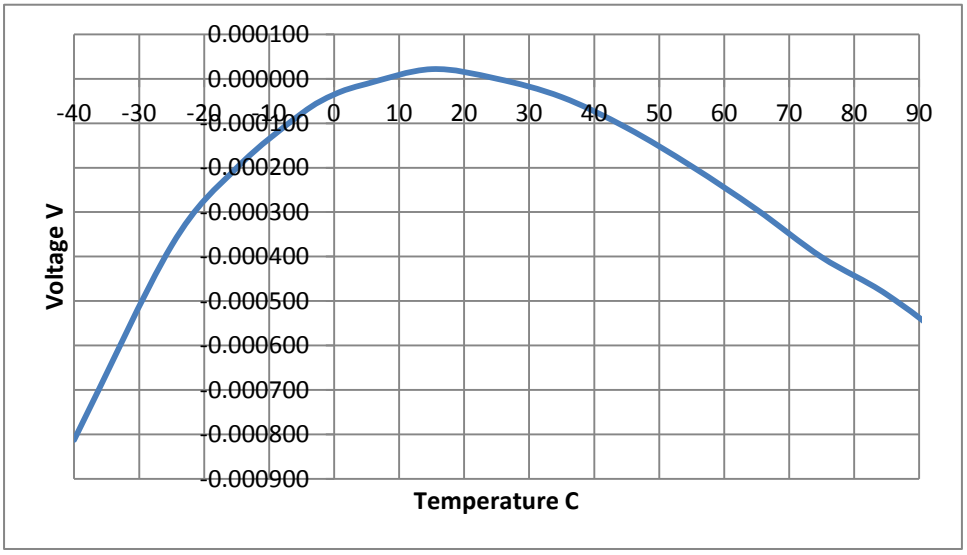


Figure 6 - Reference Output vs Temperature (Measured)

5.8.4 Interface Signals

Table 4 describes the interface signals required by the EMB1426 and their general requirements.

Signal	IC	Pin number	Description	Type
CLK	EMB1426	8	SPI Clock	Microcontroller SPI peripheral or GPIO
SDO	EMB1426	7	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
nCS	EMB1426	6	SPI chip select	Microcontroller GPIO (output)

Table 4 - ADC Interface Signals

The proper host SPI peripheral settings for the EMB1426 are:

1. CPOL = High (CLK high when idle)
2. CPHA = 2nd Clock Edge (The second clock transition is the first data capture edge)
3. Data Bit Order = Least Significant Bit first

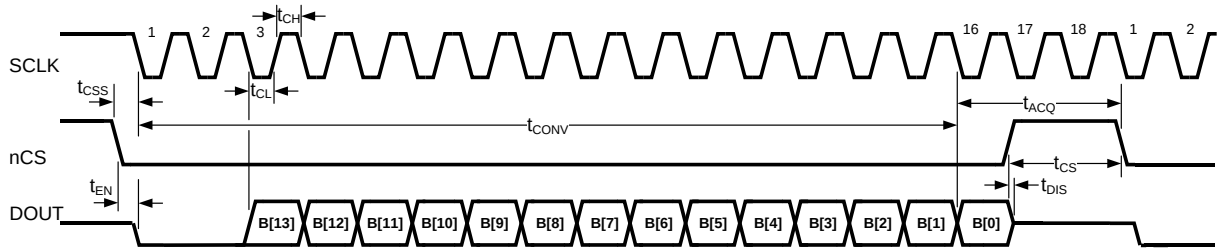


Figure 7 – Basic ADC SPI Timing Diagram

5.8.5 Power Supply Requirements

The voltage reference and EMB1426 (VA) should be on a clean 5V power supply, shared only with the EMB1432 (VP). VIO should be the same supply used by the microcontroller and can be 2.7 – 5.5V.

5.8.6 Circuit Schematic

The schematic is provided in Appendix , Section 14.1.2, and includes the ADC and voltage reference circuits.

5.8.7 PCB Layout Guidelines

The ADC is included in the PCB layout guidelines provided in Figure 5.

6 EMB1433 Battery Stack Protection

6.1 Hardware Overview

The EMB1433 is a protection chip that provides an additional layer of safety to the regular battery stack voltage acquisition chain. EMB1433 can monitor a stack of 6 to 14 cells, with a maximum of 60V at the top of the stack and can support a battery pack architecture comprised of multiple modules. The EMB1433 functions are independent from the main acquisition path, providing a layer of redundancy to the battery system. An internal flag signal is asserted any time that either one or more cells of the stack are outside a “safety” voltage window (Under-voltage , Over-voltage) or the voltage on the positive terminal of the external thermistor connected to the pin AUX exceeds a customer selectable threshold

6.2 Configuration

There are several external components that need to be configured to properly evaluate with a user’s battery pack architecture. The features that will need to be configured are listed below.

- Setpoint thresholds for:
  - HTH: over-voltage (OV)
  - LTH: under-voltage (UV)
  - AUXTH: over-temperature (OT)
- Thermistor compensation pull-down
- Number of cells
- Top module ID
- Mask delay

6.2.1 Set Point Thresholds

The EMB1433 has built-in comparators for OV, UV and auxiliary (AUX), which is typically used for over-temperature (OT). The threshold set points are configured by external resistor dividers, as outlined in the equation below:

$$Threshold = \frac{4.5V \times R1}{R1 + R2}$$

Where R1 and R2 (respectively) equate to the resistors below:
OV: R135 and R136
UV: R132 and R133
OT/AUX: R139 and R140
The external circuit where these values can be found can be seen in Appendix , Section 14.1.3. The default values for each threshold are shown in the table below.

Threshold	Description	R1	R2	Setpoint
UV	Under Voltage	8.2k	10.2k	2.00V
OV	Over Voltage	51k	10.7k	3.72V
OT/AUX	Over Temperature	17.7k	10.2k	2.85V

Table 5 - Default Threshold Values

6.2.2 Thermistor Compensation

The NTC thermistor is attached to the AUX input, and R128 provides a compensation pull-down to form the voltage divider for the temperature voltage input. R128 needs to be set as needed by the thermistor

selected by the customer to match the voltage set by the R139/R140 divider for the desired temperature. The equation for calculating pull-down (R128) value for a given thermistor is shown below.

$$Voltage\ at\ temp = \frac{4.5V \times R128}{R128 + Rt}$$

Where Rt is the thermistor resistance at the desired temperature threshold. With the default values of R139/R140 (shown in Table 5), the over-temperature threshold is 2.85V. A 103JT thermistor will be at this threshold at ~40°C, and a 104JT will be at ~98°C.

6.2.3 Number of Cells

The EMB1433 monitors 6 – 14 cells, configured by setting the CELLN[3:0] inputs with external resistors. The pull-up resistors are R115, R117, R119 and R121. The pull-down resistors are R199, R255, R256 and R257.

CELLN[3:0] need to be set as shown in Table 6.

Monitored Cells	CELLN_3	CELLN_2	CELLN_1	CELLN_0
14	1	0	0	0
13	0	1	1	1
12	0	1	1	0
11	0	1	0	1
10	0	1	0	0
9	0	0	1	1
8	0	0	1	0
7	0	0	0	1
6	0	0	0	0

Table 6 - Cell Number Configuration

6.2.4 Mask Delay

Before a fault is reported the over–under voltage and over temperature conditions are filtered to avoid a “false” or unwanted fault assertion determined by glitches and spikes on input voltage which are common in a noisy environment as the battery pack is. The amount of filtering can be programmed by mean of an external pin C_{EXT} where an external capacitor proportional to the amount of the desired “mask time” has to be connected.

C_{EXT} = 100pF provides ~3mS mask delay. This value can be multiplied to get an appropriate C_{EXT} value for the user’s application.

6.3 Interface Signals

Table 7 describes the interface signals required by the EMB1433 and their general requirements.

Signal	IC	Pin number	Description	Type
HEART	EMB1433	2	1 Wire Fault Communication Channel	Microcontroller watchdog timer peripheral or GPIO
PING_LS_IN	EMB1433	47		Microcontroller SPI peripheral

				MISO or GPIO
PING_LS_OUT	EMB1433	48		Microcontroller GPIO (output)

Table 7 - EMB1433 Interface Signals

6.3.1 HEART - 1 Wire Fault Communication Channel

The fault communication channel provides a mean for communicating the occurrence of a fault without using any extra galvanic isolation component. It consists of a 0.2mA current mode heart beat signal which is sourced from the pin DOUT_LS downwards to the next level module DIN_LS. The heart beat is a 730Hz, low duty cycle (6.7%) signal in order to reduce power consumption.

The current signal is unidirectional and propagates from the top module downwards. When there are no faults detected by the adjacent higher level module, the EMB1433 on each module will receive the 0.2mA heart beat signal on the DIN_LS pin. If EMB1433 detects a fault on its own module or sees no signal coming from the next high side module (either for a fault on any higher level module or for a broken wire), it will react ceasing to generate or retransmitting the heart beat sourcing current from its own DOUT_LS to lower modules.

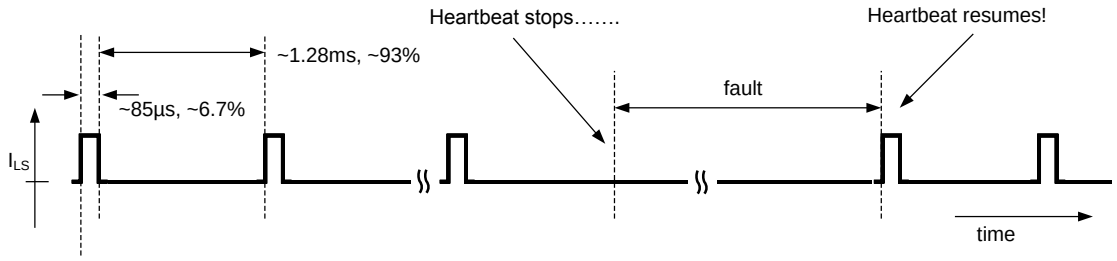


Figure 8 - HEART Signal Diagram

The dedicated HEART pin allows a direct interface of the external pack controller to the bottom module sitting at ground level. The external pack controller needs to embed an internal watch dog to capture a fault event which will be encoded on the HEART pin as an interruption of the normal beat activity.

The external pack controller watch dog timer has to be chosen taking into account the tolerance of the EMB1433 internal oscillator frequency since this is used for the heart beat signal generation plus the jitter that might be induced along the chain. Please refer to the f_{HTB} parameter in the EMB1433 datasheet. A watch dog time of 3ms (or more) is recommended.

6.3.2 PING Bus

Once a fault has been indicated by the lack of a pulse on the HEART output, the specific fault can be found by using the PING bus. Fault Information will be presented at PING_LS_OUT pin after a falling edge in detected by the EMB1433 on the PING_LS_IN input pin. The PING fault output frame output on PING_LS_OUT can be seen in Figure 9.

The ping communication consists of 10 bits sent in sequence:

- Start Bit (same as Zero Bit)
- 3 Bits for transmitting the Fault Status: OV, UV and OT
- 4 Bits for transmitting the Faulty Cell Number
- 1 Bit for parity
- Stop Bit (same as One Bit)

Nominal bit width = 21µs. The start bit or a zero bit value for OV, UV or OT will be indicated by a 25% duty cycle signal. Nominal logic 0 width = 5.3 µs. The stop bit or a one bit value for OV, UV or OT will be indicated by a 75% duty cycle signal. Nominal logic 1 width = 16 µs. Each bit takes 4 time units to transmit and is generated using an internal 375 KHz oscillator. The # of internal oscillator clock periods per time unit is 8.

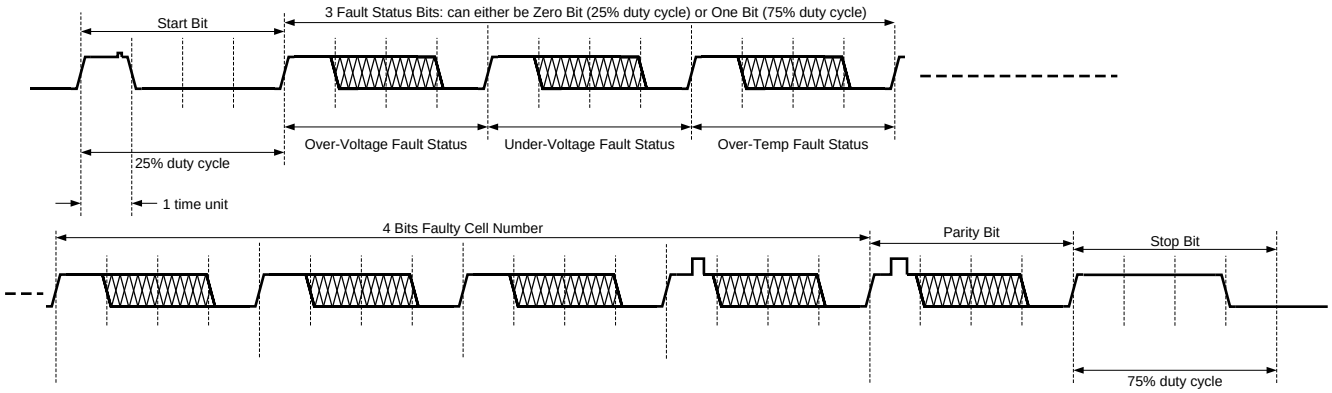


Figure 9 - PING Fault Bus Frame

Parity is calculated based on the 8 bits in the frame excluding start and stop bits. The bits are the 3 fault status bits, the 4 cell number bits and parity itself. Odd parity is used.

An OV or UV fault will also include the cell channel number at fault. In the case of an OV and UV fault being simultaneously present, the cell channel number output will be valid for the OV fault. The cell number mapping is described in Table 8.

In the case of an OT (AUX) fault, the cell channel number will be invalid.

Faulty Cell #	4-bit Cell #
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
Reserved	1110
Reserved	1111

Table 8 - Error Cell Number Mapping

6.3.3 Example #1

Let's consider the case where a module is faulty with both over-voltage (cell #5) and over-temperature. In that case the following will be transmitted:

0 101 0100 0 1

- 0 = start bit,
- 101 = over-voltage, no under-voltage, over-temperature
- 0100 = cell #5
- 0 = Parity Bit
- 1 = stop bit

6.3.4 Example #2

In case of no fault, this will be transmitted:

0 000 xxxx y 1

- xxxx: ranges from 0000 to 1101
- y: parity bit
- If fault = 000 and channel = 0000, parity will be 1 → 0 000 0000 1 1
- If fault = 000 and channel = 0001, parity will be 0 → 0 000 0001 0 1

6.4 Power Supply Requirements

-5V can be supplied with the internal charge pump or with an external supply. Use of the internal -5V supply yields adequate results, however for extremely accurate results an external precision -5V supply can be implemented. Special care should be taken to keep this supply as noise free and isolated from other switching circuits as possible.

VIO should be the same supply level used by the external pack controller and can be 2.7 – 5.5V.

6.5 Single Supply Operation

The EMB1433 is provided with an internal charge pump which supplies the right amount of negative voltage just applying a fly capacitor between CHP and CHM and a storage capacitor between CHPVM and GND and tie the negative supply pin VM to CHPVM. To enable the internal charge pump, tie CHPnSD to VP. If CHPnSD is connected to GND the internal charge pump is disabled. The following diagram shows how to connect the external capacitors to the chip for a correct usage of the charge pump. It is advisable to connect the bypass capacitors on CHPVP and the storage capacitor on CHPVM to the DGND pin. The 100 Ohm resistor across CHPVM and VM is optional (can be replaced by a short) but recommended to filter the charge pump switching noise.

6.6 Circuit Schematic

The schematic for the EMB1433 circuit is provided in Appendix , Section 14.1.3. The circuit gated by Q56 simply detects the presence of BAT14, 5VD and -5V. When 5VD and -5V are present the connection of PING_IO_LS and DOUT_LS (Q52 and Q53 respectively) are enabled. When the module is configured as the top module (TOP_DRV is connected to 3V3) Q60 connects PING_IO_HS to BAT14.

6.7 PING Header Connections

The PING_IN and PING_OUT headers shown in the EMB1433 circuit schematic in Appendix , Section 14.1.3 are to be connected in the following manner for different positions in the battery pack.

PING_OUT (bottom module)
- pin 7 (HEART) will connect to external pack controller
- pin 6 (LS_IN) will connect to external pack controller
- pin 5 (LS_OUT) will connect to external pack controller
- pin 1-4, 8 are not connected

PING_OUT (all higher modules)
- pin 7 (HEART) is not connected
- pin 6 (LS_IN) is not connected
- pin 5 (LS_OUT) is not connected
- pin 4 will connect to the adjacent lower modules PING_IN pin 1
- pin 3 will connect to the adjacent lower modules PING_IN pin 2
- pin 1, 2 are not connected

PING_IN (top module)
- pin 4 (TOP-DRV) will connect to pin 3 (3V3)
- pin 1, 2 not connected

PING_IN (all lower modules)
- pin 4 and 3 are not connected
- pin 2 will connect to the adjacent higher modules PING_OUT pin 3
- pin 1 will connect to the adjacent higher modules PING_OUT pin 4

6.8 PCB Layout Guidelines

The PCB layout guidelines for the EMB1433 are similar to the EMB1432. The AGND and RGND signal planes can be on the same layer as the GND plane for the rest of the board, as long as they are separated and connected as close to BAT0 as possible. The EMB1433 and EMB1432 AGND planes can be shared. Please refer to the schematic in Figure 10 for a description of the EMB1433 AGND and RGND signals and connections.

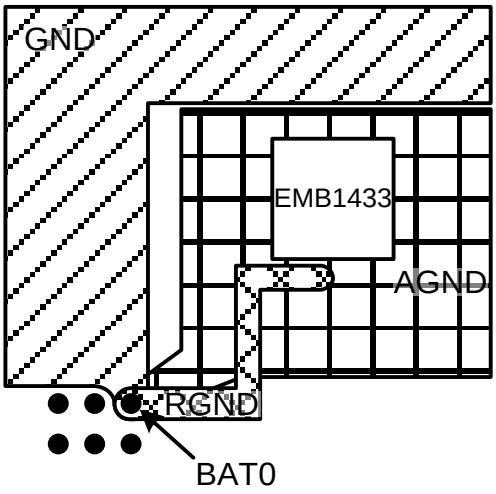


Figure 10 - EMB1433 AGND and RGND Layout Example

7 Active Cell Balancing (ACB) Architecture

7.1 Hardware overview

A switch matrix gate controller (EMB1428) and isolated DC-DC PWM controller (EMB1499) are provided for each group of cells up to 7, and each can be individually controlled. The typical BMS module manages up to 14 cells, so 2 cells can be simultaneously charged or discharged.

The chipset combination of EMB1428 and EMB1499 is controlled by a single command via SPI

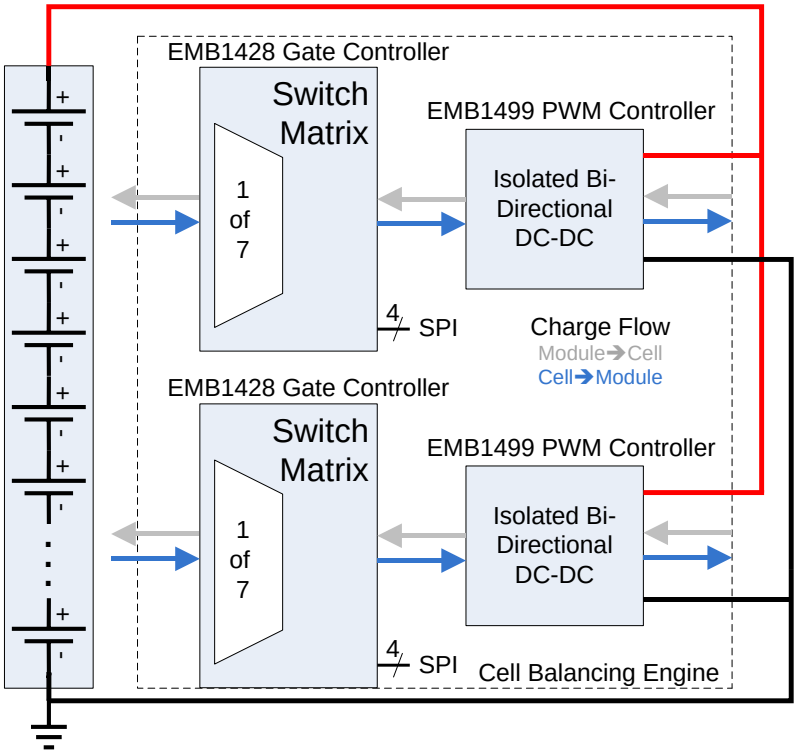


Figure 11 - Simplified Cell Balance Block Diagram

The switch matrix utilizes dual 40V FETs in series with each battery's positive and negative terminal. The source of each dual FET is connected such that there is no conduction path through the body diodes. In addition to the dual FETs in series with each battery, 4 FETs are used to route the converter to the top and bottom of the selected battery.

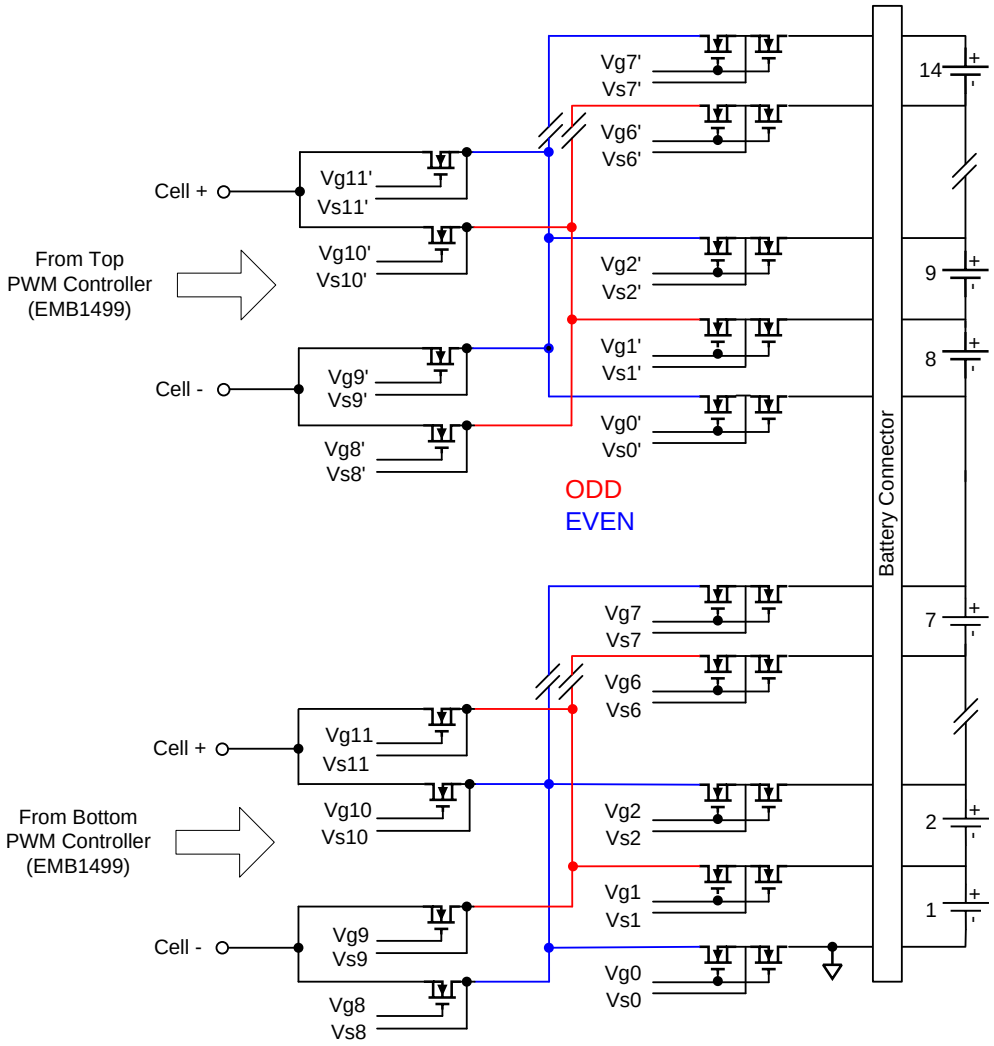


Figure 12 - Cell Balancing Simplified Diagram

The EMB1428 is a 12 channel floating NFET driver that is designed specifically for BMS systems. The primary role of the EMB1428 is to automatically make multiple switch selections based on an input of a simple cell selection command from the microcontroller. For example, selecting cell 1 (bottom half-stack cell 1) would activate bottom EMB1428 Vg1 and Vg0, and Vg11 and Vg8. Selecting cell 14 (top half-stack cell 7) would activate top EMB1428 Vg7' and Vg6', and Vg10' and Vg9'. This device also serves as a communication bridge between the microcontroller and the EMB1499 PWM controller. The EMB1428 also passes fault information from the EMB1499 to the system microcontroller.

The EMB1499 is specially designed to control the active clamp forward topology, with the ability to control the charge current in both directions (sink or source).

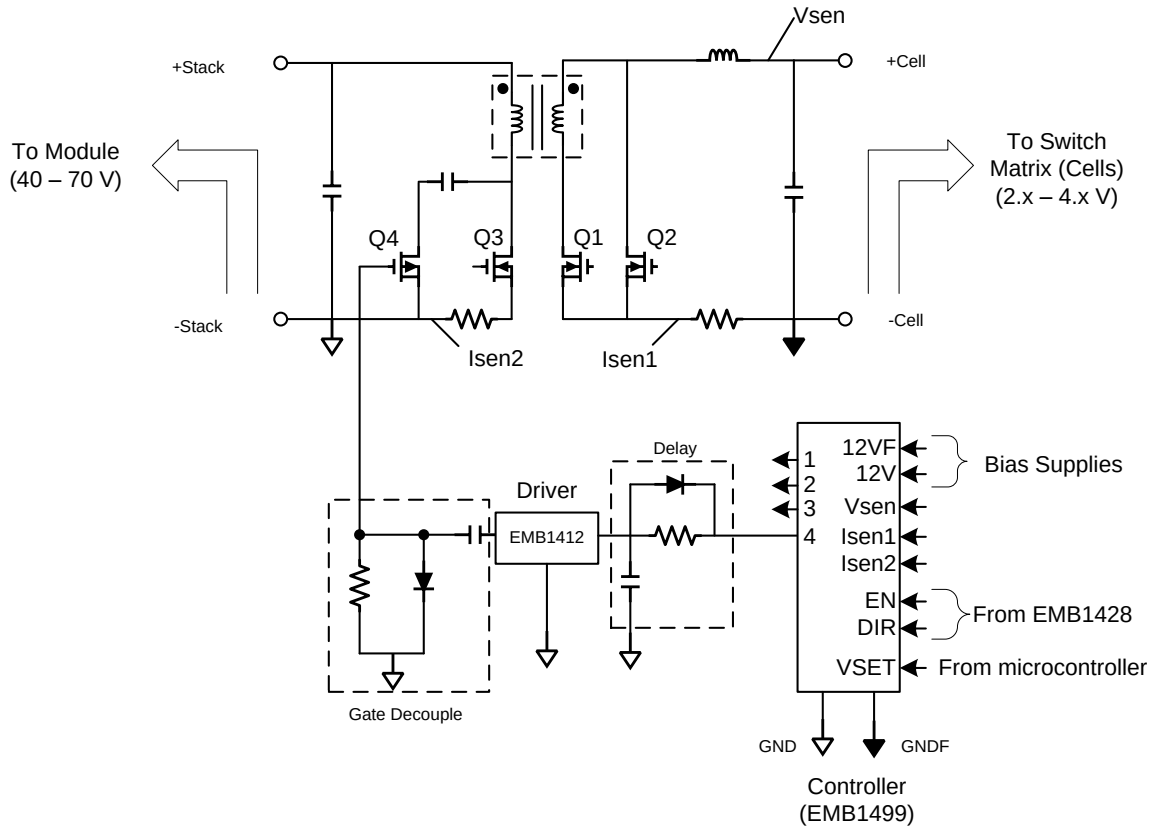


Figure 13 - PWM Controller Simplified Diagram

7.2 Interface Signals

Table 9 describes the interface signals required by the EMB1428 (2x) and EMB1499 and their general requirements.

Signal	IC	Pin number	Description	Type
SCL_C	EMB1428	27	SPI Clock	Microcontroller SPI peripheral or GPIO
SDI	EMB1428	28	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
SDO	EMB1428	29	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
CS (NOTE 1)	EMB1428	30	SPI chip select	Microcontroller GPIO (output)
FAULT_INT (NOTE 1)	EMB1428	31	Fault interrupt source	Microcontroller GPIO (interrupt input)
RESET (NOTE 1)	EMB1428	35	Reset (active high)	Microcontroller GPIO (output)
VSET	EMB1499	6	Current set point	Microcontroller DAC or PWM (with low-pass filter) output
Inrush limit	Q46		Enables FET bypass of	Microcontroller GPIO (output)

bypass	(NOTE 2)		in-rush limit circuit	

NOTE 1 - 2 of these interface signals are required for both bottom and top half-stacks if design includes more than 7 cells.
NOTE 2 – Q46 is described in Section 4.2.

Table 9 - EMB1428 and EMB1499 Interface Signals

The primary communication method between the EMB1428 and the system microcontroller is via Serial Peripheral Interface (SPI). This serial interface can be configured in a variety of standard ways.

The proper host SPI peripheral settings for the EMB1428 are:

1. CPOL = Low (CLK low when idle)
2. CPHA = 1st Clock Edge (The first clock transition is the first data capture edge)
3. Data Bit Order = Most Significant Bit first

The serial interface operates on 8-bit transactions. The microcontroller must send a 4-bit command on SDI followed by 4 zeros. The EMB1428 will provide FAULT[3:0] on SDO, followed by the 4-bit command that was previously received. The EMB1428 will drive SDO on the falling edge of SCL_C and sample SDI on the rising edge of SCL_C. If nCS goes high at any point before the 8th rising edge of SCL_C, the transaction will be considered aborted and the data that was received on SDI will be discarded. No command change will occur from such a transaction. However, if FAULT_INT was cleared by the transaction it will remain cleared and the fault data will no longer be accessible. AC timing specs can be found in the device datasheet.

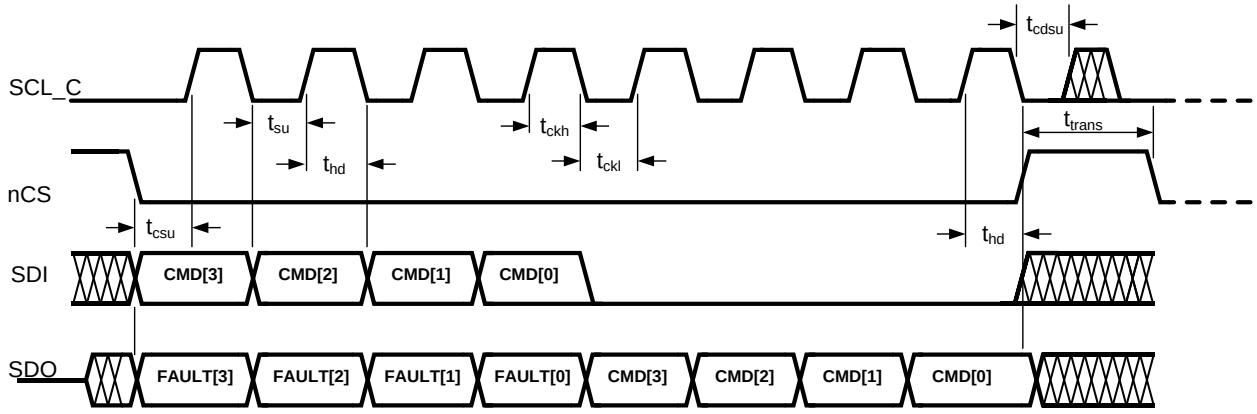


Figure 14 - EMB1428 SPI Timing Diagram

The EMB1428 SPI drivers are optimized for a maximum interface speed of 1MHz. Since SPI can be configured to operate at speeds higher than this rate, care should be exercised to configure SPI properly to limit the interface rate. Failure to properly limit the interface speed may result in bit errors during communication.

The EMB1428 controls the EMB1499 with a digital I/O interface. All communication between the EMB1428 and the EMB1499 are originated from the EMB1428, and the EMB1428 initiates this communication only in response to SPI commands sent to it from the system microcontroller.

7.2.1 EMB1428 Commands Codes

The channel selection and charge transfer direction are combined into a single SPI command byte sent from the microcontroller to the EMB1428 (which then controls the EMB1499's DIR and EN pins after having selected the desired channel). The command to the EMB1428 is a single byte of data. Bits 7 to 4 of this data byte control the channel selection and current charge transfer direction, whereas bits 3 to 0 of this data byte should be zero. Bit 7 controls the charge transfer direction (0 for charge, 1 for discharge), and bits 4 to 6 sets the channel selection (001 = channel 1, 010 = channel 2, etc. to 111 = channel 7) or disconnects all channels (0000 = STOP or open all channels). The commands can be seen in Appendix B.

It is very important to note, the EMB1499 has a built-in safety timer which expires in eight seconds. Once a command to start a charge or discharge current transfer has been sent to the EMB1428, and the EN and DIR signals to the EMB1499 have been set, the transfer may be cancelled in one of two ways:

1. STOP command
2. EMB1499 time-out

Sending the STOP command stops the EMB1499 and disconnects the EMB1428 from all cell channels. A STOP command must be sent to the EMB1428 before eight seconds have elapsed.

For current transfers longer than 8 seconds, the user should send a STOP command followed by a START command (after t_{trans} – see EMB1428 datasheet), in a period of less than 8 seconds.

Alternately, the EMB1499 may be allowed to time-out on its own using its built-in eight second timer. However, if the EMB1499 is allowed to time-out, a fault will be generated by the EMB1499, causing the EMB1428 FAULT_INT line to be asserted and the device will need to be reset (by toggling the EMB1428 RESET signal) before a new command can be sent for a subsequent cell selection and charge or discharge.

When the EMB1499 has ramped the output current down to zero, the DONE output will be set, telling the EMB1428 that a new command can be accepted.

7.2.2 EMB1499 Fault Codes

Fault Codes (or lack of any faults) are reported by the EMB1499 to the EMB1428 companion IC via the EMB1499's FAULT[2:0] pins, which connect to the FAULT[2:0] pins on the EMB1428. The codes which appear on the EMB1428's FAULT[2:0] pins are translated into codes reported via SPI back to the microcontroller.

7.2.3 FAULT generation and Reporting

The response from the EMB1428 after having communicated with the EMB1499 via the I/O pins is also a single byte of information. This single byte contains the FAULT code (or lack of fault, as the case may be) associated with the previous command concatenated with the channel/direction command that was just sent to the EMB1428 to initiate the communication. The response byte contains the FAULT code in bits 4 to 7, and the channel selection/direction command in bits 0 to 3. The possible FAULT codes can be seen in Appendix B.

For example, if the application selects channel 5 for charge, the microcontroller would send 05h to the EMB1428. If there was no fault in carrying out the command, the EMB1428 would respond with, A5h. A

request to discharge channel 3 would be sent as 0Bh, and if there was no fault in carrying out the command the response to this command would be ABh.

7.2.4 Sleep Mode

The EMB1428 will enter sleep mode when any of the following methods are applied:

- A STOP command is received
- The RESET pin is held high
- The RESET pin is toggled high then low

There are several conditions which, if present, the EMB1428 will not allow any switched to be closed. These include:

- Insufficient VDDCP to VSTACK voltage
- Insufficient supply voltage on an individual floating driver rail
- Loss of the VDD_5V or VDD_12V supply
- The following illegal combinations of gate driver output are detected:
  - More than 2 bits of Vg[7:0] are set
  - Two non-consecutive bits of Vg[7:0] are set
  - (Vg11 | Vg8) & (Vg10 | Vg9)

7.2.5 Example Flow

The following flow charts describe the basic relationship of commands and faults in the EMB1428 and EMB1499.

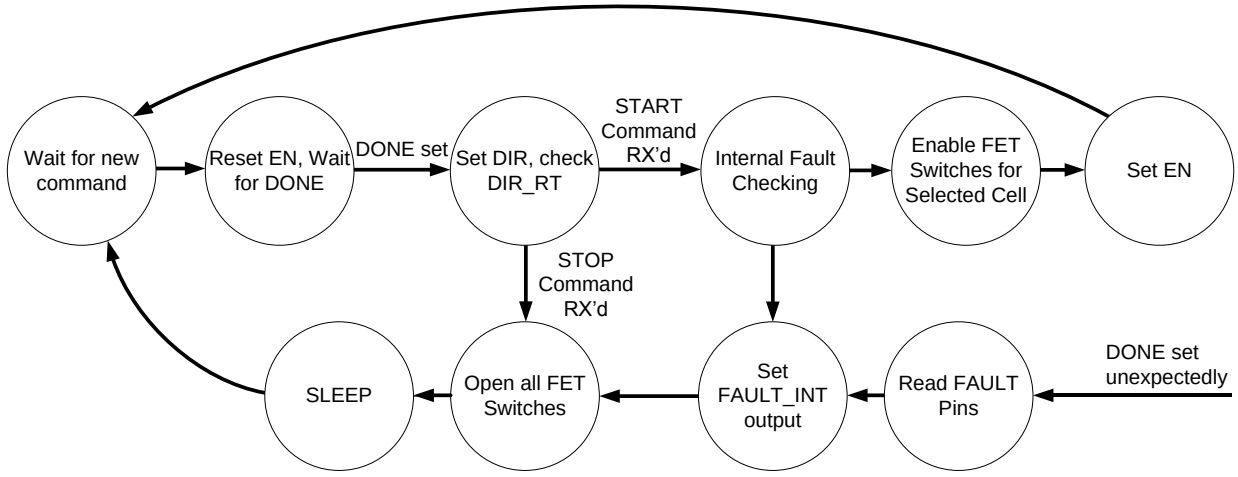


Figure 15 - EMB1428 Flowchart

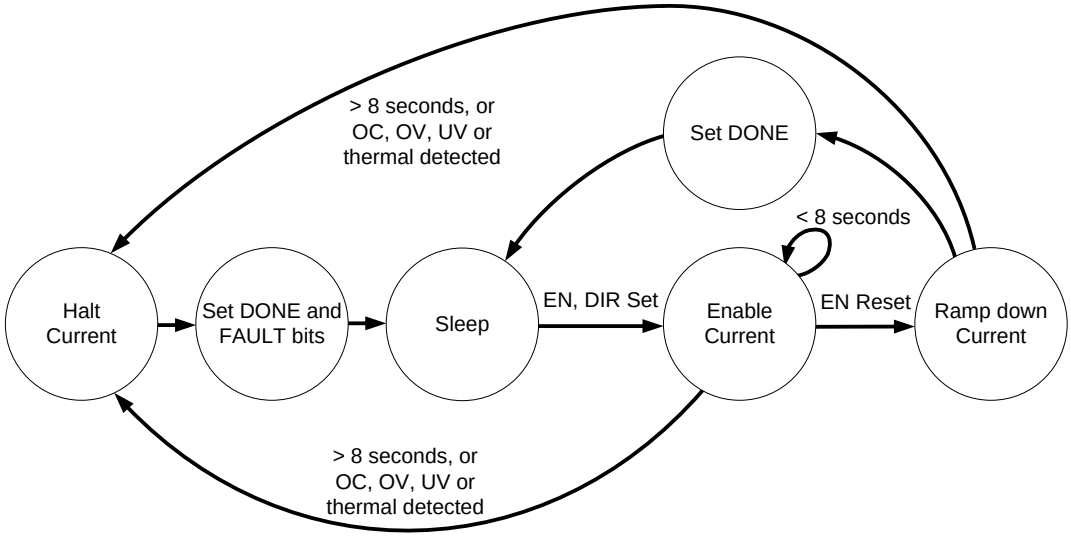


Figure 16 - EMB1499 Flowchart

7.3 Current Set Point

One input signal not provided to the EMB1499 by the EMB1428 is the current set point (VSET). This set point, in conjunction with the current sense resistor, will control the amount of current used in the transfer. The current is set by a combination of the setting of the feedback voltage (via VSET), and selection of the secondary current sense resistor as governed by the equation below.

$$balance\ current = feedback\ voltage\ \div secondary\ sense\ resistor$$

The primary current sense resistors are R179 and R197 in the schematics for the EMB1499 circuit provided in Appendix , Sections 14.1.6 and 14.1.8. The secondary current sense resistors are R174 and R192 in the schematics for the EMB1499 circuit provided in Appendix , Sections 14.1.6 and 14.1.8.

7.3.1 Setting the Balancing Current (VSET and Secondary Sense Resistor)

The cell balancing current is equal to the steady state value of the main inductor current. Two external parameters determine the balancing current ($I_{balancing}$): the voltage at VSET pin and the secondary side sense resistance (R_{SENSE2}). The voltage at the VSET pin controls the reference voltage at the internal error amplifier, and therefore the voltage at the V_{SENSE_HS} pin.

The equation for selecting the secondary side sense resistance is:

$$R_{SENSE2} = \frac{V_{SENSE\_HS}}{I_{balancing}}$$

In the equation, V_{SENSE_HS} is a value dictated by the VSET voltage, in accordance with the following equation:

$$V_{SENSE\_HS} = \frac{VSET}{40}$$

Supported values for VSET range from 1V to 2.2V. However, the EMB1499 is factory trimmed at VSET = 2V. Therefore, it is recommended to use VSET = 2V for highest balancing current accuracy. See the Electrical Characteristic table for specified tolerances on V_{SENSE_HS} when for VSET =2V and 1.2V.

It should be noted, however, that in order to guarantee loop stability, the sense resistor value should also be chosen in conjunction with the output inductor. See Section 7.11 for detailed description of the output inductor selection.

For example, if a 5A balancing current is desired, and VSET voltage is set to 2V, a 10mΩ sense resistor should be chosen.

$$V_{SENSE\_HS} = \frac{2V}{40} = 50mV$$

$$\therefore\ R_{SENSE2} = \frac{50mV}{5A} = 10\text{m}\Omega$$

Due to switching noise present at the secondary side current sense resistor, it is possible that current values are slightly different for different directions of balancing, even if VSET is the same. In such a case, it is recommended that a calibration be conducted at the system level so that a slightly different VSET is programmed when changing the direction of balancing. A procedure for this is described in Section 7.14.

7.3.2 Primary Sense Resistor Selection

The primary sense resistor should be chosen in conjunction with the secondary sense resistor so that the ratio between the two resistors is approximately equal to the transformer turns ratio. For example if the secondary sense resistor is 10mΩ, and the transformer turns ratio is 3.5:1 (14 cell application), the primary sense resistor should be chosen to be approximately 35mΩ.

7.4 EMB1428 Switch Matrix FET Selection

For optimal balance transfer efficiency, the switch matrix FETs should be selected to provide the lowest possible conduction loss. For the purpose of FET selection, a good figure of merit to use is on resistance (R_{dson}). The total power loss due to this parameter can be calculated using the equation below.

Conduction power loss can be calculated by multiplying the square of the charge current by the static drain to source on resistance ($r_{DS(on)}$) parameter.

$$P_{LOSS} = {I_{RMS}}^2 \times R_{dson}$$

In addition to the total conduction loss, the EMB1428 switch matrix FETs have the following additional requirements:

- N-channel
- All FETS must have absolute max rating for V_{GS} at least 20V
- A breakdown voltage > than half of the stack voltage (from cell 0- to top of half-stack cell+) + 10V
- Gate resistance (R_g) ≤ ~10Ω, to ensure adequate turn-off strength during transient events

7.5 EMB1499 Switch FET Selection

The parameters described in this section can be used to estimate the total conduction and gate charge losses for each FET, which should be minimized:

$$P_{LOSS} = {I_{RMS}}^2 \times R_{dson} + Q_G \times F_{SW}$$

Where F_{SW} is the switching frequency of the EMB1499 (typically 250kHz), and I_{DS} is the RMS drain current in each FET during steady state. The following equations can be used to provide a first order estimation of the RMS drain current in each FET:

Primary switching N-channel FET (Q28 and Q33 in the schematics for the EMB1499 circuit provided in Appendix , Sections 14.1.6 and 14.1.8):

$$I_{RMS} \approx \frac{I_{balancing}}{2 \times NumCells}$$

Secondary switching N-channel FET (Q27 and Q29 in the schematics for the bottom EMB1499 circuit provided in Appendix , Section 14.1.6 and Q31 and Q34 in the schematics for the top EMB1499 circuit provided in Appendix E, Section 14.1.8):

$$I_{RMS} \approx \frac{I_{balancing}}{\sqrt{2}}$$

Active Clamp P-channel FET (Q26 and Q32 in the schematics for the EMB1499 circuit provided in Appendix E, Sections 14.1.6 and 14.1.8):

$$I_{RMS} \approx 25mS \times V_{CELL\_MAX}$$

Where V_{CELL_MAX} is the maximum operating voltage of any cell in the stack

The FETs package thermal characteristics should also be sufficient to handle the sum of the conduction and switching power losses.

In addition to power dissipation concerns, and assuming that the transformer turns ratio has been chosen correctly (see the section on transformer selection), the EMB1499 FETs have the following additional requirements:

- All FETS must have absolute max rating for V_{GS} at least 20V.
- Primary FETS (switching and active clamp) must have drain-source voltage rating at least 2.5 times the maximum operating stack voltage.
- Secondary FETs must have drain-source voltage rating at least 30V, gate resistance no more than 3Ω, and be avalanche robust (e.g. have an Avalanche Energy rating (E_{AR}) specified in the datasheet).

7.6 Active Clamp Driver Circuit

The active clamp driver circuit can be found in the schematics for the EMB1499 circuit provided in Appendix , Sections 14.1.6 and 14.1.8. The driver path consists of a delay circuit (around U24 and U28), the driver (U30 and U12), and a passive level shifting circuit (C129, C139, D17, D20, R172 and R190).

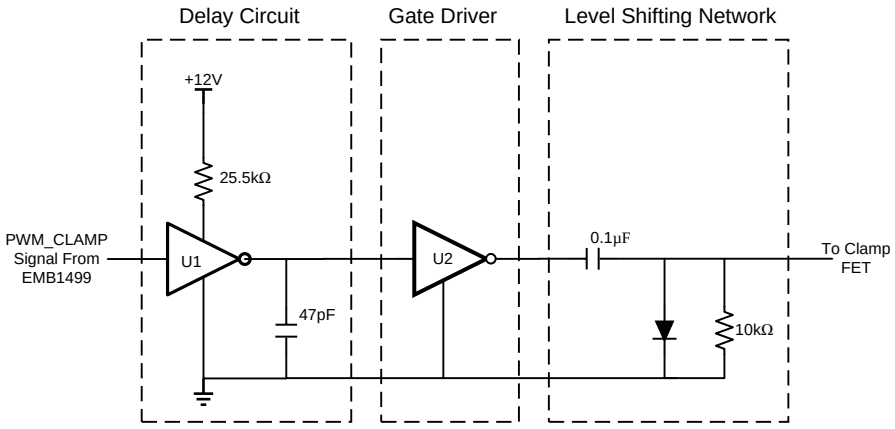


Figure 17 - Active Clamp Circuit

7.6.1 Delay Circuit

The delay network should provide approximately 300 to 400ns delay to the turn-on transition of the clamp FET, and minimal delay to the turn-off transition. The recommended inverter for this application is the BU4S584G2 Schmitt Trigger Inverter from Rohm Semiconductor.

An N-channel MOSFET can also be used. An N-channel FET should be selected with a drain-source capacitance significantly less than the external 47pF capacitor (C225 and C226) to properly set the desired delay. It is also recommended that the FET must be able to withstand gate-source and drain-source voltages higher than 20V. Using an inverter has the advantage of consuming no standing current regardless of the state of the input, whereas using the FET creates standing current through the 25kOhm resistor when the PWM_CLAMP signal is high (this is the default state of the PWM_CLAMP signal during shutdown). For this reason U24 was selected because it could withstand 12V.

7.6.2 Driver

The recommended driver for this application is the EMB1412 (U30 for the bottom converter and U12 for the top converter). It is important to configure the driver in an inverting configuration.

7.6.3 Passive Level Shifting Circuit

The passive level shifting network (C129, D17 and R172 for the bottom converter C139, D20, and R190 for the top converter) is required in order to provide a negative gate voltage for the clamp P-channel FET. It consists of a 0.1µF AC coupling capacitor, a clamping diode, and a 10kΩ resistor to provide a DC path to ground for the gate of the clamp PFET.

7.6.4 Clamp FET

The clamp FET should have the following spec:

- P-channel
- Absolute maximum V_{gs} ≥ 20V
- Drain-source breakdown voltage ≥ 150V

7.7 Input Capacitor Selection

The input capacitors are C122, C123 and C124 in the schematics for the bottom EMB1499 circuit provided in Appendix , Section 14.1.6 and C132, C133 and C134 in the schematics for the top EMB1499 circuit provided in Appendix E, Section 14.1.8.

Ceramic capacitors are required for proper operation, due to their low ESR (equivalent series resistance). The voltage rating of the capacitor should exceed the maximum stack voltage in an application with proper de-rating. For example, in a 14 cell Li-ion application, the maximum stack voltage would be approximately 60V. Therefore, a 100V rated capacitor would be recommended.

It is recommended to use at least 6.6µF of capacitance. Optimum performance will be achieved by using multiple smaller value capacitors in parallel, to minimize series resistance and inductance.

For proper performance, X5R or X7R ceramics are recommended.

7.8 Output Capacitor Selection

The output capacitors are C126 and C127 in the schematics for the bottom EMB1499 circuit provided in Appendix , Section 14.1.6 and C136 and C137 in the schematics for the top EMB1499 circuit provided in Appendix E, Section 14.1.8.

As with the input capacitors, ceramic capacitors are required (X5R or X7R recommended). Since the maximum operating cell voltage of a Li-ion cell is 4.2V, a voltage rating of 6.3V or higher is recommended.

It is required to use at least 10µF of capacitance. Optimum performance will be achieved by using multiple smaller value capacitors in parallel, to minimize series resistance and inductance.

7.9 Clamp Capacitor Selection

The clamp capacitors are C125 and C135 in the schematics for the EMB1499 circuit provided in Appendix E, Sections 14.1.6 and 14.1.8.

As with the input and output capacitors, a ceramic capacitor is required for the clamp capacitor. Assuming that the transformer turns ratio has been chosen correctly (see the section on transformer selection), the voltage rating of the capacitor should be at least 2.5 times the maximum operating voltage of the battery stack.

For example, in a 14 cell solution with a maximum operating cell voltage of 4.2V, the maximum operating voltage of the stack is 58.8V. Therefore, the voltage rating of the capacitor should be at least 2.5 * 58.8V = 147V.

So for a 14 cell solution, a voltage rating of 200V (the next closest commonly found voltage rating) is recommended.

The recommended capacitance value for the clamp capacitor is 0.1µF.

7.10 EMB1499 Transformer Selection

In selecting the proper transformer (T2 and T3 in the schematics for the EMB1499 circuit provided in Appendix E, Sections 14.1.6 and 14.1.8) for use with the EMB1499, several major factors should be

considered, including turns ration, primary magnetizing inductance, leakage inductance and DC winding resistance.

7.10.1 Turns Ratio

The EMB1499 was designed to work with a transformer turns ratio of 3.5:1 when operating within a stack of 14 cells. In order to maintain proper peak currents and voltage stresses on the drains of the power FETs, it is recommended that this relationship between turns ratio and number of cells be maintained. In other words, follow the following equation when choosing a turns ratio for the transformer:

$$n = 0.25 * NumCells$$

7.10.2 Primary Magnetizing Inductance

As can be seen in the schematic for the EMB1499 circuit is provided in Appendix , Sections 14.1.6 and 14.1.8, the forward transformer for the EMB1499 has a minimum primary side inductance of 190µH. To guarantee proper operation, it is recommended to use this as the minimum inductance specification for a 14 cell solution. It is reasonable to scale this inductance with the number of cells in the stack. For example, for a 7 cell stack, a minimum primary inductance of 95uH can be used.

7.10.3 Leakage Inductance

The leakage inductance is directly related to the coupling coefficient of the transformer. For proper operation, it is recommended that the leakage inductance of the transformer be less than or equal to 1% of the magnetizing inductance.

7.10.4 DC Winding Resistance

On the transformer used in a typical 5A design, the primary side DC resistance is typically 57mΩ, and the secondary side resistance is typically 12mΩ. In order to ensure reasonable efficiency, and to ensure properly gauged wires are used in the transformer, it is recommended to follow this specification for 5A balancing current. It is reasonable to scale these resistance specifications for constant DC power dissipation with different balancing currents.

7.11 EMB1499 Inductor Selection

In selecting the proper inductor (L5 and L7 in the schematics for the EMB1499 circuit provided in Appendix , Sections 14.1.6 and 14.1.8) for use with the EMB1499, several major factors should be considered, including output current ripple, loop stability, core saturation current and DC resistance.

7.11.1 Output Current Ripple

The value of the inductor, along with the converter input/output voltages, determines the AC ripple of the inductor current. A good rule of thumb is to choose the inductance value so that the peak-to-peak ripple falls somewhere between 20% and 40% of the steady state balancing current during typical operation. If the transformer turns ratio is selected properly (see section 6.8 above), and assuming a 250kHz switching frequency, then the equation relating inductance to current ripple for the EMB1499 can be reduced to:

$$L = 3x10^{-6} * V_{CELL} * \Delta i_L$$

Where V_{CELL} is the typical cell voltage in the given application, and Δi_L is the peak to peak current ripple value, calculated as:

$$0.2I_L \leq \Delta i_L \leq 0.4I_L$$

For example, a 6.8µH inductor is used in the active chipset reference design (5A balancing current). With this inductance value and a typical cell voltage of 3.5V, the peak-to-peak ripple can be calculated to be:

$$\Delta i_L = \frac{3x10^{-6} * 3.5V}{6.8\mu H} = 1.54A$$

which is about 31% of the 5A balancing current.

7.11.2 Loop Stability

The EMB1499 utilizes peak current mode control, which means that the inductor current is sampled in real time and used for loop control. In this type of control method, the slope of the sensed inductor current ripple is an important parameter. This sensed slope is inversely proportional to the inductor value, and directly proportional to the gain of the current sense path. In other words:

$$\frac{dI_{SENSE}}{dt} \propto \frac{R_{SENSE2}A_I}{L}$$

Where I_{sense} is the sensed inductor current, R_{sense2} is the secondary side sense resistor value, and A_i is the gain of the internal current sense amplifier.

In order to guarantee stability of the internal current sense loop, it is recommended that the slope of the sensed inductor current remain somewhat constant if external component values are changed. From the above equation, this means that if the value of the secondary sense resistor is increased (possibly to achieve lower balancing current), then the value of the output inductor should be increased with approximately the same scale.

7.11.3 Core Saturation Current

When selecting an inductor, be sure to choose an inductor that can support the peak output current without saturating. Inductor saturation will cause a sudden reduction in the inductance value, and cause the converter to operate incorrectly.

7.11.4 DC Resistance

This parameter becomes especially important at higher balancing currents (such as 5A). It is recommended to choose an inductor with minimal DC resistance in order to minimize conduction losses and maximize efficiency.

As with the input and output capacitors, a ceramic capacitor is required for the clamp capacitor. The recommended capacitance is 0.1 µF with a voltage rating of at least 200V.

7.12 EMB1428 and EMB1499 Power Supply Requirements

The following power supplies are common to both the EMB1428 and EMB1499:

- 12V

- Supplies EMB1428 VDD_12V and EMB1499 VINA and VINP
- Consumes ~22mA during use and TBD during sleep mode

7.12.1 EMB1428

- VIO
  - 2.5 – 5.5V
- 5V
  - VDD_5V
  - Digital logic supply, can be shared with +5V supply used for other ICs (EMB1432, EMB1433)
- Top of stack
  - VDD_CP
  - Internal charge pump supply that provides the gate drive.
  - This supply must always be present before VDD_12V, VDD_5V and VDD_IO.

7.12.2 EMB1499

- Floating 12V
  - Separate supply required for each EMB1499
  - Supplies EMB1499 VINF and PVINF
  - Consumes ~36mA during use and TBD during sleep mode.

7.13 Circuit Schematic

The schematic for the EMB1428 circuit is provided in Appendix , Sections 14.1.5 and 14.1.7. The schematic for the EMB1499 circuit is provided in Appendix , Sections 14.1.6 and 14.1.8.

7.14 Current Calibration

To provide maximum accuracy, the system will need to be factory calibrated for current offset and gain on each converter. The system will need to be calibrated with an accurate ammeter measuring each converter output.

Although the current set point could be implemented with a fixed external voltage reference, typically a microcontroller provides this reference to the EMB1499 using a DAC or a PWM signal and an external RC filter. Configuration of the DAC output, or calculation of the PWM duty cycle required to reach a specific voltage level will depend on the microcontroller internal features and IO voltage. Please consult the microcontroller datasheet for specific configuration information.

The procedure described here will allow the user to adjust the calibration offsets to return accuracy to the system.

The method to adjust the current offset calibration is as follows:

1. Start a cell charge transfer.
2. Take measurement at the cell with external ammeter and calculate difference from system current setpoint (EMB1499 Vset).
3. Write current offset calibration value by found in step 2 to a non-volatile data memory area (Flash or EEPROM).
4. Repeat this procedure for all converters.
5. Repeat this procedure for a cell discharge transfer.
6. Apply the stored calibration value to the DAC or PWM (EMB1499 driving Vset).

7.15 PCB Layout Guidelines

7.15.1 EMB1428

This section describes the design criteria that need to be considered for the EMB1428 PCB layout. The EMB1428 schematics are can be referenced in Appendix , Sections 14.1.5 and 14.1.7.

The charge pump components are C_Vstack1, CEXT1, CEXT2 and D7 for bottom EMB1428 and C_Vstack2, CEXT3, CEXT4 and D2 for the top EM1428.

The decoupling caps (C17-19 and C209 for bottom EMB1428 and C118-120 and C210 for top EMB1428) are as close as possible to the EMB1428 devices.

The layout should keep every gate trace as close as possible to its companion source trace.

7.15.2 EMB1499

The EMB1499 is in essence a bi-directional active clamp Forward switching converter, thus the designer simply need to follow the basic guidelines for layout of a forward converter. This means keeping the traces short and the loops small for discontinuous currents. There are also a couple of unique considerations for this specific application/topology. The schematics for the EMB1499 circuits provided in Appendix , Sections 14.1.6 and 14.1.8

The designer needs to sure the decoupling cap from EMB1499 PGNDF to GND is situated close to the EMB1499 and that the PCB trace loop is as small as possible. This capacitor is critical to providing an AC return path and should be kept as clean as possible. This capacitor is C215 for bottom EMB1499 and C216 for the top EMB1499.

The sense lines for the current sense resistor (R174 for bottom EMB1499 and R192 for top EMB1499) should also be setup as a kelvin connection. Traces to both sides of the resistor need to be close to the EMB1499 to minimize offset errors and reduce the risk of noise being coupled in.

The following basic criteria should also be met:

- All decoupling capacitors should be placed as close as possible to the EMB1499.
- Run the gate traces in parallel with their associated ground planes for as much of the total runs as possible.
- Keep current sensing traces away from high dv/dt nodes such as the drain of power FETs.
- Place enough copper underneath power FETs to help cool down the same.
- The EMB1499 should ideally be situated within a couple inches of the power FETs so that the gates are tightly controlled.
- Place ten or so 8-mil vias on the PCB pad beneath the EMB1499 and connect them to the corresponding ground plane(s) on all layers to cool down the chip.

8 System Integration Considerations

This section describes features or issues which will need to be considered when the previously mentioned subsystems and circuits are integrated in a customer's design.

8.1 Cell Connection

The EMB1499 internal protection circuits and the EMB1432 cell measurement can be affected by the cell connection method.

The EMB1499 has built-in protection for overvoltage (OVP) or undervoltage (UVP) while transferring current to/from a battery cell. This protects the BMS from damage due to an open cell connection. The cell voltage is sensed on the CELLPLUS pin of the EMB1499. The spec for OVP/UVP is provided in the electric specifications section of the EMB1499 datasheet.

There are some battery cell connection design considerations which will influence PCB layout, connector selection, and wire harness construction.

The equation below describes the voltage level on CELLPLUS while balance current is flowing. What is referred to as "Common Path" includes every circuit connection from the CELLPLUS pin to the external connector. This includes:

- Harness connector contact resistance
- Switch matrix FET $r_{DS(on)}$ (x4)
- PCB trace resistance

$$CELLPLUS\ V = Vcell + (Balance\ Current \times (BMS\ common\ path\ R + Harness\ R))$$

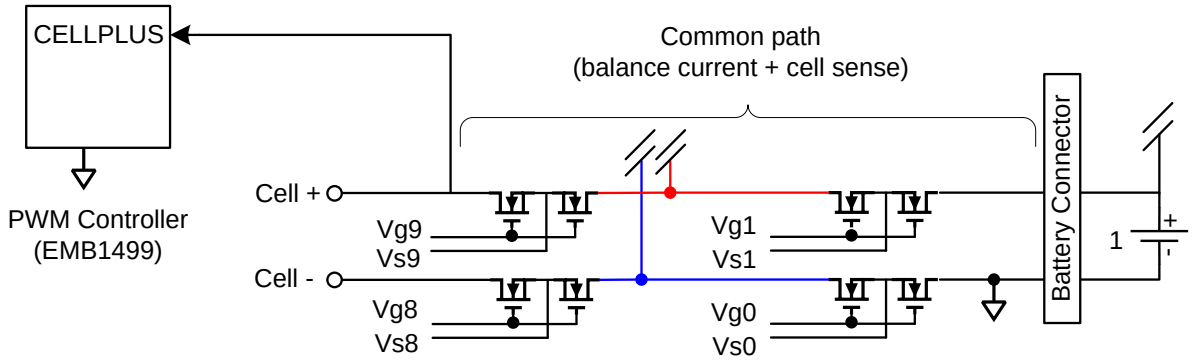


Figure 18 - CELLPLUS Common Path

As an example, on the EM1401 BMS Evaluation Board, the resistance of the common path shown in Figure 18 is ~75mΩ. At 5A charge, with a common path resistance from the board connector to the cell of 75mΩ, a wire harness resistance of 100mΩ and a cell voltage of 4V, the voltage level at CELLPLUS will be 4.875V.

In a similar manner, the EMB1432 cell measurement can be affected depending on design choices regarding the cell connection method. There are 2 choices:

- Separate cell sense connector (kelvin sense), with a connection to a point as close to the cell terminal as possible dedicated to the purpose of cell measurement.
- Cell sense connection that is shared with cell balance connection, with a significant portion of the cell measurement path also subject to cell balance charge/discharge currents.

9 System Power Supplies

9.1 Overview

An external power supply circuit will need to be designed to meet the system requirements with the following goals:

- Provide the supplies required by the system with as high efficiency as possible.
- Provide the ability to go into a shutdown or standby mode with extremely low quiescent power draw.
- Provide the ability to come out of shutdown or standby mode (wake-up) and reach a stable level in a reasonable amount of time.
- This will require the ability to control the supply generation to adapt to the needs of the system in a dynamic fashion, e.g. under the control of the microcontroller.
- Decoupling may also be required to achieve minimal quiescent current draw in shutdown mode.

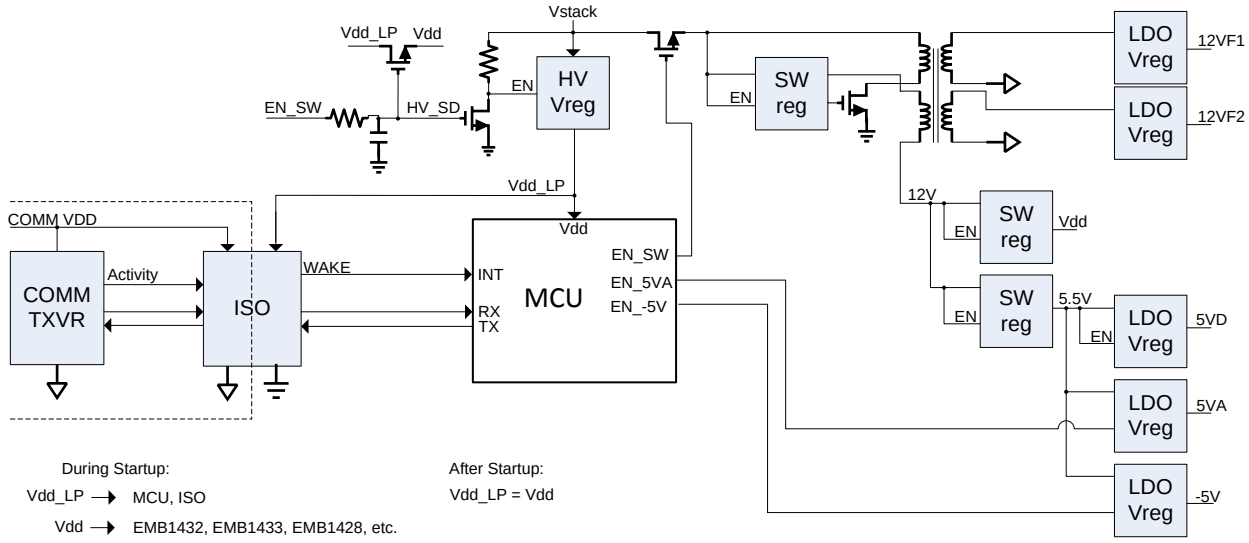


Figure 19 - Power Supply Proposal Block diagram

The design proposed here will supply 12V (3x 1 GND referenced, 2x floating), 5VD, 5VA, -5V and 3.3V from the BMS module cells as a source. A summary of the power supply requirements of the system are outlined in Section 13.1. A simple block diagram of the power supply can be seen in Figure 19. There are many possible strategies to provide these supplies, and customer requirements will also influence the design, including different internal or external sources. Other possible solutions are briefly discussed in Section 13.1.

9.2 Design

The HV linear regulator is required to provide a fast starting supply to the minimal circuits needed during system startup and initialization. It is not an efficient supply for continued operation, and therefore is intended to only be used during the MCU initialization or low power standby modes (depending on the MCU). As the HV linear regulator is only needed for initialization, it should be powering only the MCU (and any other peripheral circuits required during initialization). The HV linear regulator output should be

decoupled (via a FET) from the supply used by other ICs which are not required to be powered during initialization.

The switching regulator input is also decoupled by a FET to reduce the quiescent current during shutdown mode to a minimum. Once the MCU has been initialized, the EN_SW signal will turn on the switching regulator, which in turn will provide an efficient supply for all ICs VDD and VDDIO. Once the switching regulator output is stable, the circuits supplied by the HV linear regulator can be sourced from the switching regulator output (decoupling FET enabled), and HV linear regulator should be turned off. This is typically achieved by a fixed RC delay from the EN_SW signal (called HV_SD in the diagram).

A tested power supply design schematic is provided in Appendix , Section 14.1.10.

10 Appendix A

10.1 AFE Source Selection Tables

Source	Discrete MUX lines				SPI				
	MUX3	MUX2	MUX1	MUX0	Bit 3 (MSB)	Bit 2	Bit 1	Bit 0	FB* (LSB)
Battery 1	0	0	0	0	0	0	0	0	0
Battery 2	0	0	0	1	0	0	0	1	0
Battery 3	0	0	1	0	0	0	1	0	0
Battery 4	0	0	1	1	0	0	1	1	0
Battery 5	0	1	0	0	0	1	0	0	0
Battery 6	0	1	0	1	0	1	0	1	0
Battery 7	0	1	1	0	0	1	1	0	0
Battery 8	0	1	1	1	0	1	1	1	0
Battery 9	1	0	0	0	1	0	0	0	0
Battery 10	1	0	0	1	1	0	0	1	0
Battery 11	1	0	1	0	1	0	1	0	0
Battery 12	1	0	1	1	1	0	1	1	0
Battery 13	1	1	0	0	1	1	0	0	0
Battery 14	1	1	0	1	1	1	0	1	0
AUX1	Not Selectable				1	1	1	0	0
AUX2	Not Selectable				1	1	1	1	0

*Note – This function not fully described in this document. Please refer to EMB1432 datasheet.

11 Appendix B

11.1 EMB1428 Command / Output Table

Command [3:0]	Description	Direction	Cell	Converter			
			Vg[7:0]	Vg11	Vg10	Vg9	Vg8
0000b	STOP (Open all switches)	-	00000000b	0b	0b	0b	0b
0001b	START (Connect) cell 1	Charge	00000011b	1b	0b	0b	1b
0010b	START (Connect) cell 2	Charge	00000110b	0b	1b	1b	0b
0011b	START (Connect) cell 3	Charge	00001100b	1b	0b	0b	1b
0100b	START (Connect) cell 4	Charge	00011000b	0b	1b	1b	0b
0101b	START (Connect) cell 5	Charge	00110000b	1b	0b	0b	1b
0110b	START (Connect) cell 6	Charge	01100000b	0b	1b	1b	0b
0111b	START (Connect) cell 7	Charge	11000000b	1b	0b	0b	1b
1000b	Test mode (reserved)	-	00000000b	0b	0b	0b	0b
1001b	START (Connect) cell 1	Discharge	00000011b	1b	0b	0b	1b
1010b	START (Connect) cell 2	Discharge	00000110b	0b	1b	1b	0b
1011b	START (Connect) cell 3	Discharge	00001100b	1b	0b	0b	1b
1100b	START (Connect) cell 4	Discharge	00011000b	0b	1b	1b	0b
1101b	START (Connect) cell 5	Discharge	00110000b	1b	0b	0b	1b
1110b	START (Connect) cell 6	Discharge	01100000b	0b	1b	1b	0b
1111b	START (Connect) cell 7	Discharge	11000000b	1b	0b	0b	1b

11.2 EMB1428/EMB1499 Fault Code Table

Failure Description	Fault Code	Fault Interrupt Triggered?
DONE went high while EN was high and FAULT[2:0] != 3'b000	{1'b0, FAULT[2:0]}	yes
DONE went high while EN was high and FAULT[2:0] == 3'b000	4'b1100	yes
SDI sampled high when it should be low	4'b1101	yes
9th SCL_C rising edge seen while nCS is low	4'b1101	yes
nDIR_RT isn't the opposite of DIR	4'b1110	yes
nCS falling edge while the Switch & Tigon Control block is still waiting for a transition on DONE (rising or falling edge)	4'b1000	no
nCS falling edge while out_slew is high or we are waiting for it to go high	4'b1001	no
nCS falling edge while bg_good is low and the current command is not 4'h0 (open all switches)	4'b1011	no
Internal signal bg_good went low after it was sampled high	4'b1011	yes
No fault condition	4'b1010	no

12 Appendix C

12.1 Chipset Interface Signals

For up to 7 cells, 10 – 16 control signals are required. For 8 or more cells 12 – 19 control signals minimum are required.

Signal	IC	Pin	Description	Type
CLK	EMB1432	43	SPI Clock	Microcontroller SPI peripheral or GPIO
	EMB1426	8		
	EMB1428	27		
SDI	EMB1432	41	SPI slave input	Microcontroller SPI peripheral MOSI or GPIO
	EMB1428	28		
SDO	EMB1432	44	SPI slave output	Microcontroller SPI peripheral MISO or GPIO
	EMB1426	7		
	EMB1428	29		
MUX0 (NOTE 1)	EMB1432	1	MUX selection bit 0	Microcontroller GPIO (output)
MUX1 (NOTE 1)	EMB1432	48	MUX selection bit 1	Microcontroller GPIO (output)
MUX2 (NOTE 1)	EMB1432	47	MUX selection bit 2	Microcontroller GPIO (output)
MUX3 (NOTE 1)	EMB1432	46	MUX selection bit 3	Microcontroller GPIO (output)
nSD (NOTE 2)	EMB1432	40	Shutdown (active low)	Microcontroller GPIO (output)
nRS (NOTE 2)	EMB1432	39	Reset (active low)	Microcontroller GPIO (output)
FAULT_INT (NOTE 3)	EMB1428	31	Fault interrupt source	Microcontroller GPIO (interrupt input)
RESET	EMB1428	35	Reset (active high)	Microcontroller GPIO (output)
VSET (NOTE 3)	EMB1499	6	Current set point	Microcontroller DAC or PWM (with low-pass filter) output
nCS (NOTE 4)	EMB1432	42	SPI chip select (active low)	Microcontroller GPIO (output)
nCS	EMB1426	6	SPI chip select (active low)	Microcontroller GPIO (output)
nCS (NOTE 3)	EMB1428	30	SPI chip select (active low)	Microcontroller GPIO (output)
Inrush limit bypass	Q46 (NOTE 5)		Enables FET bypass of in-rush limit circuit	Microcontroller GPIO (output)

NOTE 1 – The MUX[3:0] signals are only required if the fastest switch rate of the EMB1432 is desired.
NOTE 2 – Can be tied high, or controlled by microcontroller lowest current in shutdown.
NOTE 3 - 2 of these interface signals are required for if design includes more than 7 cells.
NOTE 4 – This signal is only required if the EMB1432 Open Wire Sense feature will be used, or SPI control of the EMB1432 is desired.
NOTE 5 – Q46 is described in Section 4.2.

12.2 Optional Interface Signals

These are extra signals which may be necessary for additional optional features such as temperature sensing or power supply control.

Signal	IC	Pin	Description	Type	Description
nCS	EMB1402	1	SPI chip select (active low)	Microcontroller GPIO (output)	ADC (Temp Sense) CS
EN	EMB1420	7	Enable (active high)	Microcontroller GPIO (output)	HV Switching Regulator enable
EN	EMB1487	4	Enable (active high)	Microcontroller GPIO (output)	-5V enable

13 Appendix D

13.1 Power Supply Rails (TBD)

The supplies listed below are separate power supply rails or planes and the respective pin connections in the chipset. Please refer to the system schematic for detailed description.

Supply	IC	Signal	Pin	Description
2.7 – 5.5V	EMB1432	VIO	3	IO supply
	EMB1433	VIO	3	IO supply
	EMB1428	VDD_IO	32	IO supply
	EMB1426	VIO	9	IO supply
	EMB1402	VA	2	Analog supply
		VD	13	Digital/IO supply
	Microcontroller	VDD		VDD, VDDA and/or VDDIO
	EMB1424	VCC	5	Supply
5V	EMB1432	CHPVP	35	Charge pump supply
	EMB1433	CHPVP	35	Charge pump supply
12V	EMB1428	VDD_12V	34	
	EMB1499	VINA	16	
	EMB1499	VINP	21	
	EMB1412	VCC	4, 6	Low-side driver supply
GND	EMB1432	DGND	4	Digital GND
	EMB1433	DGND	4	Digital GND
	EMB1428	GND	13, 36, DAP	Digital GND
	EMB1428	GNDP	1	Charge pump GND
	EMB1426	GND	5	ADC digital GND
	EMB1499	GND	GNDA, GNDP, DAP	
	EMB1412	VEE	1, 3, DAP	Low-side driver GND
	EMB1402	AGND	3	Analog GND
		DGND	12	Digital GND
	Microcontroller	GND		GND, GNDA
	EMB1424	GND	1, 2	Supply GND
5V (analog)	EMB1432	VP	28	Charge pump supply
	EMB1433	VP	28	Analog supply
	EMB1433	VPREF	29	Voltage reference supply
	EMB1426	VA	10	Analog supply
-5V	EMB1432	VM	32	Negative voltage supply
AGND	EMB1432	GND	5, 23, DAP	Analog GND
	EMB1433	GND	5, 23, DAP	Analog GND
RGND	EMB1432	GNDREF	31	Reference GND
	EMB1426	GND	4	Analog GND
	REF5025	GND	4	Supply GND
RGND_BSP	EMB1433	GNDREF	31	Reference GND
12VF1	EMB1499	PVINF	22	Floating 12V supply
	EMB1499	VINF	28	Floating 12V supply
GNDF1	EMB1499	PGNDF	24	Floating GND
	EMB1499	GNDF	27	Floating GND

12VF2	EMB1499	PVINF	22	Floating 12V supply
	EMB1499	VINF	28	Floating 12V supply
GNDF2	EMB1499	PGNDF	24	Floating GND
	EMB1499	GNDF	27	Floating GND

14 Appendix E

14.1 Chipset Schematic

14.1.1 Top Level

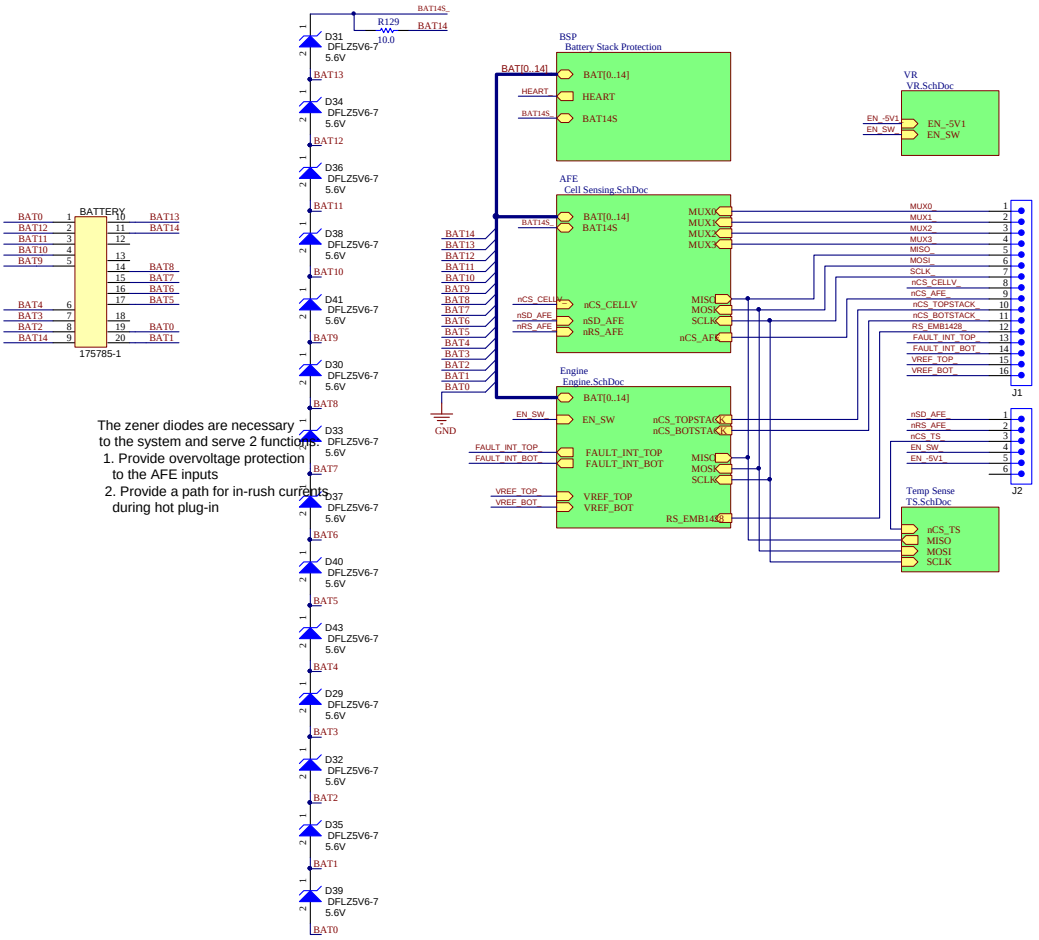


Figure 20 - Top Level Schematic

14.1.2 Cell Sensing

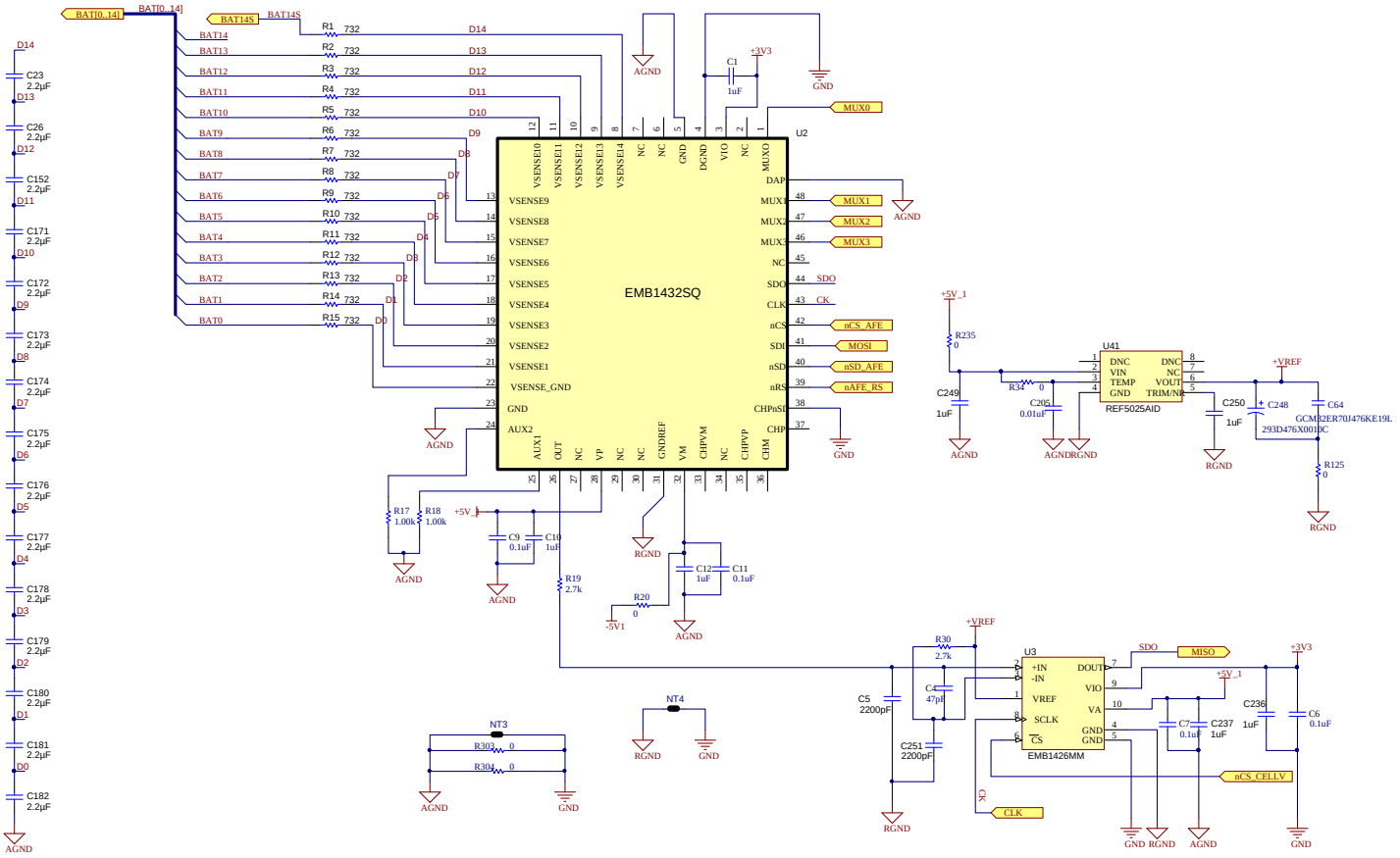


Figure 21 - Cell Sensing Schematic

14.1.3 Battery Stack Protection

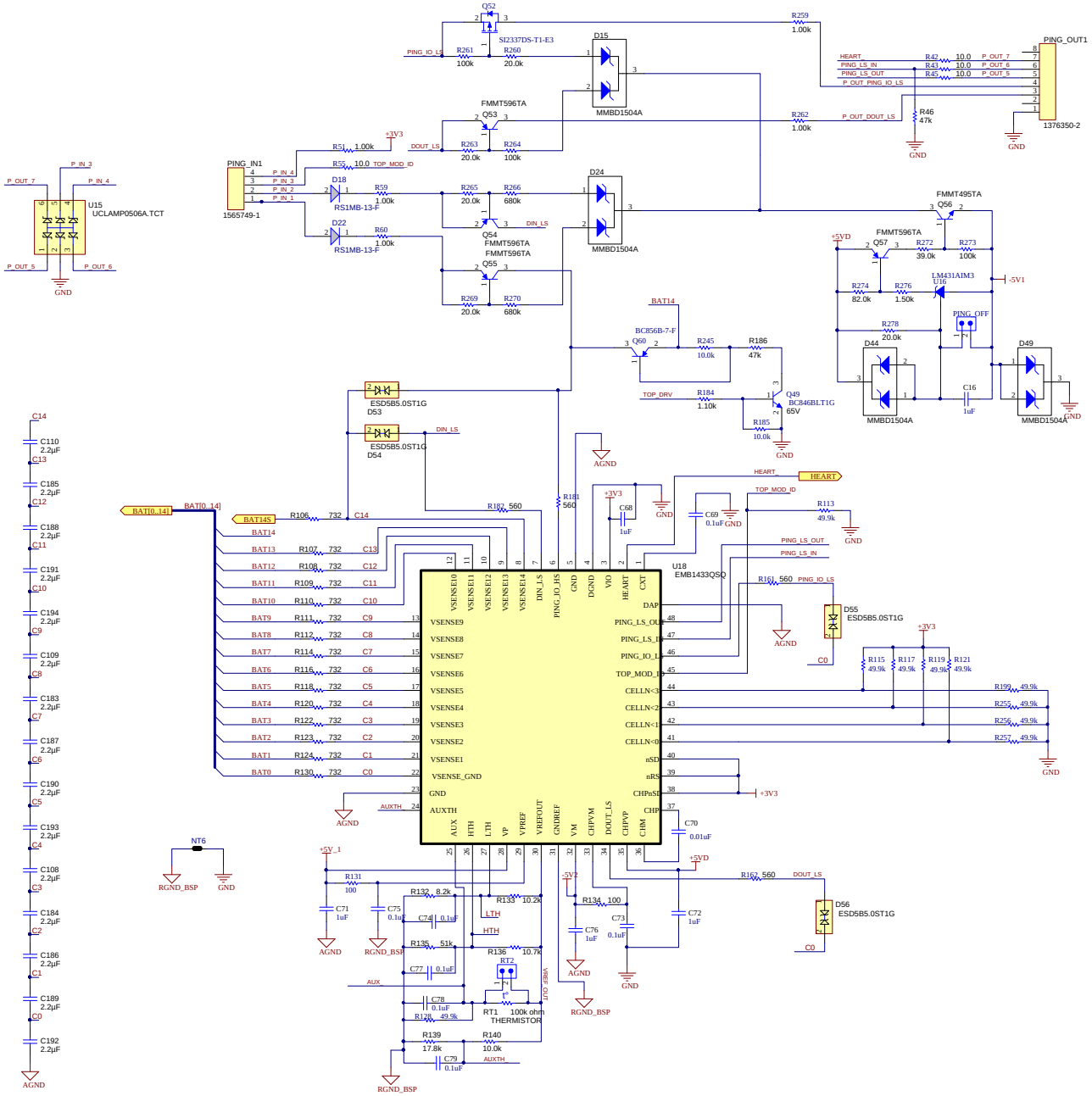


Figure 22 – Battery Stack Protection Schematic

14.1.4 Active Cell Balance Top Level

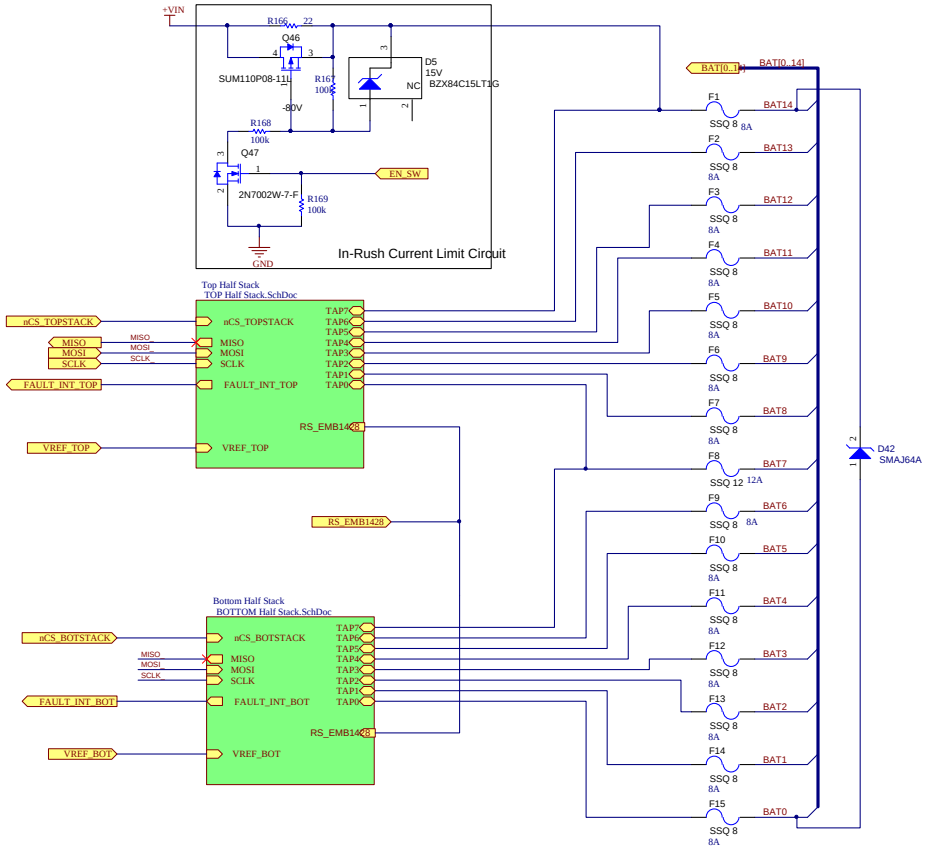


Figure 23 – Active Cell Balance Top Level Schematic

14.1.5 Bottom Half-Stack Switch Matrix

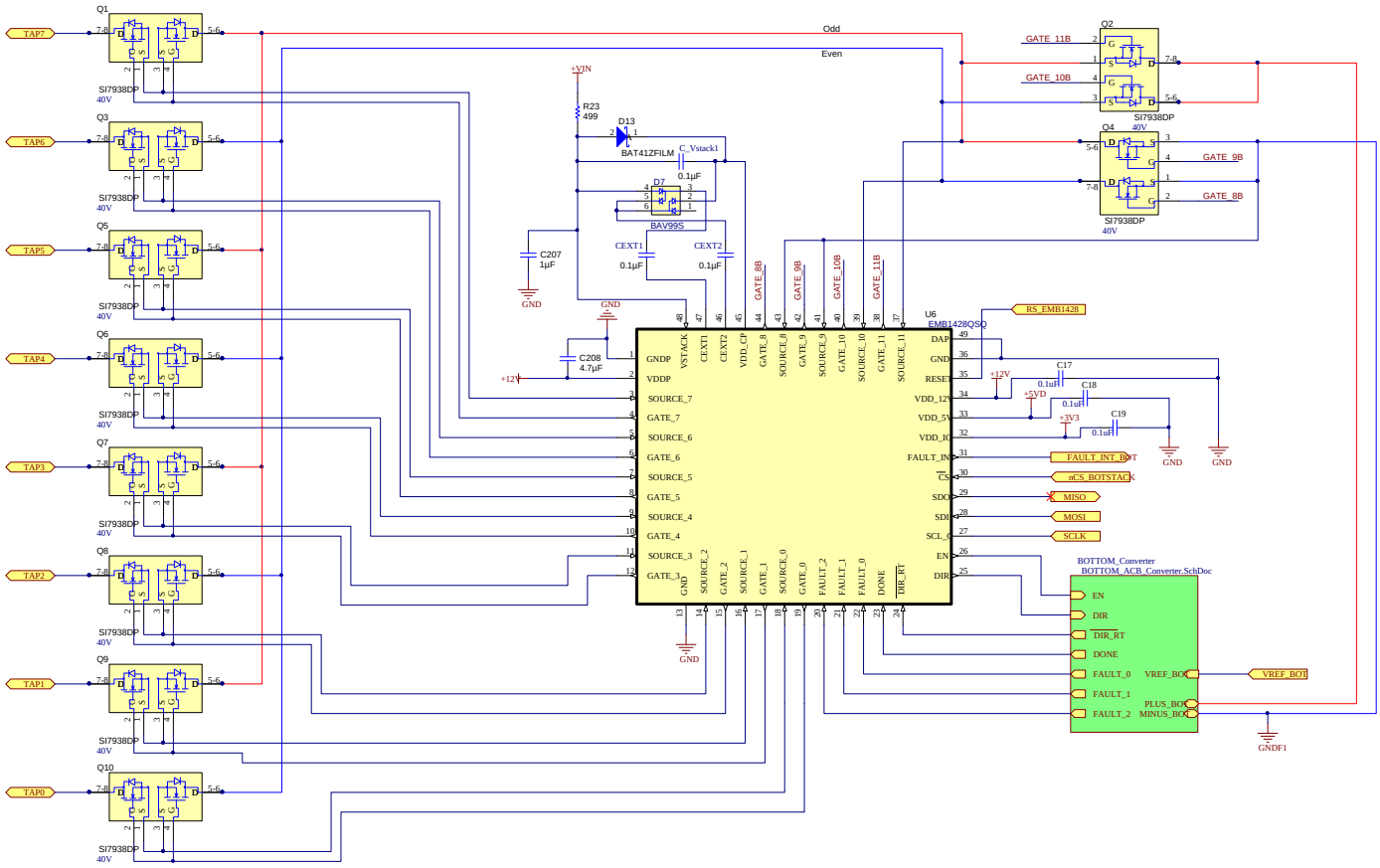


Figure 24 – Bottom Half-Stack Switch Matrix Schematic

14.1.6 Bottom Converter

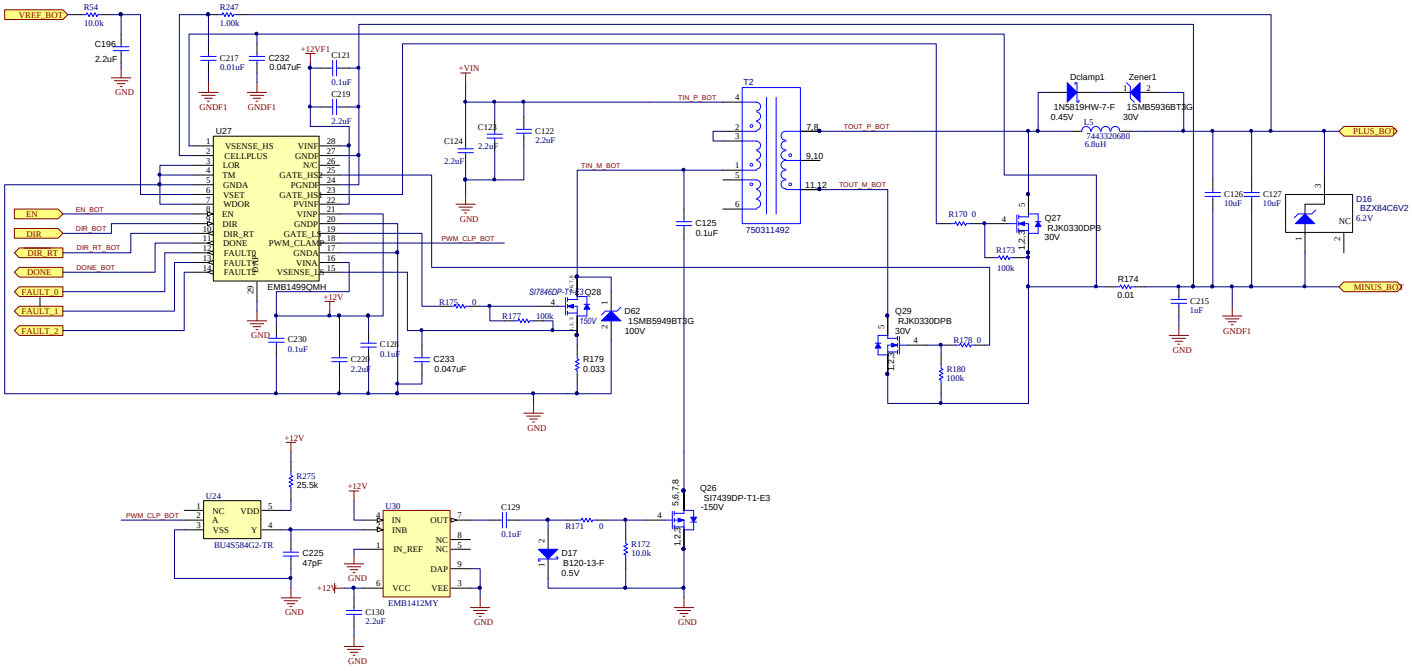


Figure 25 – Bottom Converter Schematic

14.1.7 Top Half-Stack Switch Matrix

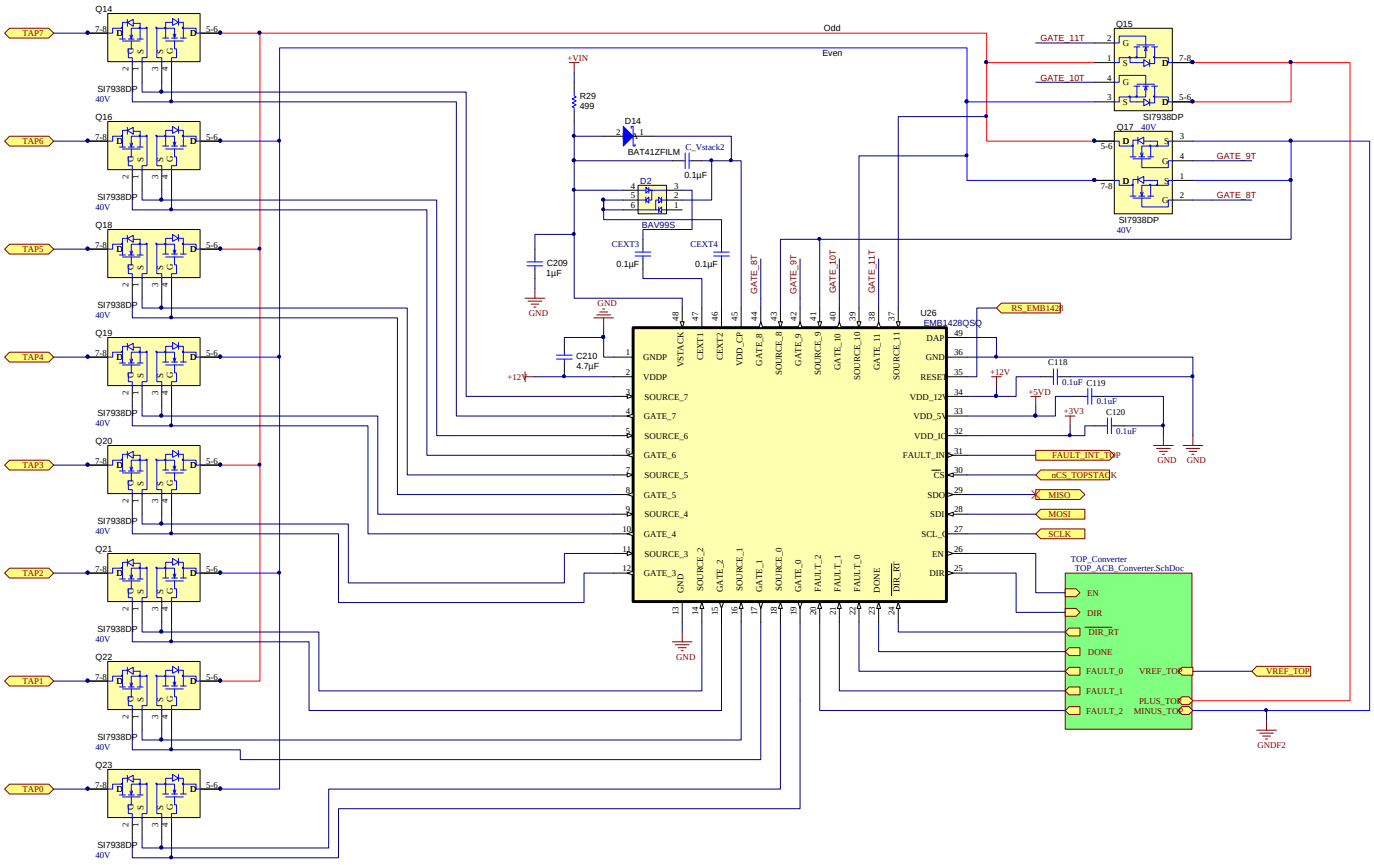


Figure 26 – Top Half-Stack Switch Matrix Schematic

14.1.8 Top Converter

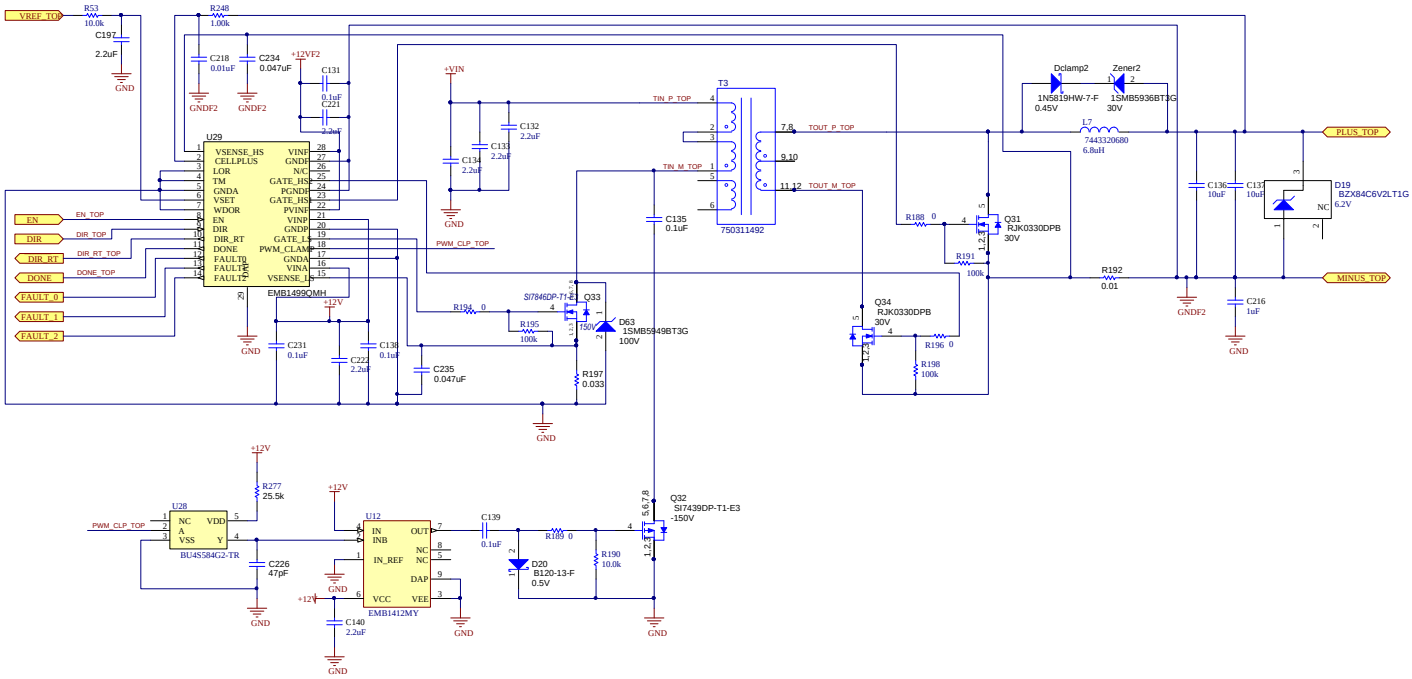


Figure 27 – Top Converter Schematic

14.1.9 Temperature Sensing

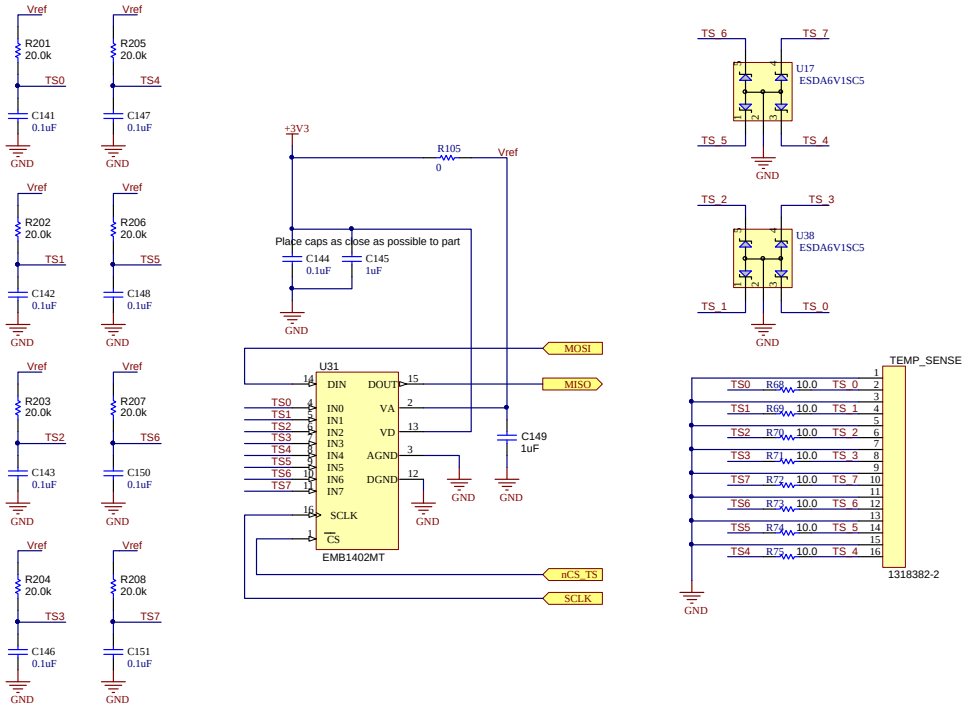


Figure 28 – Temperature Sensing Schematic

14.1.10 Power Supply

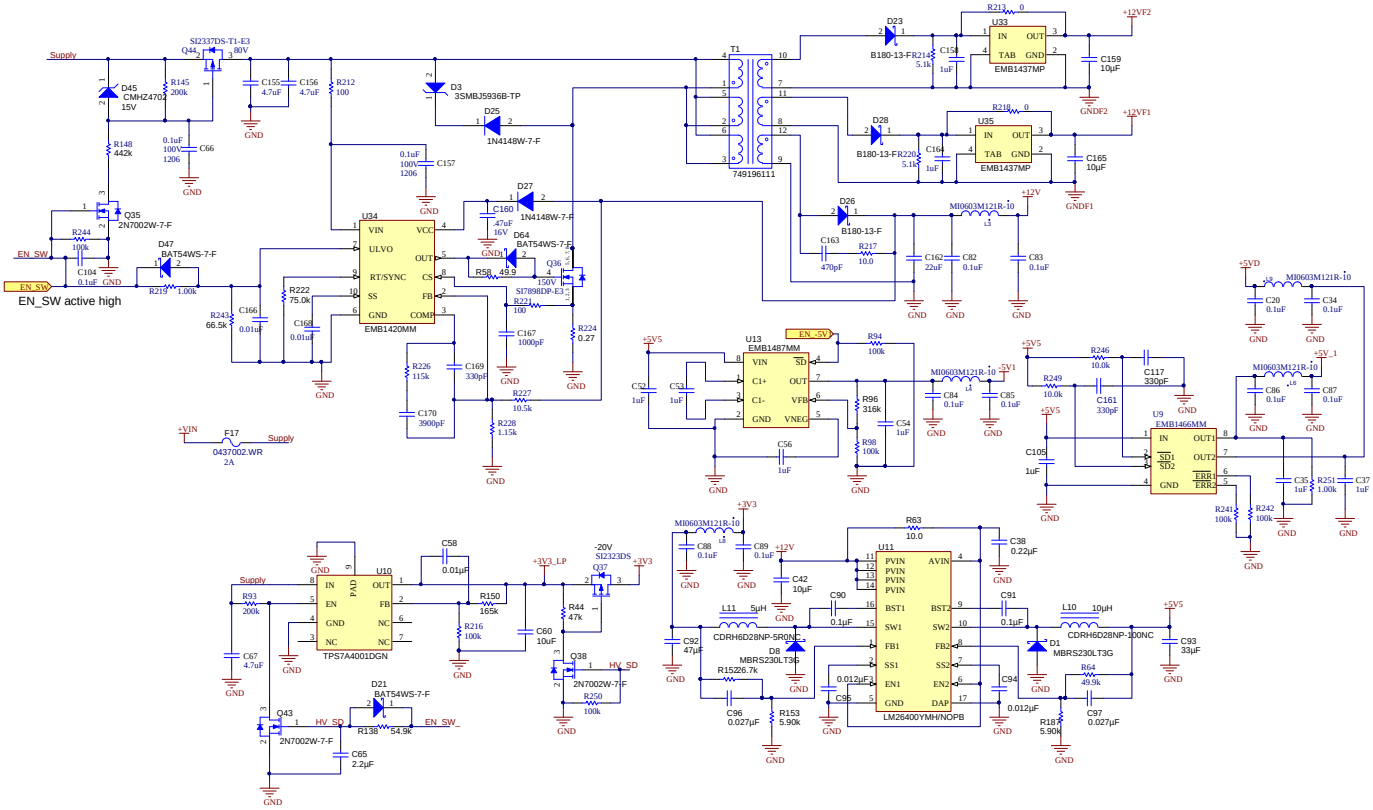


Figure 29 – Power Supply Schematic

15 Revision History

This section records a brief summary of changes to each revision of this document.

Revision	Date	Author	Description of Changes from Previous Revision
1.0	11/16/2011	Stephen Holland	First release
1.1	01/17/2012	Stephen Holland	Updated description of switch matrix FETs (section 6.1) Added detailed description of the VSET, sense resistors, clamp circuit, input capacitor and output capacitor device selection
1.2	01/19/2012	Stephen Holland	Updated description of active clamp circuit, added diagram Revised FET selection guidelines
1.3	02/14/2012	Stephen Holland	Changed name of document from EM1451 to Active Chipset
1.4	03/28/12	Stephen Holland	Changed classification rom 'NDA Required' to 'Selective Disclosure' Adjusted some page layout
1.5	04/26/12	Stephen Holland	Removed Electrical Characteristics (was Appendix C) User should refer to device datasheets Updated TOC