



How can we adjust the DESAT detection threshold?

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Intro

DESAT is a short-circuit/overcurrent detection system integrated in UCC5870, UCC217xx, and ISO5x5x. As its name suggest, DESAT detects "desaturation" of an IGBT and is triggered when V_{CE} rises above a certain threshold set by the design. V_{CE} rising corresponds with the IGBT leaving saturation region and approaching the active region. After DESAT detection, gate drivers (including ISO5x5x and UCC217xx families) will immediately begin pulling the gate low to turn off the IGBT and end the short circuit condition.

Gate drivers with DESAT protection have a built-in threshold which is effective for many IGBTs, but could be slightly too high or too low for other IGBTs or other types of device. This DESAT detection threshold can be tailored to suit different devices simply by changing discrete components in the DESAT circuit.

What is Desaturation in an IGBT?

The optimal operating point of IGBTs in power applications is in the saturation region, where V_{CE} and thus dissipated power are controlled. In the event of a short circuit condition (for example if both high and low-side IGBTs get turned ON simultaneously), V_{CE} will rise quickly while collector current saturates. This puts the IGBT in the active region of operation. A general I_C V_{CE} curve is shown in [Figure 1](#).

Active region is very undesirable for IGBTs in power applications because this causes unsustainably high power dissipation in the bipolar junction and a swift failure of the IGBT itself. This "desaturation" concept is in contrast to FETs, where rising V_{GS} leads to the device approaching saturation region (rather than leaving it), and where devices are operated in the linear region for power applications. [Please see here](#) for additional information on Desaturation.

In FETs, DESAT detection would therefore be utilized for detecting "saturation" rather than "desaturation," though for SiC FETs in particular direct Over-current can be preferable due to SiC's drain characteristics. The difference in DESAT efficacy between IGBT and SiC is explained further in [this eBook](#).

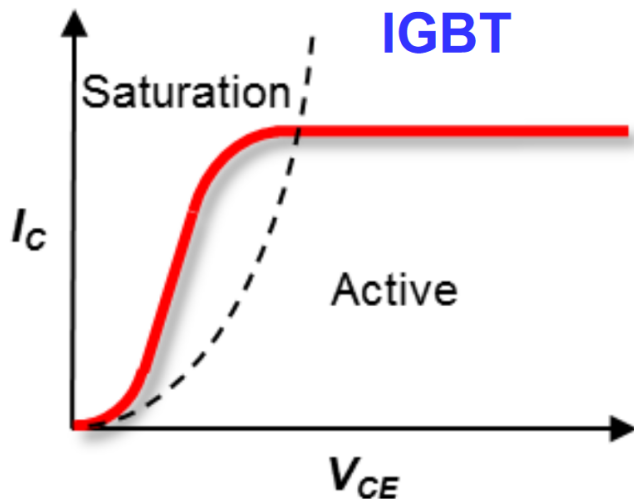


Figure 1: IGBT Collector Characteristics



How does the DESAT detection circuit work?

DESAT system detects when the collector voltage V_{CE} is above a threshold, V_{DESAT} , though not directly.

Figure 2 shows a standard DESAT implementation.

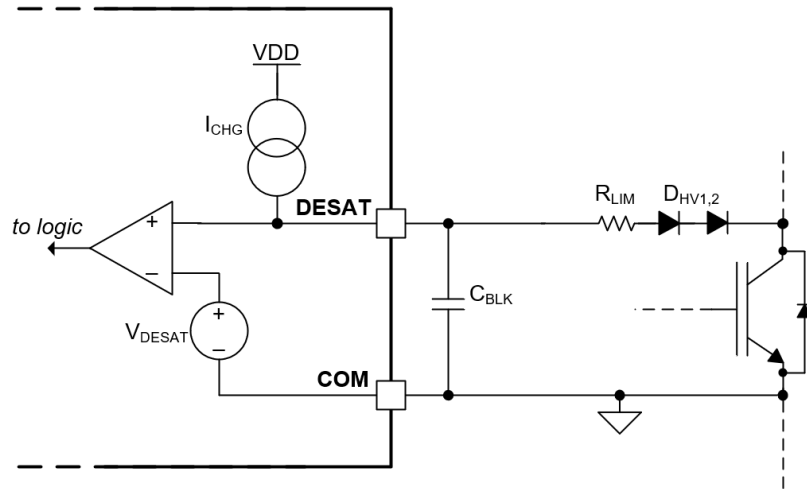


Figure 2: Typical DESAT circuit

During normal operation, the IGBT is in saturation, V_{CE} is low and the diodes $D_{HV1,2}$ are forward biased. The I_{CHG} current can then flow through the diodes to the collector, preventing the blanking capacitor C_{BLK} from charging, as shown in

Figure 3.

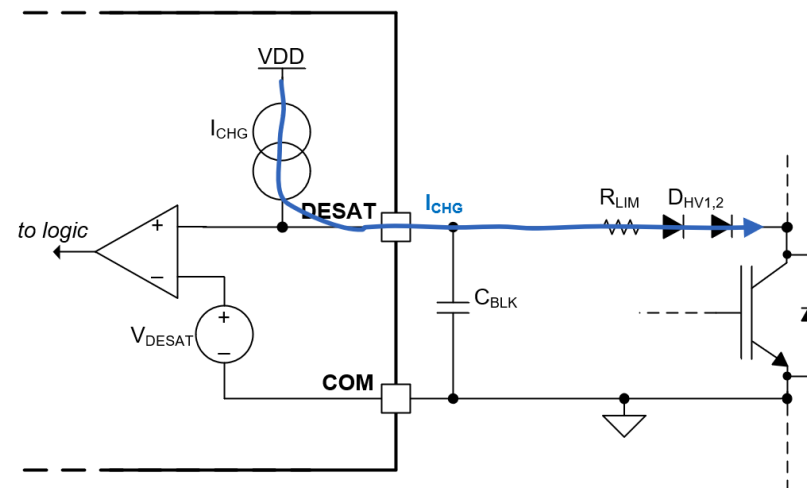




Figure 3: DESAT circuit during normal IGBT operation

In short-circuit, V_{CE} rises and reverse-biases $D_{HV1,2}$, so the I_{CHG} current now charges the blanking capacitor C_{BLK} , as shown in [Figure 4](#).

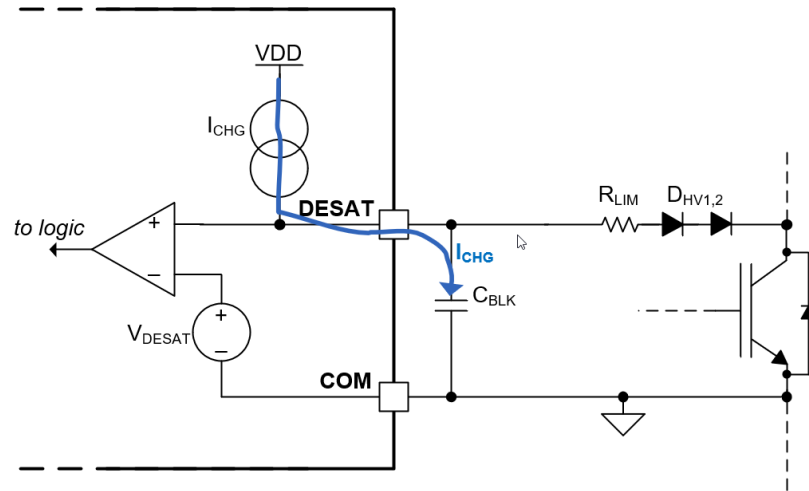


Figure 4: DESAT during Short-circuit

After a time (set by the capacitance value), the voltage on the cap exceeds the internal threshold V_{DESAT} and the comparator indicates that DESAT is detected. The collector voltage where I_{CHG} begins charging the blanking capacitor is $V_{CE,DESAT}$. This is considered the DESAT detection threshold.

Due to the presence of the $D_{HV1,2}$, the voltage at the **DESAT** pin when the current source begins charging the blanking capacitor will be *higher* than V_{CE} by 1 or 2 forward voltage drops, or $V_{CE} + 2 \cdot V_F$. We must also consider the drop across the series resistor R_{LIM} due to the internal current source. Therefore, we find the effective DESAT threshold as $V_{CE,DESAT} = V_{DESAT} - 2 \cdot V_F - I_{CHG} \cdot R_{LIM}$.

In short, the DESAT threshold is the voltage when the diodes stop conducting, which tells the system V_{CE} is too high.

Why adjust the DESAT threshold?

Not all IGBTs are identical, so their V_{CE} / I_C transfer characteristics are also different.

The DESAT detection threshold is usually chosen at the "knee voltage" (often 7-10V), depicted in [Figure 5](#), which is the point at which the collector current saturates and is akin to V_{DSAT} for MOSFETs. Designers may wish to choose the effective DESAT detection threshold to suit an IGBT with a different knee voltage, or possibly choose a threshold below the knee voltage to have earlier DESAT detection.

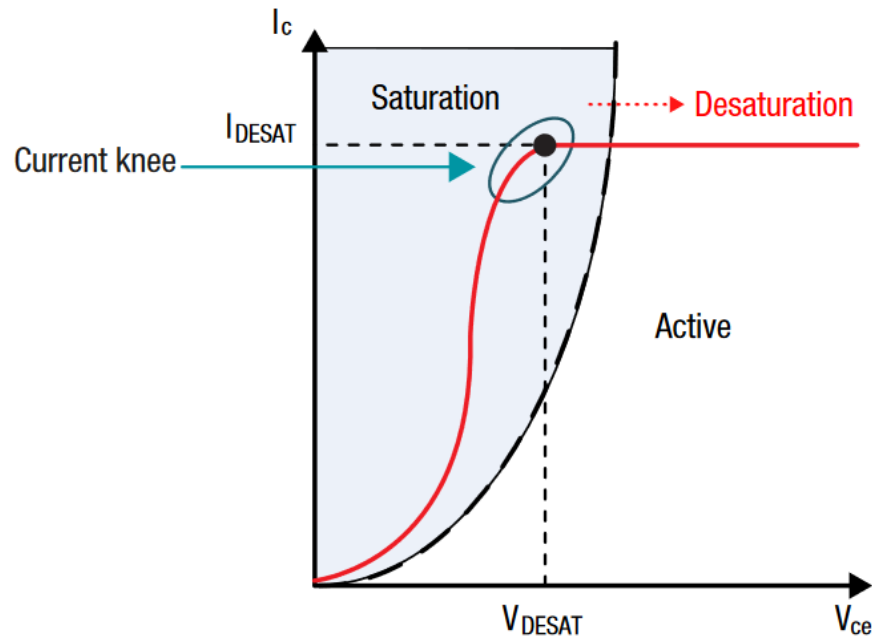


Figure 5: IGBT Current Knee

How do we adjust the DESAT threshold?

The methods to adjust the DESAT detection threshold involve making changes to the components in series between the **DESAT** pin and the IGBT collector. These methods are summarized in [Table 1](#)

Changing the number of series HV blocking diodes allows us to *decrease* the threshold in steps of the diode V_F . Similarly, we can increase the detection threshold in larger increments by adding a zener diode, as shown in [Figure 6](#). With this, we find that

$V_{CE,DESAT} = V_{DESAT} - V_Z - n \cdot V_F - I_{CHG} \cdot R_{LIM}$, where n is the number of HV blocking diodes, minimum 1, though often 2 are necessary in order to stand off working voltages of 1kV and up.

To a lesser extent, small adjustments to the threshold can also be made by changing the value of R_{LIM} , though this should not be used for adjustments larger than a few hundred mV. A zener diode may be used to make larger (for example, 3V) changes to the DESAT detection threshold and are available in several knee voltages. When selecting a zener, the voltage drop will depend on the current bias—in this case, I_{CHG} .

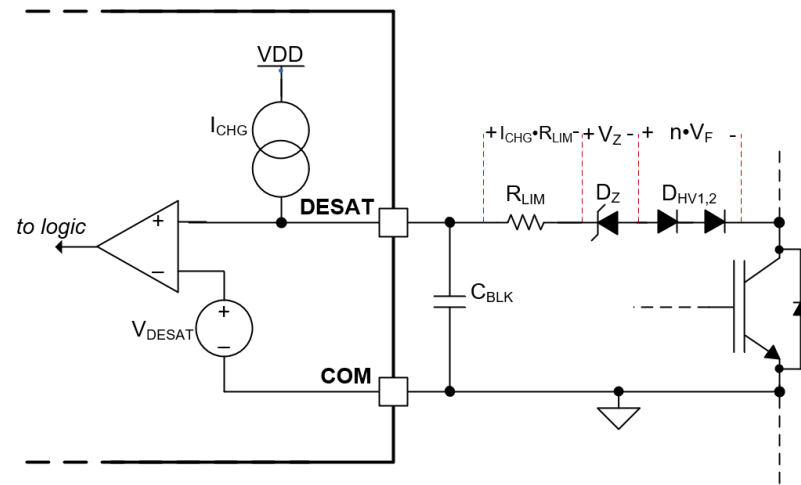


Figure 6

Change	Effect on DESAT Threshold
Add (or remove) HV Blocking diodes	Decreases threshold by total diode V_F s
Add a zener diode	Decreases threshold by zener V_Z
Change limiting resistor value	Decreases threshold by $I_{CHG} \cdot R_{LIM}$

Table 1: DESAT Threshold Adjustments Summary

References & additional resources

- IGBT & SiC Gate Driver Fundamentals
- High Voltage Interactive - How to protect SiCMOSFETs... the best way!