

Details :

The Aux supply is the 5V0.

When this fails PFI signal goes low.

Thus generating the PFO signal.

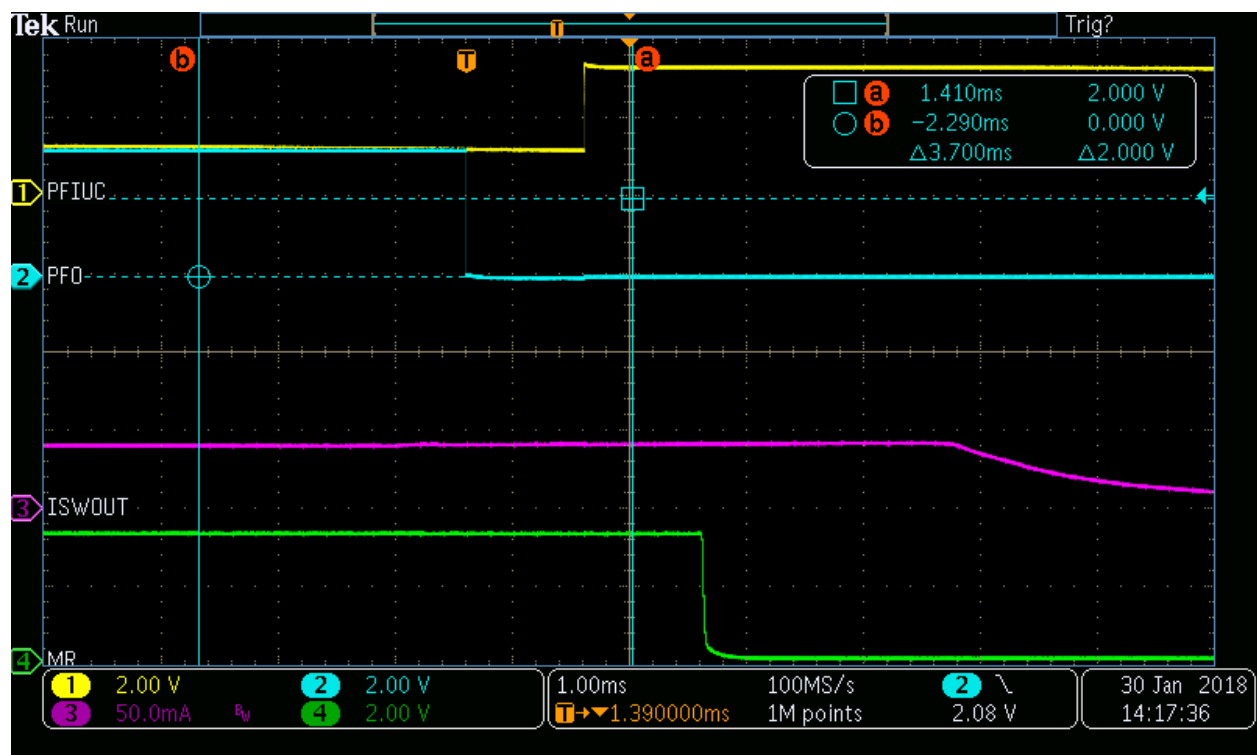
The uC makes PFO pin as output and grounds it.

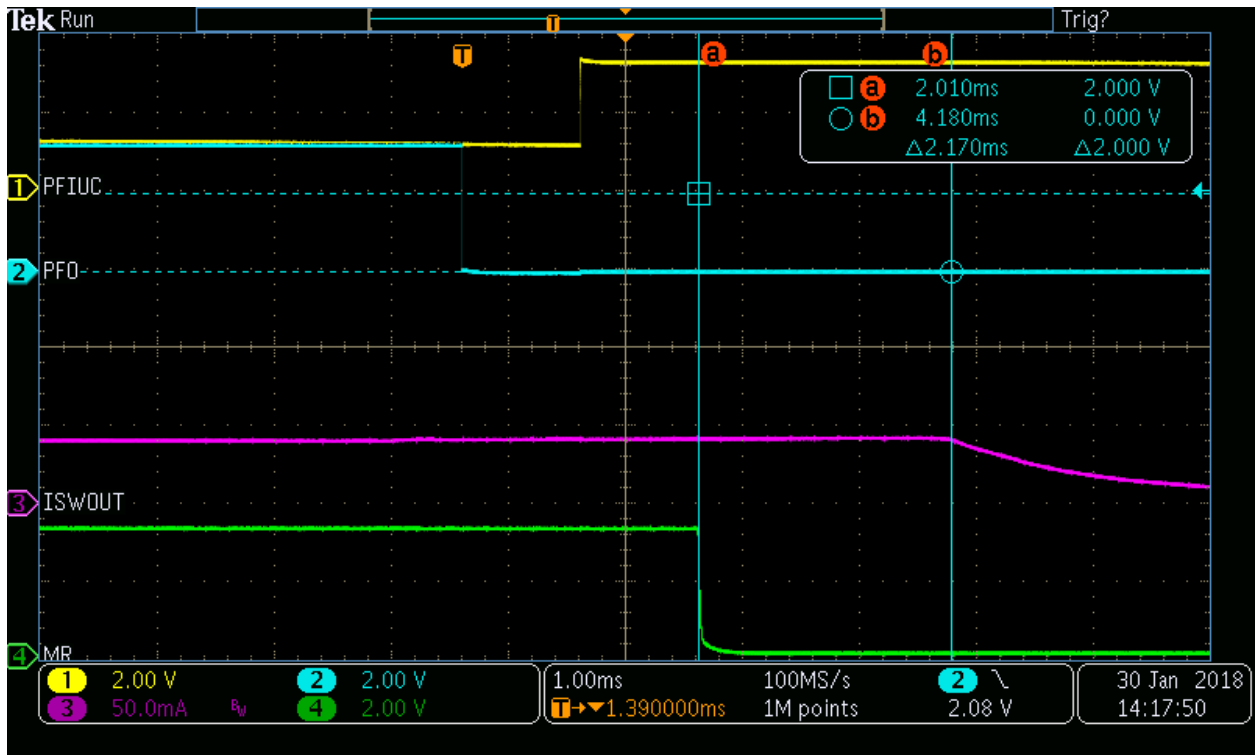
After 1 msec delay the uC generates the GPIO17 to raise PFI to 3.3V.

After 1 msec delay the uC grounds the MR pin.

Results :

With these steps the device goes into BFM mode. To know BFM mode entry we monitor the current on the Vout pin 3v3_SW_out current. We observe elow waveforms.



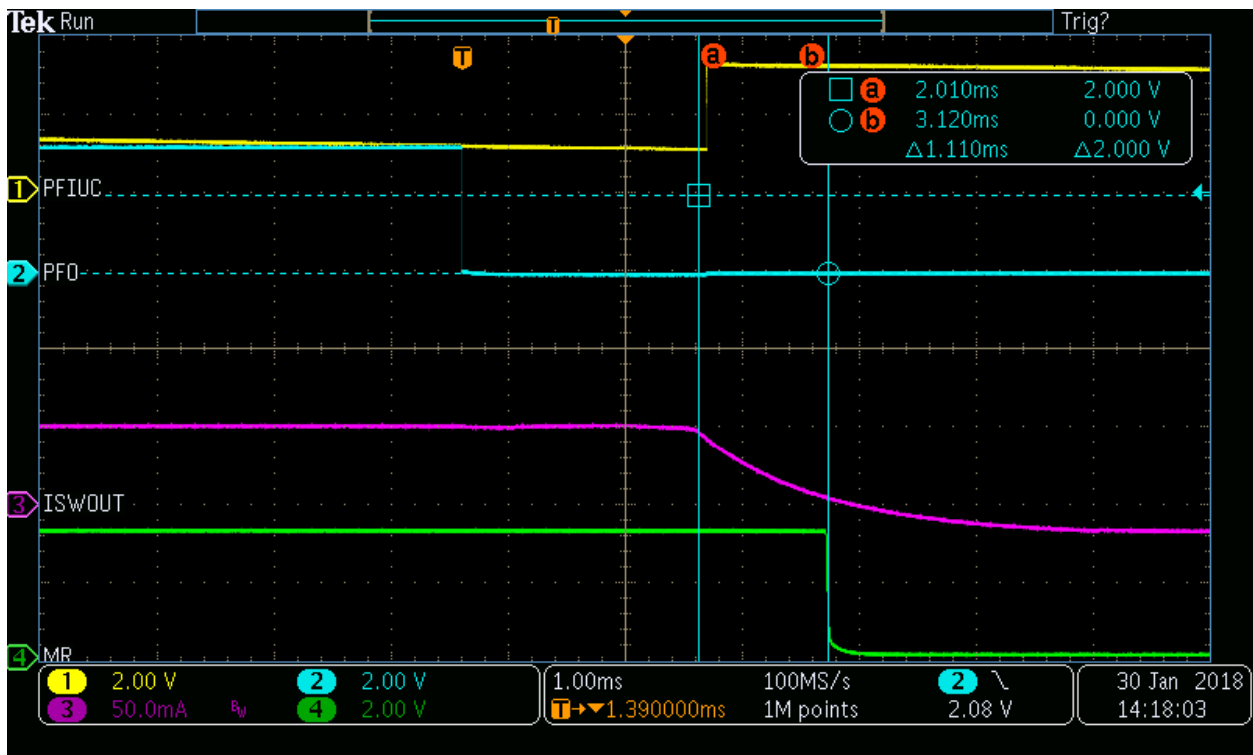


See above wf.

ISWOUT shows a DIP after the last step in which MR goes low.

This is ideal condition.

Query :



See the above wf.

Here the ISWOUT dips below the steady level before the MR goes low. Does this mean the BFM mode is triggered before the MR goes low ?

What is the reason for this?

At what point is the BFM mode actually entered ?

Some more waveforms for your reference :

