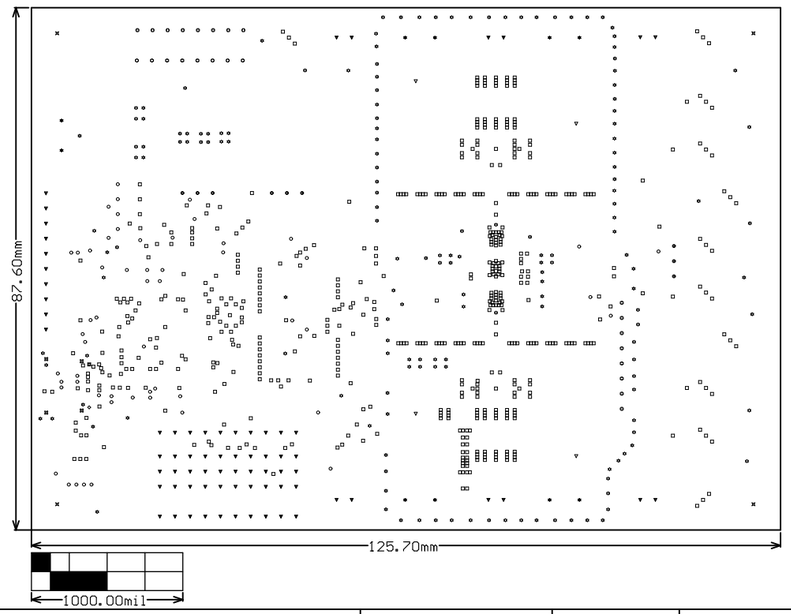

Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.010mm	3.5	
3	Top Layer	Copper	0.070mm		
4	Dielectric 1	FR-4	0.150mm	4.2	
5	GND Layer 1	Copper	0.035mm		
6	Dielectric 2	FR-4	0.250mm	4.2	
7	Signal Layer 1	Copper	0.035mm		
8	Dielectric 3	FR-4	0.500mm	4.2	
9	Signal Layer 2	Copper	0.035mm		
10	Dielectric 4	FR-4	0.250mm	4.2	
11	GND Layer 2	Copper	0.035mm		
12	Dielectric 5	FR-4	0.150mm	4.2	
13	Bottom Layer	Copper	0.070mm		
14	Bottom Solder	Solder Resist	0.010mm	3.5	
15	Bottom Overlay				

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
◘	1	0.650mm (25.59mil)	NPTH	Round	Top Layer - Bottom Layer	
▽	4	1.100mm (43.31mil)	NPTH	Round	Top Layer - Bottom Layer	
□	579	0.200mm (7.87mil)	PTH	Round	Top Layer - Bottom Layer	
○	55	0.400mm (15.75mil)	PTH	Round	Top Layer - Bottom Layer	
✡	167	0.500mm (19.69mil)	PTH	Round	Top Layer - Bottom Layer	
▼	72	1.016mm (40.00mil)	PTH	Round	Top Layer - Bottom Layer	
✪	24	1.020mm (40.16mil)	PTH	Round	Top Layer - Bottom Layer	
◙	9	1.150mm (45.28mil)	PTH	Round	Top Layer - Bottom Layer	
✽	10	1.200mm (47.24mil)	PTH	Round	Top Layer - Bottom Layer	
✖	4	3.048mm (120.00mil)	PTH	Round	Top Layer - Bottom Layer	
◇	1	0.650mm (25.59mil)	NPTH	Slot	Top Layer - Bottom Layer	
⊠	4	0.500mm (19.69mil)	PTH	Slot	Top Layer - Bottom Layer	
	930 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

BOARD SIZE (REFER ALSO ARRAY/PANEL PROFILING INFORMATION)
125.7mm X 87.6mm

Number of Layers : 6
MIN. TRACK WIDTH: 0.2 mm
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 0.5 mm
MINIMUM ANNULAR RING 0.15mm (6MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
COPPER THICKNESS (FINISHED):
OUTER: [ ] 1.4MIL (1oz) [ ] 2MIL (1.4oz) [X] 2.8MIL (2oz)
INNER SIGNAL: [X] 1.4MIL (1oz) [ ] 2.8MIL (2oz) [ ] N/A
DRILLING:
REFERENCE: [ ] AS SHOWN [X] NC_DRILL FILES
PTH MIN COPPER THICKNESS: [X] 1MIL [ ] OTHER _____
BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR:
[ ] GREEN [X] BLUE [ ] OTHER _____
SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER _____
ARRAY/PANEL: [X] CUT AND TRIM PER MECH LAYER 1
[ ] N.C. ROUTE [ ] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] UL 94V-0 [X] RoHS [ ] OTHER PER ORDER
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER
ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER
MANUFACTURER'S UL: [ ] RAIL [ ] METAL [X] SILK
VIA FILLING AND CAPPING PER IPC-4761 Type VII

TEXAS INSTRUMENTS

PROJECT TITLE: LP8764xQ1EVM
DESIGNED FOR: Public Release
FILE NAME: BMC062E2.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: BMC062	REV: E2	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 10/26/2020 12:36:21 PM	TEXAS INSTRUMENTS	

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.

ENGINEER:	LAYOUT BY:
Jari NiemelΣ	Jari NiemelΣ
SCALE: 1.00	ALTIUM DESIGNER VERSION: 18.1.9.240