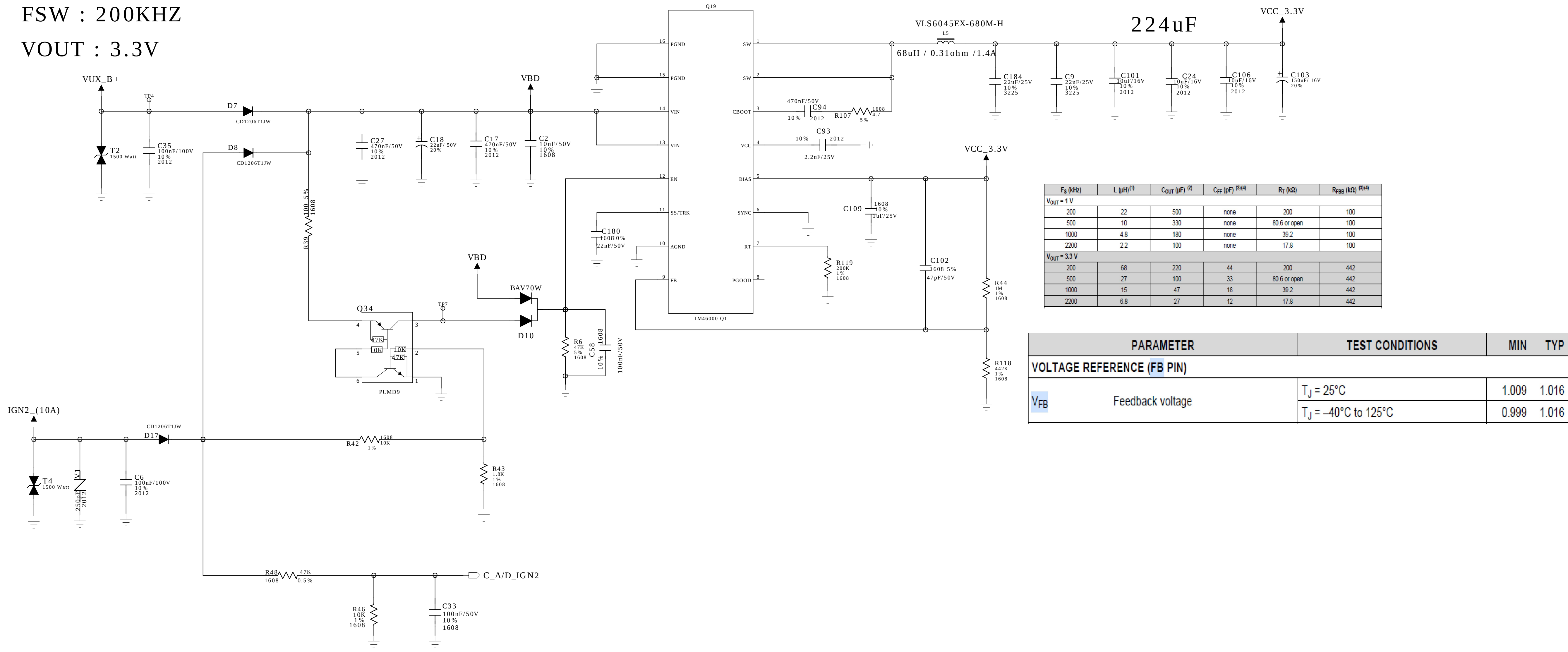


VIN 8 ~ 16V
FSW : 200KHZ
VOUT : 3.3V

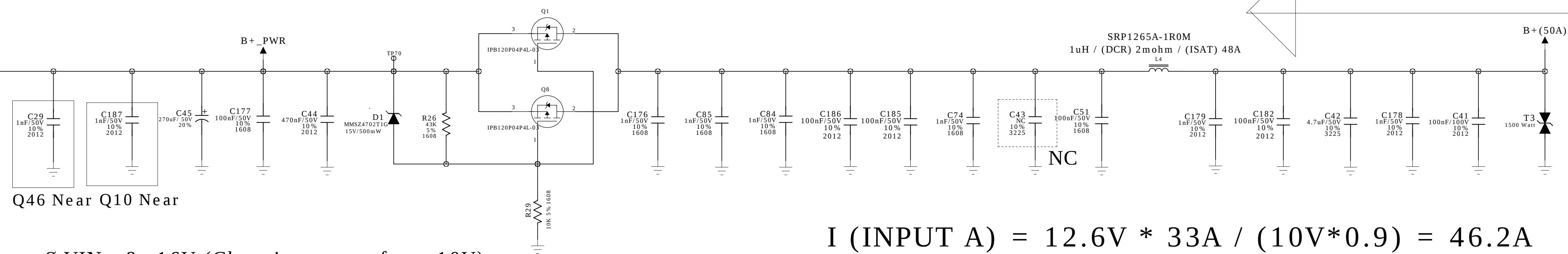


F _s (kHz)	L (μH) ¹⁾	C _{out} (μF) ²⁾	C _{err} (pF) ³⁾	R _z (kΩ)	R _{eqn} (kΩ) ⁴⁾
V _{out} = 1 V					
200	22	500	none	200	100
500	10	330	none	80.6 or open	100
1000	4.8	180	none	39.2	100
2200	2.2	100	none	17.8	100
V _{out} = 3.3 V					
200	68	220	44	200	442
500	27	100	33	80.6 or open	442
1000	15	47	15	39.2	442
2200	6.8	27	12	17.8	442

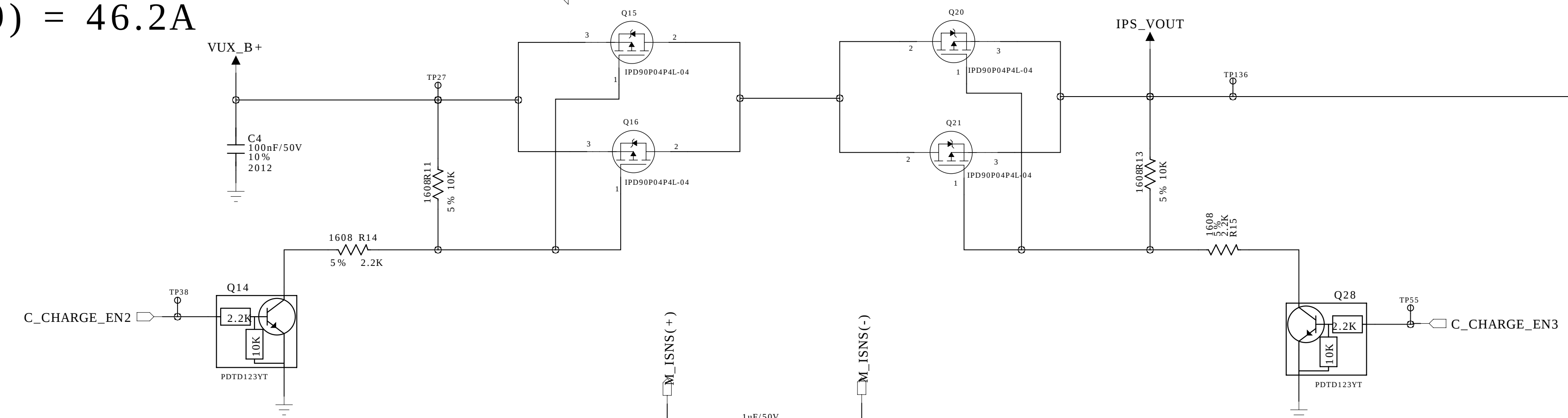
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE (FB PIN)					
V _{FB}	Feedback voltage				V
	T _J = 25°C	1.009	1.016	1.023	
	T _J = -40°C to 125°C	0.999	1.016	1.039	

		COMPANY:				
		TITLE:				
		BMS				
DRAWN: JH CHO	DATED: 18.02.28					
CHECKED: JH CHO	DATED: 12.06.18	CODE:	SIZE:	DRAWING NO:	REV:	
QUALITY CONTROL: < QC By >	DATED: < QC Date >	< Code >	E	REVISION	2.00	
RELEASED: < Released By >	DATED: < Release Date >	SHEET: 1 OF 3				

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

$$ID(FET) = \text{Square} \left((175-75) / (4.4\text{mohm} * 40) \right) = 23.8A \quad (23.8*2 = 47.6A)$$

$$I (\text{INPUT A}) = 12.6\text{V} * 33\text{A} / (10\text{V} * 0.9) = 46.2\text{A}$$

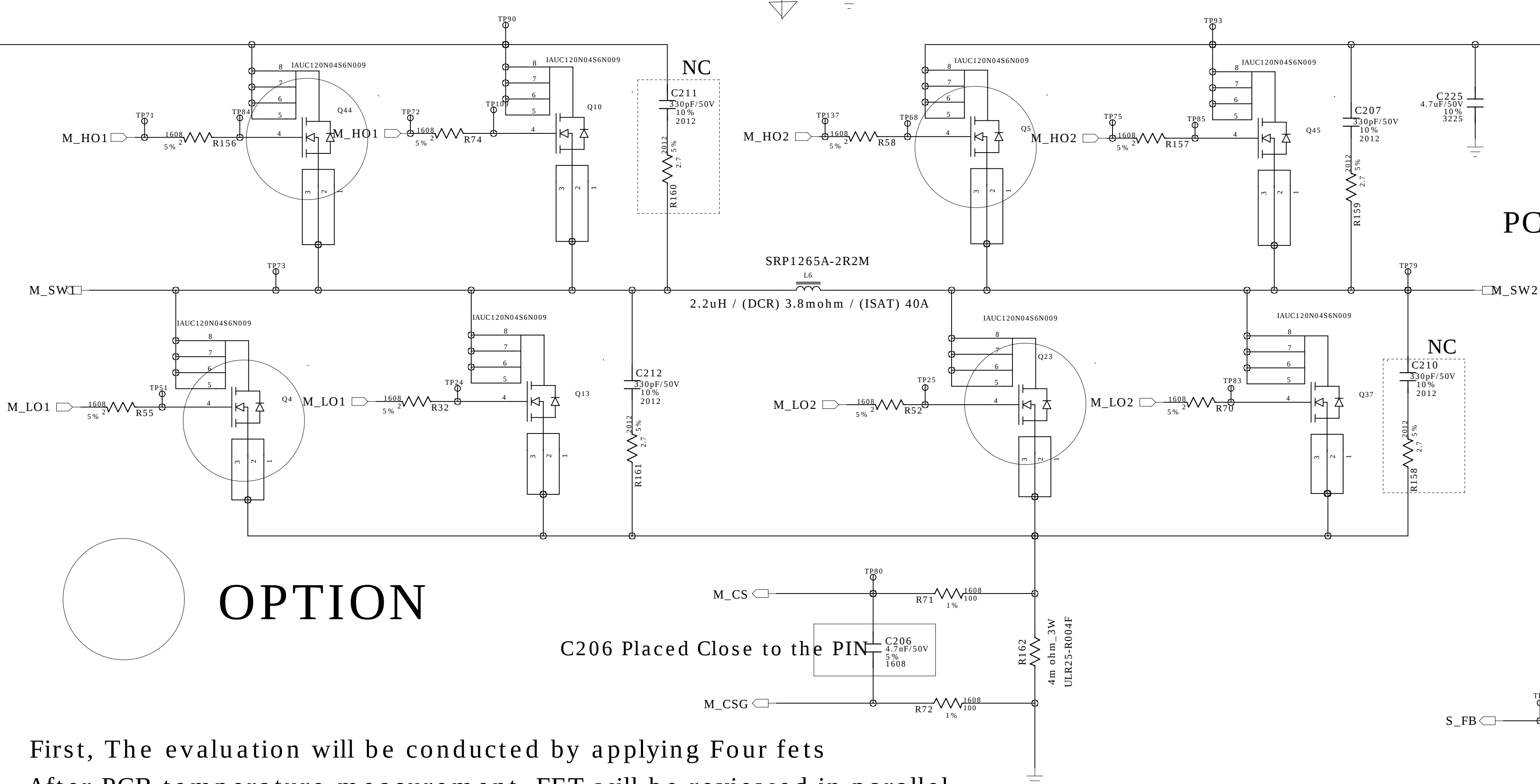
- VIN : 8~16V (Charging starts from 10V)
- FSW : 300KHZ (Master / Slave)
- 2Phase Max Charging Current Limit 33A : 16.5A Per 1Phase
- Charging Voltage : 12.6V
- LM5176 2EA Applications : Master 1EA / Slave 1EA
- CC (Constant Current) Variable Control
- NC : (NOT Connect) Debugging point



Master Control_ 12.6V / 16.5A

CHARGE_PCB1(NTC_10K)
TH2
10K NTC RES
BGND L6 Inductor Near

Master Load_ 12.6V / 16.5A (20A Pattern width)



PCB Artwork will be performed symmetrically for each phase

Max Current Limit = 16.5A

☐ OPTION

First, The evaluation will be conducted by applying Four fet
After PCB temperature measurement, FET will be reviewed in parallel
However, FETs (8EA) will be left in the PCB space

Slave Control_12.6V / 16.5A

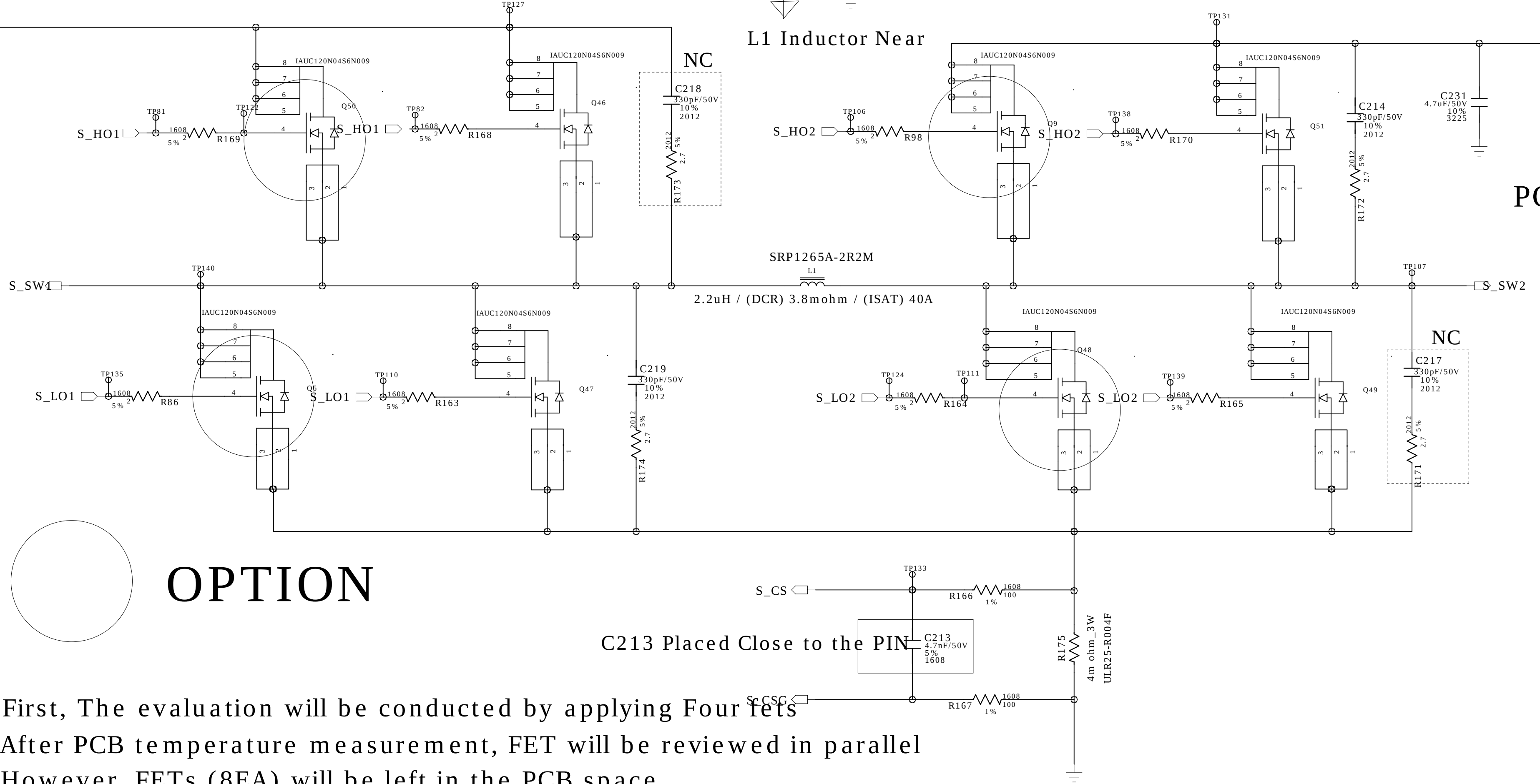
5A

CHARGE_PCB2(NTC_10K)

TH4
10K NTC RES

BGND

Master Load_ 12.6V / 16.5A (20A Pattern width)

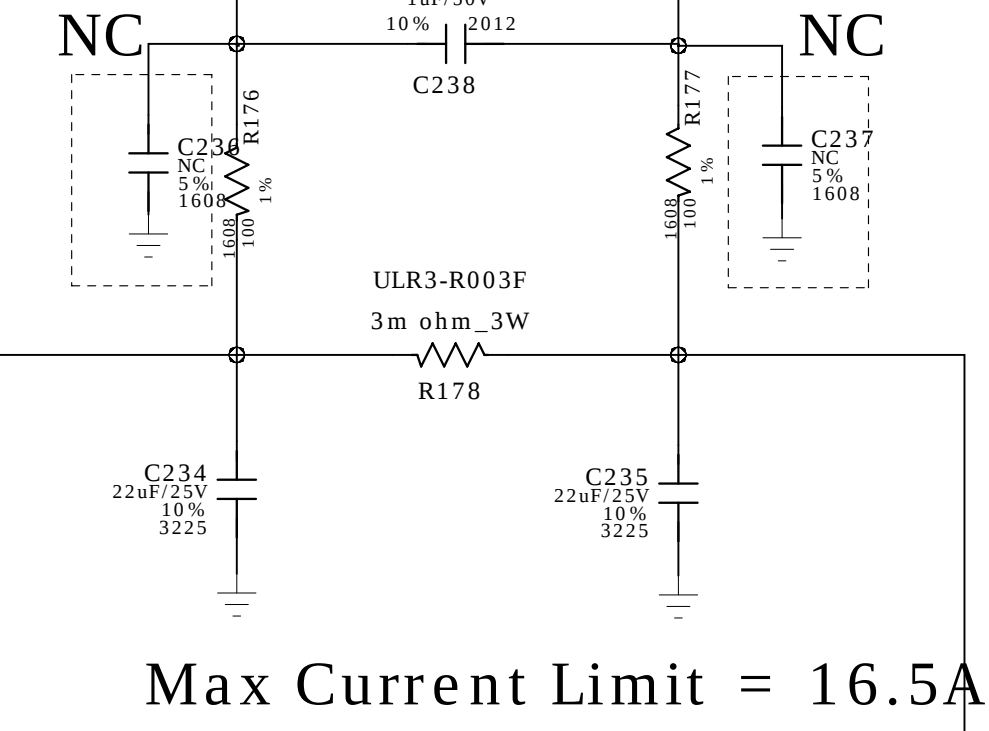


PCB Artwork will be performed symmetrically for each phase

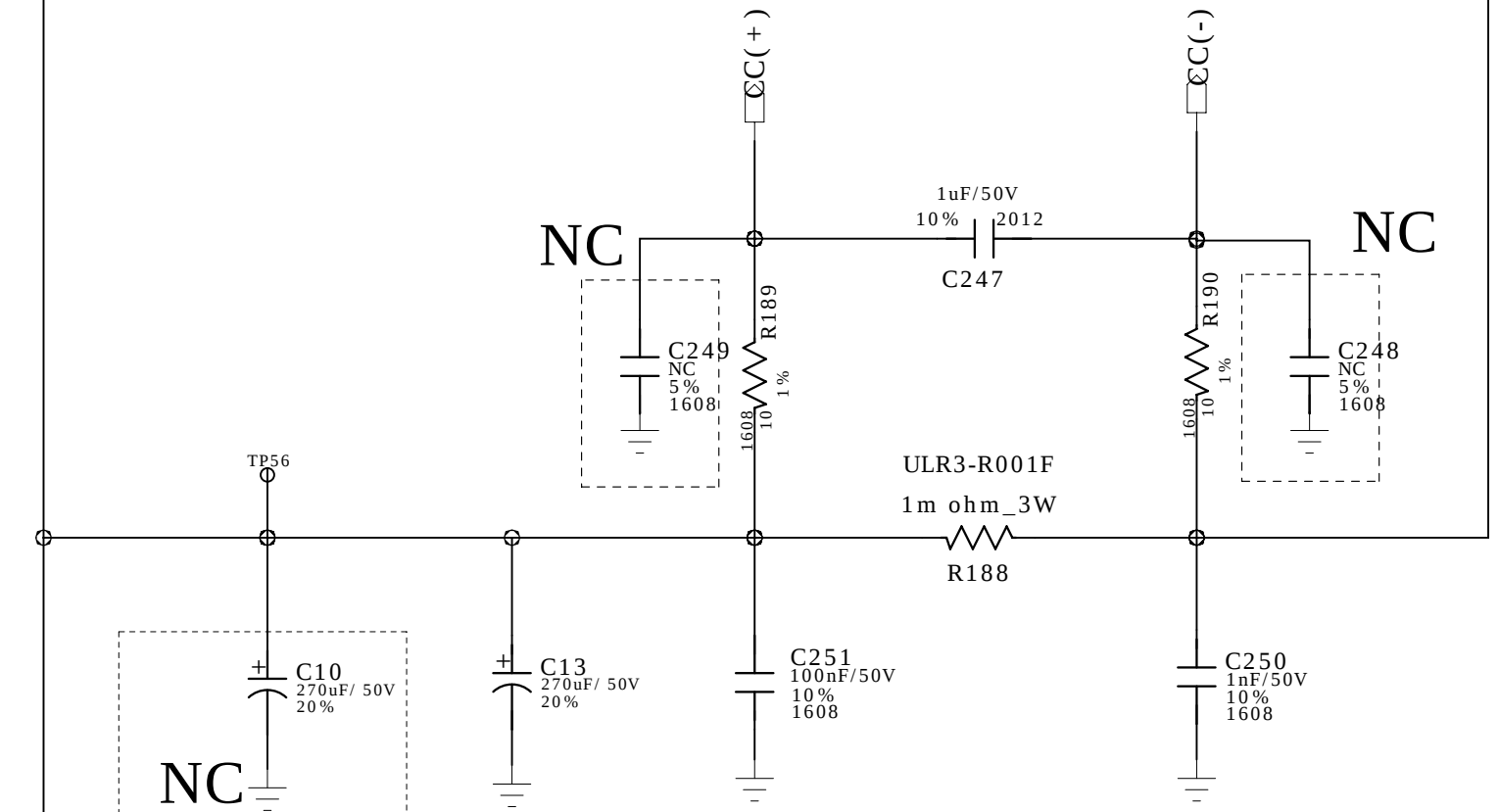
Max Current Limit = 16.5A
each phase

OPTION

First, The evaluation will be conducted by applying Four tests
After PCB temperature measurement, FET will be reviewed in parallel
However, FETs (8EA) will be left in the PCB space



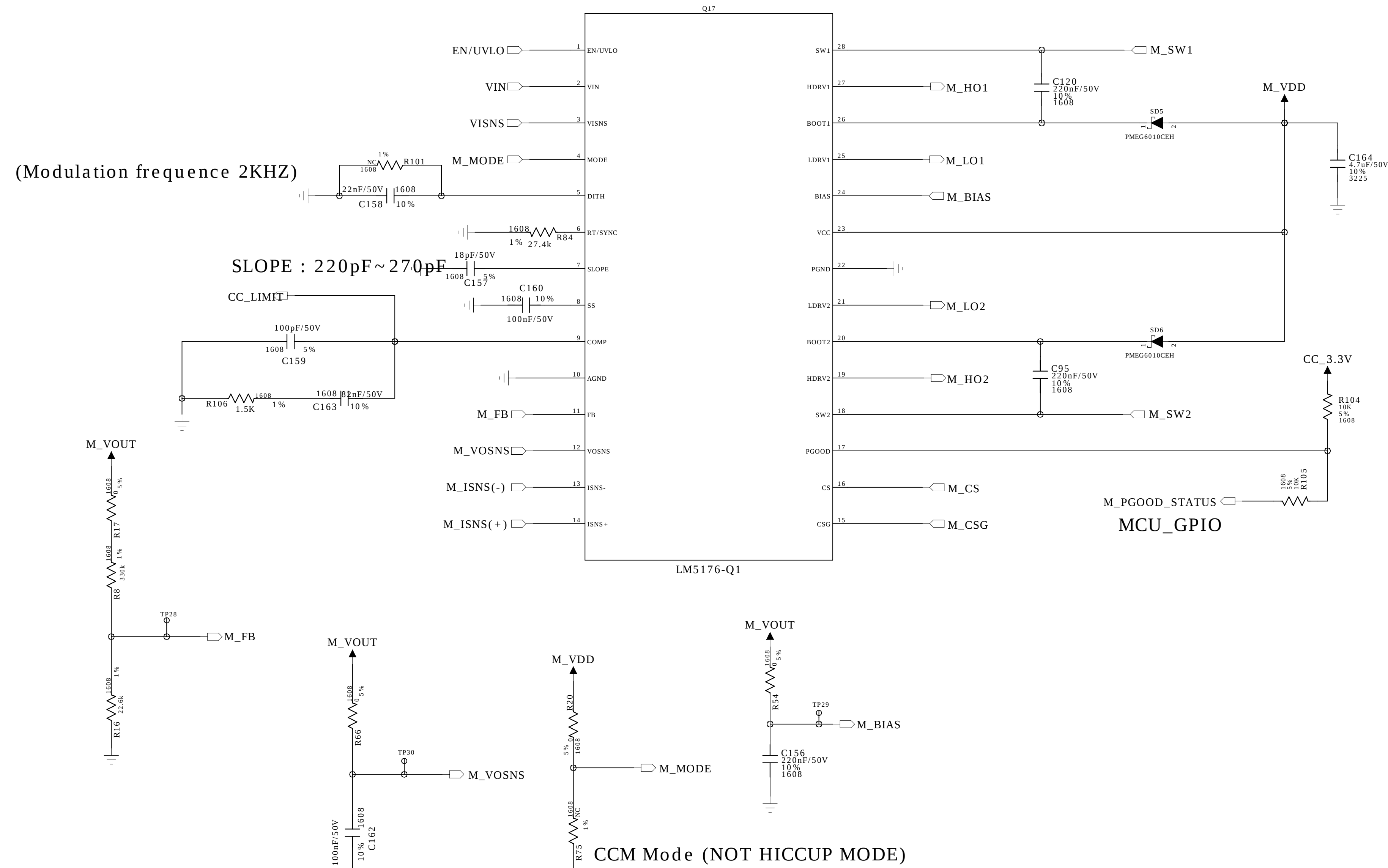
CC (Constant Current Variable Control)



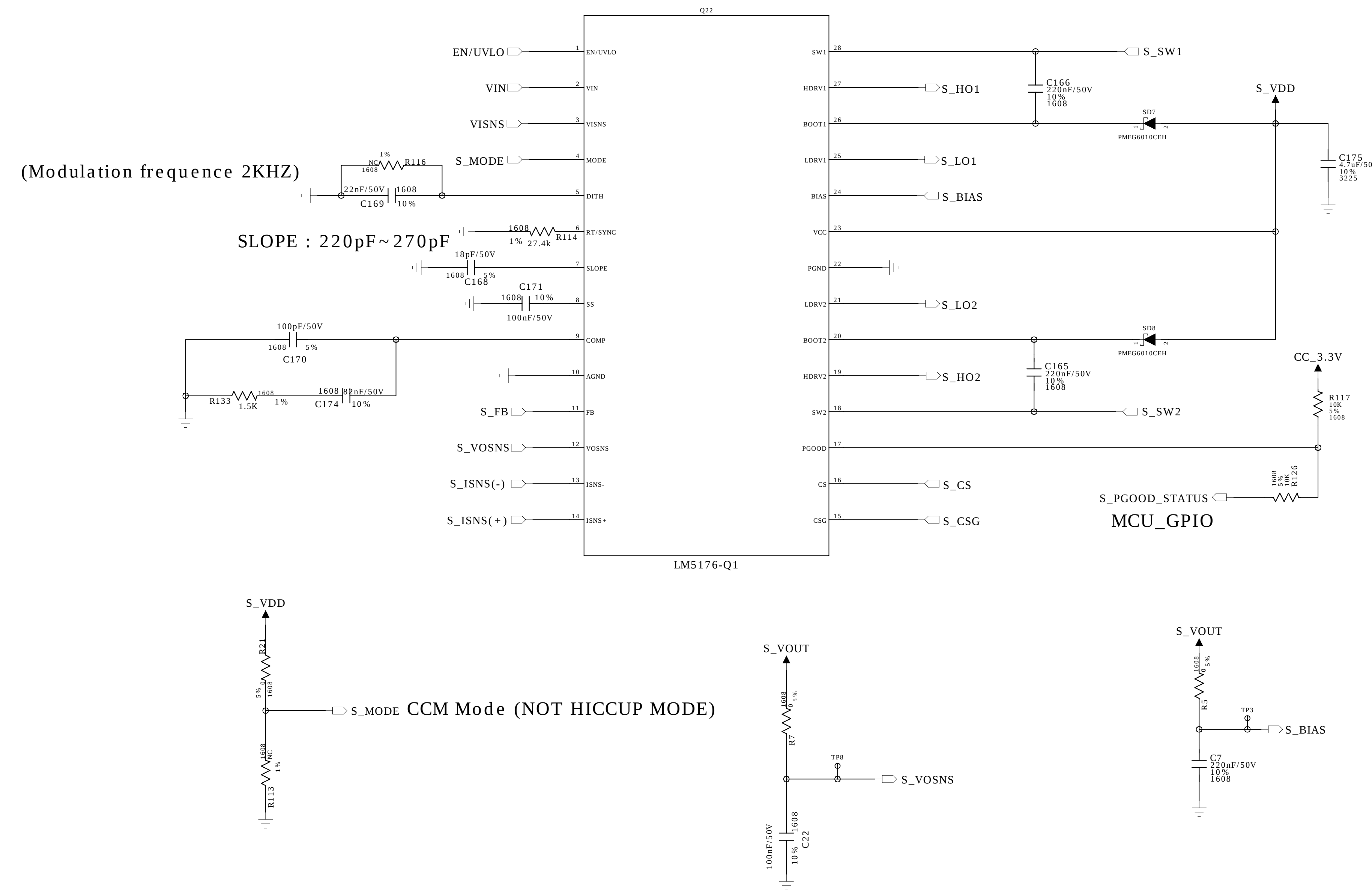
Total Current Limit 33A (12.6V) : 35A Pattern width

		COMPANY:			
		TITLE:		BMS	
DRAWN:	JH CHO	DATED:	18.02.28		
CHECKED:	JH CHO	DATED:	18.06.18		
		CODE:	<Code>	DRAWING NO:	REVISION
		SIZE:	E	2.00	
RELEASED:	<Released By>	DATED:	<QC Date>		
		ISSUED:	<Scale>	SHEET: 2 of 3	

MASTER # 1 LM5176



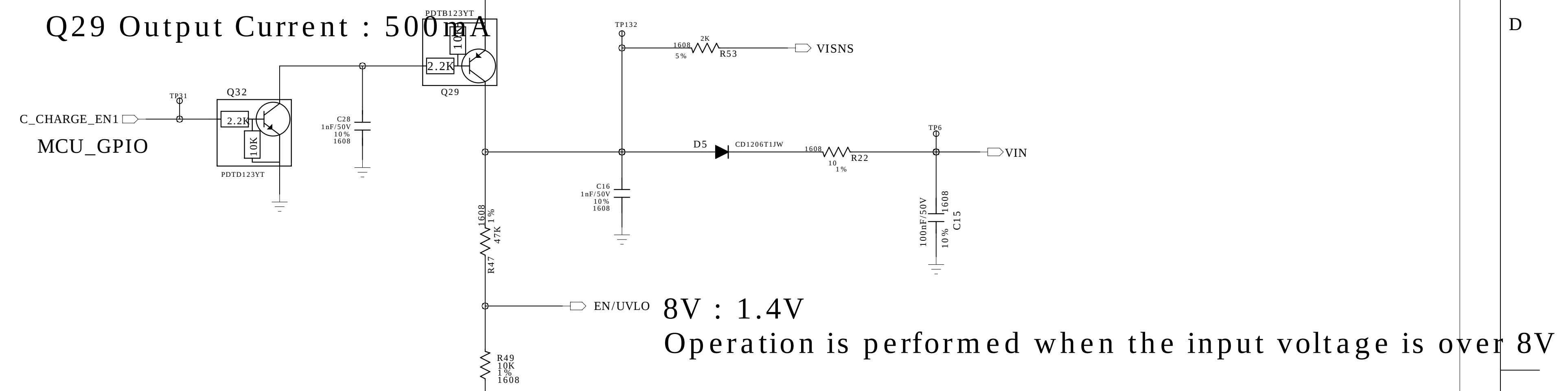
SLAVE # 2 LM5176



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Power Supply of Master and Slave

B+_PWR : LM5176 Input Volatage (B+_PWR is supplied continuou
Changed to collector Pin to minimize leakage current

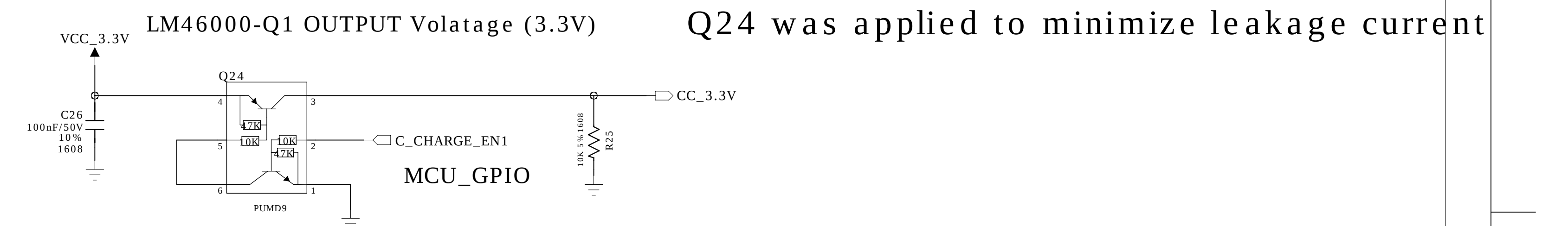


EN/UVLO	VCC	DEVICE MODE
$EN/UVLO < V_{EN(STBY)}$	—	Shutdown: VCC off, No switching
$V_{EN(STBY)} < EN/UVLO < V_{EN(OP)}$	—	Standby: VCC on, No switching
$EN/UVLO > V_{EN(OP)}$	$VCC < V_{UVLO(VCC)}$	Standby: VCC on, No switching
$EN/UVLO > V_{EN(OP)}$	$VCC > V_{UVLO(VCC)}$	Operating: VCC on, Switching enabled

CC (Constant Current) Variable Control

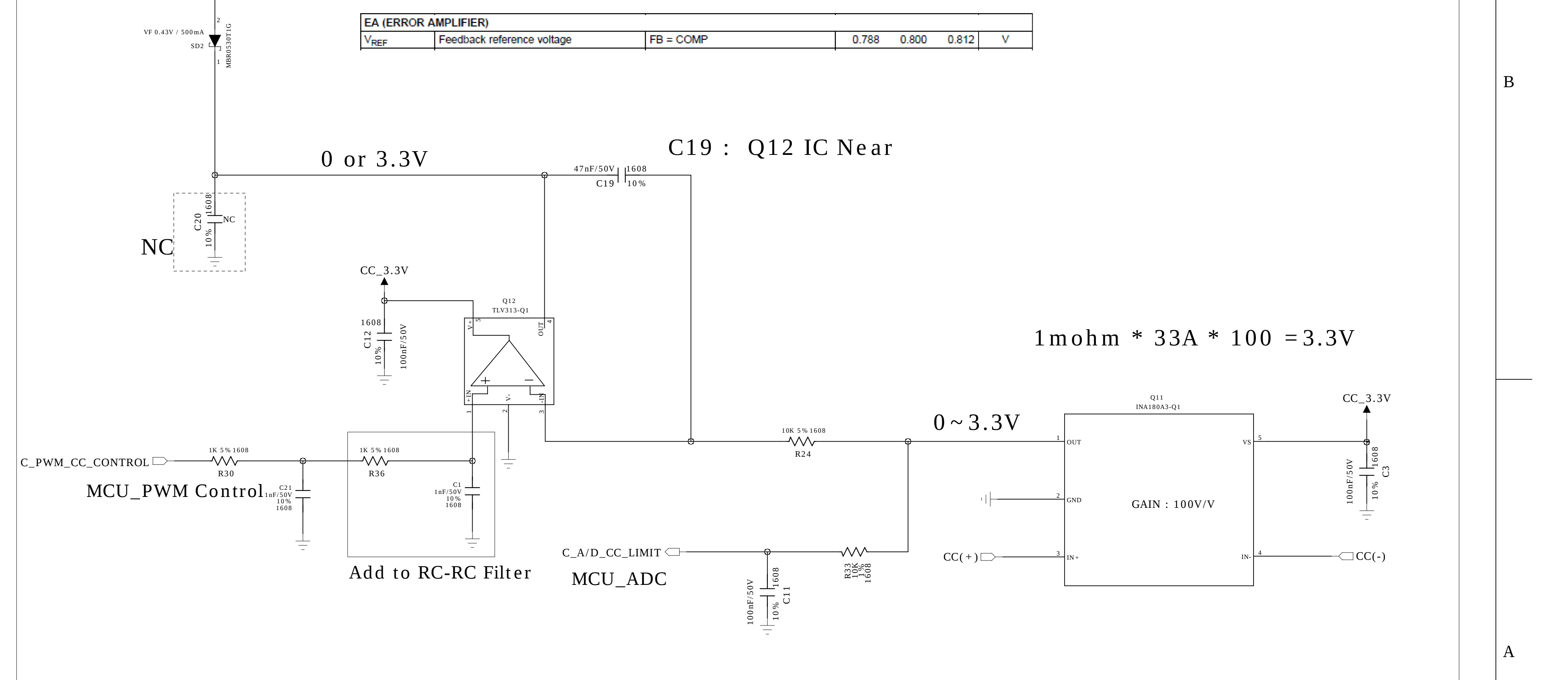
(3.3V Power is supplied continuously)

Q24 was applied to minimize leakage current



Charging end less than 0.788V (Comp pin Of Master) : Slave auto shutdown when Master off (M_VOUT Power Off of Q2 V	
Only connected to the master comp pin	

EA (ERROR AMPLIFIER)						
V _{REF}	Feedback reference voltage	FB = COMP	0.788	0.800	0.812	V



		COMPANY:				
		TITLE:				
		BMS				
DRAWN:	JH CHO	DATED:	18.02.28			
CHECKED:	JH CHO	DATED:	12.06.18	CODE:	SIZE:	DRAWING NO:
QUALITY CONTROL:	<QC Day>	DATED:	<Code>	E	REVISION	
RELEASED:	<Released By>	DATED:	<Release Date>	2.00		REV:
		SALES:		SHEET: 3 of 3		