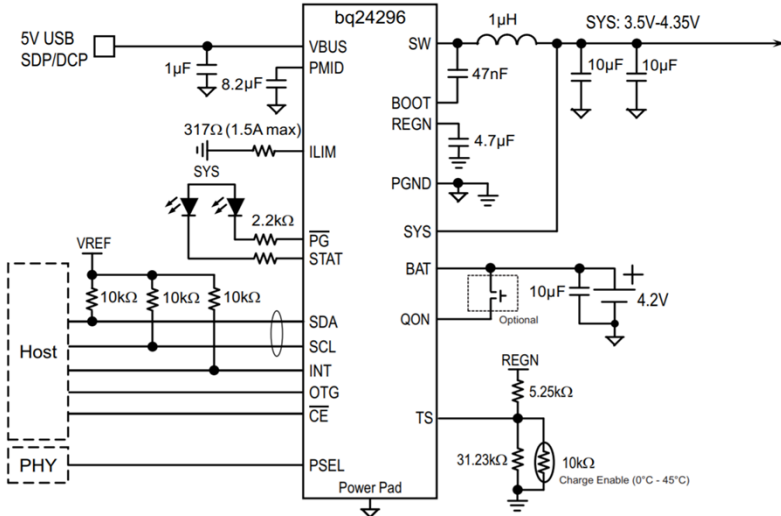
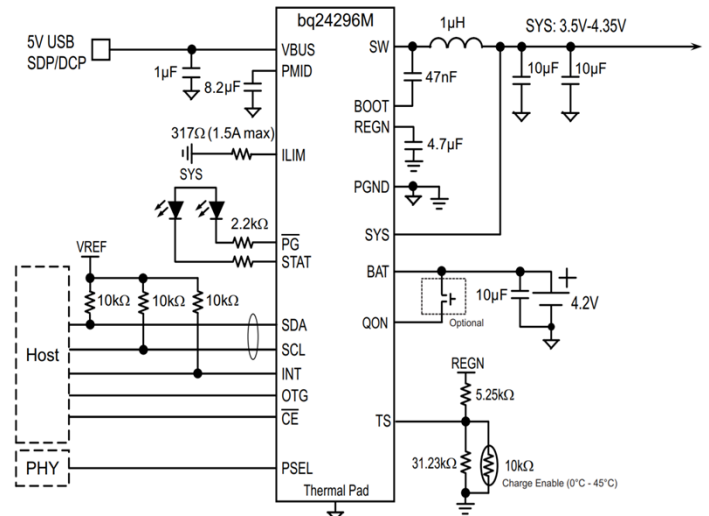


BQ24296/BQ24296M/BQ24259 TYPICAL SCHEMATIC



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BQ24296/BQ24296M/BQ24259 SCHEMATIC CHECKLIST

PIN NAME	REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS	
PSEL	2	Optional				Power source selection input.	High indicates a USB host source and Low indicates an adapter source. Do not float.	
/PG	3	Optional	PG resistor	2.2 kΩ	10 kΩ	Open drain active low power good indicator.	LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.	
STAT	4	Optional	STAT resistor	2.2 kΩ	10 kΩ	Open drain charge status output	1. If not used, leave it float. 2. HIGH indicates charge complete or charge disabled. When any fault Digital condition occurs, STAT pin in blinks at 1 Hz.	
SCL/SDA	5-6	Optional	SCL resistor	10 kΩ		I2C Interface clock and data	If I2C communication is not used, leave it float.	
		Optional	SDA resistor	10 kΩ		Open-drain Interrupt Output	If I2C communication is not used, leave it float.	
INT	7	Optional	INT resistor	10 kΩ		Active high enable pin during boost mode.	1. If not used, leave it float. 2. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.	
OTG	8	Optional				Active low Charge Enable pin.	1. If OTG boost mode is not used, short it to ground. 2. In buck mode with USB host (PSEL=High), when OTG = High, IIN limit = 500 mA and when OTG = Low, IIN Digital limit = 100 mA. 3. The boost mode is activated when the REG01[5:4] = 10 and OTG pin is High.	
/CE	9	Required				Input current limit input.	1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[5:4] = 01 and CE pin = Low.	
ILIM	10	Required	ILIM resistor		* Ω	Temperature qualification voltage inputs.	1. The actual input current limit is the lower one set by ILIM and by I2C REG00[2:0]. 2. The minimum input current programmed on ILIM pin is 500 mA. 3. If ILIM pin is short, the input current limit is set by the register. 4. If ILIM pin is open, the input current is limited to zero	
TS	11	Required	TS resistor and thermistor			BATFET enable control in shipping mode	1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. 3. Charge suspends or Boost disable when TS pin is out of range. 4. A 103AT 2 thermistor is recommended.	
QON	12	Optional			Switch	Input source to the charger	A logic low to high transition on this pin with minimum 2-ms high level turns on BATFET to exit shipping mode. It has internal 1-MΩ (Typ) pull down. For backward compatibility, when BATFET enable control function is not used, the pin can be no connect or tied to TS pin (10-kΩ NTC thermister only).	
VBUS	1,24	Required	VBUS caps	1µF		Actual input source to the charger	1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10µF capacitance at VBUS & PMID for USB input compliance.	
PMID	23	Required	PMID caps	6.8µF		Positive battery connection point	Given the total input capacitance, connect a 1-µF capacitor on VBUS to PGND, and the recommended 8.2 µF or more on PMID to PGND	
VBAT	13-14	Required	VBAT caps	10µF	10µF	System connection point.	1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.	
VSYS	15-16	Required	VSYS caps	20µF	20µF	40µF	Switching node connecting to output inductor.	Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.
SW	19-20	Required	Output inductor	1µH		2.2µH	PWM high side driver positive supply.	The charger device has internal loop compensator. To get good loop stability, the resonant frequency of the output inductor and output capacitor should be designed between 15 kHz and 36 kHz.
		Optional	SW Resistor			* Ω	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.	
		Optional	SW Cap			* F		
BTST	21	Required	BTST-SW cap	0.047µF	0.047µF	0.047µF	PWM low side driver positive supply output.	Connect the 0.047µF bootstrap capacitor from SW to BTST.
		Optional	BTST resistor			* Ω	Help with EMI performance. Recommend unpopulated footprint on new designs.	
REGN	22	Required	REGN cap	4.7µF	4.7µF	4.7µF	Power ground connection for high-current power converter node.	PWM low side driver positive supply output. Internally, REGN is connected to the cathode of the bootstrap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of TS pin.
PGND	17-18	Required					On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power PGND and the analog GND near the IC PGND pin.	
PowerPAD		Required					Always solder PowerPAD Pad to the board, and have vias on the PowerPAD plane star-connecting to PGND and ground plane for high-current power converter.	