RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
1		PCB layer stackup	Thermal, efficiency, signal integrity	Multi-layer PCB is suggested. Allocate at least one ground layer. The BQ24800EVM and BQ24780SEVM uses a 4-layer PCB (top layer, power ground layer, signal layer and bottom layer).
2	CBUS, Q4 (Buck high side), Q5 (buck low side)	Input Loop	High frequency noise, ripple	Input capacitors, Q4, Q5 forms the input loop of a buck converter. It is best to put them on the same side. Connect them with large copper to reduce the parasitic resistance. Move part of CBUS to the other side of PCB for high density design.
3	Q1 (ACFET), Q2 (RBFET), RAC, Q4 (Buck high side), L1 (power stage inductor)	Current path	Efficiency	The current path from input to battery would need to be optimized for efficiency. Wider trace width reduces copper loss. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2A/via for a 10-mil via with 1 oz. copper thickness.
4	RSR, Q3 (BATFET)	Current path	Efficiency, battery voltage detection	Place Q3 and RSR near the battery terminal. The current path from battery to output would need to be optimized for efficiency. Wider trace width reduces copper loss. Pay attention to via resistance if they are not on the same side. The device detects the battery voltage through SRN near battery terminal.
5	Q4 (Buck high side), Q5 (buck low side), L1 (power stage inductor)	Power stage	Thermal, efficiency	Place Q4, Q5, L1 next to each other. Allow enough copper area for thermal dissipation. The copper area is suggested to be 2x to 4x of the pad size. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
6	RAC, RSR	Current sense	Regulation accuracy	Use Kelvin-sensing technique for RAC and RSR current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs.

7	Small capacitors	IC bypass caps	Noise, jittering, ripple	Place VCC cap, REGN caps, and other filtering caps near IC.
8		Ground partition	Measurement accuracy, regulation accuracy, jitters, ripple	Separate analog ground(GND on EVM) and power ground(PGND on EVM) is preferred. PGND should be used for all power stage related ground net. GND should be used for all sensing networks. Some example of sensing networks include ACP, ACN, SRP, SRN, ILIM, etc. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad. Connect analog ground and power ground together using power pad as the single ground connection point.

Sample Layout