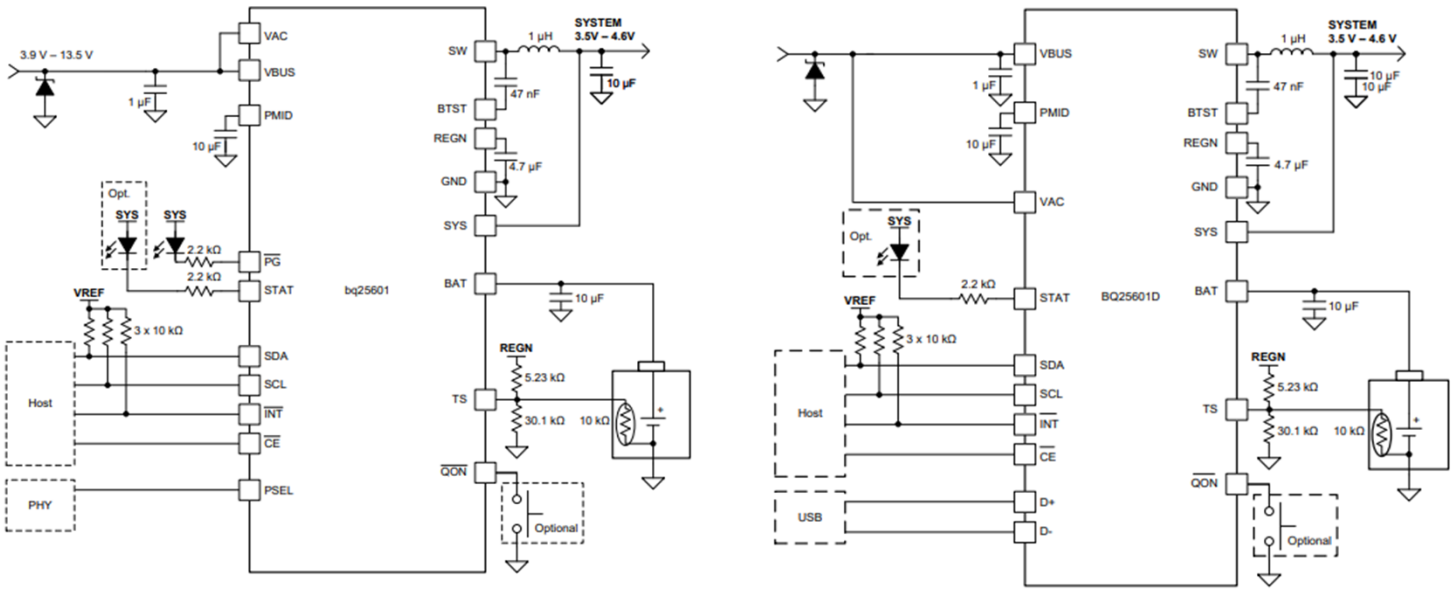
BQ25601/D TYPICAL SCHEMATIC



BQ25601/D SCHMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							USB data line pair	
D+/D- BQ25601D ONLY	2,3	Optional					Positive line of the USB data line pair.	1. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
		Optional					Negative line of the USB data line pair.	
							Power source selection input.	
PSEL BQ25601 ONLY	2	Required						Set 500 mA input current limit by pulling this pin high and set 2.4A input current limit by pulling this pin low. Once the device gets into host mode, the host can program different input current limits to IINDPM register. Do not float.
							Open drain active low power good indicator.	
/PG BQ25601 ONLY	3	Optional	PG resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 10-kΩ resistor.	LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
							Open drain charge status output	
STAT	4	Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it float. 2. The STAT pin indicates charger status. Collect a current limit resister and a LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses 4.This pin can be disabled via EN_ICHG_MON[1:0] register bits.
							I2C Interface clock and data	
SCL/SDA	5-6	Optional	SCL resistor		10 kΩ		Connect SCL to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it float.
		Optional	SDA resistor		10 kΩ		Connect SDA to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it float.
							Open-drain Interrupt Output	
INT	7	Optional	INT resistor		10 kΩ		Connect the INT to a logic rail via 10-kΩ resistor.	1. If not used, leave it float. 2. The INT pin sends active low, 256-µs pulse to host to report charger device status and fault.
							No connect	
NC	8, 10	Optional						Keep the pins float
							Active low Charge Enable pin	
/CE	9	Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[4] = 1 and CE pin = Low.
							Temperature qualification voltage inputs for JEITA	
TS	11	Required	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	 1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
							BATFET enable/reset control input	
/QON	12	Optional			Switch			1.If not used, leave it float. 2.The pin contains an internal pull-up to maintain default high logic. 3.When BATFET is in ship mode, a logic low of tSHIPMODE duration turns on BATFET to exit shipping mode. When VBUS is not pluggeD–in, a logic low of tQON_RST (minimum 8 s) duration resets SYS (system power) by turning BATFET off for tBATFET_RST (minimum 250 ms) and then re-enable BATFET to provide full system power reset.
							Charge input voltage sense	
VAC	1	Required						Charge input voltage sense. This pin must be connected to VBUS pin.
							Charge input voltage	
VBUS	24	Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
							Actual input source to the charger	
PMID	23	Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
							Positive battery connection point	
BAT	13-14	Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.
							Converter output connection point	
SYS	15-16	Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R.
							Switching node connecting to output inductor	
SW	19-20	Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
							PWM high side driver positive supply.	
BTST	21	Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor snubbing resistor	Help with EMI performance. Recommend unpopulated footprint on new designs.

REGN	22						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10 Vrating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of the TS pin.
GND	17-18						**Power ground**	
		Required						On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.
Thermal PAD		Required						Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.