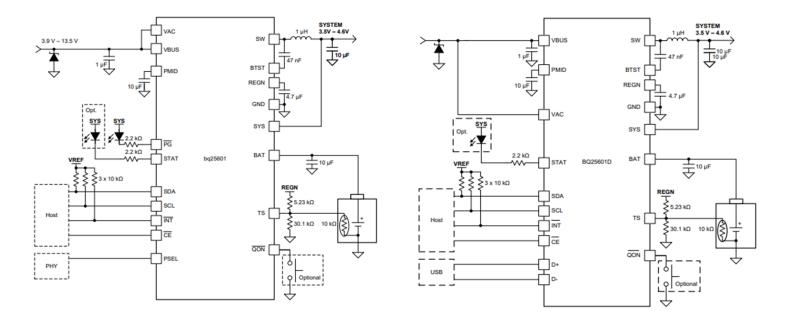
BQ25601/D TYPICAL SCHEMATIC



SCLYSDA 5-6 Optional SCL resistor 10 kD Connect SCL to the logic rall through a 10-kDr cresistor. 10 kD Connect SOL to the logic rall through a 10-kDr cresistor. 10 kD Connect SOL to the logic rall through a 10-kDr cresistor. 10 kD Optional INT resistor No connect SOL to the logic rall through a 10-kDr resistor. No connect SOL to the logic rall through a 10-kDr resistor. No connect SOL to the logic rall through a 10-kDr resistor. Int resistor No connect the INT to a logic rall via 10-kDr resistor. No connect the INT to a logic rall via 10-kDr resistor. No connect the INT to a logic rall via 10-kDr resistor. No connect the INT to a logic rall via 10-kDr resistor. No connect the INT to a logic rall via 10-kDr resistor. Active low Charge fenable pin 1. (/EE pin must be pulled High or Low. 2. Battery charging is enabled when REGO1[4] = 1 and CE pin = Low. Temperature qualification voltage inputs for JETA Temperature qualification voltage inputs for JETA Connect a negative temperature coefficient thermistors. Recommend J03AT2 thermistors. 1. If thermistor is not used, sear 15 pin voltage within normal range 2. If thermistor is used, program temperature window with a resistor divider from REGN to Ts to GND. Charge suspends when Ts pin is out of range. BATET enable/reset control input Int used, leave it float. 2. The pin contains an internal pull-up to maintain default high logic 3. When BATET is nable provided. In later the internal pull-up to maintain default high logic 3. When BATET is nable provided. In later the internal pull-up to maintain default high logic 3. When BATET is nable provided. In later the internal pull-up to maintain default high logic 3. When BATET is not used, leave it float. 2. The pin contains an internal pull-up to maintain default high logic 3. When	BQ25601/D SCHMATIC CHECKLIST								
Device Devices 2.5 Concept 2.5 Concept	PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX		COMMENTS AND RELEVANT EQUATIONS
POLICE ON 19 Secured 1 S								USB data line pair	
Processor Section Processor		2,3						·	
RPSIL PROJECT CHAVY 2 REQUERED 3 PROJECT CHAVY 4 PROJECT CHAVY 4 PROJECT CHAVY 4 PROJECT CHAVY 5 PROJ			Optional						
## Required ## Disparation Control the other passes are the first the pulse growth register control to pulse the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the pulse of the pulse growth register (PE) and the	PSFI							Power source selection input.	Set 500 mA input current limit by nulling this nin high and set 2.44 input current limit
STAT Optional PG resister 2 2 4 to 30 to Connect to the pollular parisks 10 to 10 to Connect to the pollular parisks 10 to 10 to Connect to the pollular parisks 10 to 10 to Connect to the pollular parisks 10 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to Connect to the pollular parisks 20 to 10 to 10 to Connect to 10 to Co		2	Required						by pulling this pin low. Once the device gets into host mode, the host can program different input current
Open date the expectation original processes that the original processes are also as a control processes and the processes are also as a control processes and the processes are also as a control processes and the processes are also as a control processes		3	Optional	PG resistor		2.2 kΩ	10 kΩ		
STAT 4								Open drain charge status output	
SCL/SPA 5-6 Optional SA resistor 10 kg 10 Optional SA resistor 11 Required SA resistors and feature 12 Required SA resistors and feature 13 kg 11 Optional SA resistors and feature 13 kg 11 Required SA resistors and feature 13 kg 11 Required SA resistors and feature 14 kg 11 kg	STAT	4	Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-k Ω or 10-k Ω resistor.	from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses 4.This pin can be disabled via EN_ICHG_MON[1:0]
Optional SOA relation 10 No. Connect State to the logic and through a 10-14 relation. FIZC communication is not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger device state and float. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger floate. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger floate. Immediately leave it is not to report charger floate. If not used, leave it float. 2. The IMT pin sends active low, 256 µs pute to host to report charger it is not pute to the pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends active low. 2. If not used, leave it float. 2. The IMT pin sends								I2C Interface clock and data	
Optional NT resistor 10 kg/ call via 10-k1 resistor 20 kg/ call via 10-k1 resistor 5 kg/	SCL/SDA	5-6							
NT 2 Optional NT resistor NC 8.10 NC 8.10 Optional Ts resistor NC 8.10 Optional Ts resistor NC 8.10 Optional NC NC 8.10 Active flow Charge fashes pin I./CE pin must be pulled High or Low 2. Battery charging is enabled when REGO[4] = 1 and CE pin = Low. Temperature qualification voltage inputs for JRTTA Temperature qualification voltage inputs for JRTTA Accommend JOAT 2 thermistors. BATTET enable/reset control input If flow used, leave it flow 2. The pin contains an internal pull-upp to minitian default high logs. A When SATTET is in high more, a rigid low of 100, MET finalments 9 duration reserved by the minitian default high logs. A When SATTET is in high more, a rigid low of 100, MET finalments 9 duration reserved by power feature. See Supplements When SATTET is in high more, a rigid low of 100, MET finalments 9 duration reserved by power feature. See Supplements When SATTET is in high more, a rigid low of 100, MET finalments 9 duration reserved by the sattle providings seense Charge input voltage seense Actual input source to the charger PMID 23 Required PMID caps 8.20			Optional	SDA resistor		10 kΩ			If I2C communication is not used, leave it float.
NCC 8, 3.0 Optional NF resistor 10 kB No connect Herit to a logic rail was 15-kB resistors. No connect a more department of the control imput 1.7CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Temperature qualification voltage imputs for JETIA 1.1CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Temperature qualification voltage imputs for JETIA 1.1CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Connect a negative temperature working in puts for JETIA 1.1CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Connect a negative temperature working in puts for JETIA 1.1CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Connect a negative temperature working in puts for JETIA 1.1CE pin must be pulled High or Low. 2. Battery charging is enabled when REGOI(s) = 1 and CE pin = Low. Connect a negative temperature working in puts for JETIA 1.1CE pin must be contains an internal pull-up to maintain default high logic. 3. When BATTET to exist piping mode. When VBUST is not pulgage. 1 and pick or ITCD, ITC pinimisms of jud and created things in pull-up to maintain default high logic. 3. When VBUST is not pulgage. 1 and pick or ITCD, ITC pinimisms of jud and created the VBUST pinimisms of jud and created the VBUST pinimisms. 2 and pink or reside SATTET to provide full system pulgage. 1 and pink or reside ASTTET to provide full system pulgage sense. This pin must be connected to VBUS pin. VBUS 24 Required VBUS caps 1 uf Charge input voltage sense. This pin must be connected to VBUS pin. Charge input voltage sense. This pin must be connected to VBUS pin. Pinimisms of jud and pink or its an internal band residence provided to the data of the SETIA or SATM pinimisms of jud and their residence provided to the data of the SETIA or SATM pinimisms of	INT	-						Open-drain Interrupt Output	4. If you have delicated 2. The INT sign and a self-relative law 2500 was the Asia based a growth because decides
Active four charge finable pin Temperature qualification voltage inputs for JETA Temperature qualification voltage inputs for JETA Temperature qualification voltage inputs for JETA Connect a negative temperature coefficient thermistors. BATTET enable/reset control input BATTET enable/reset control input Active four control input BATTET enable/reset control input Active four control input BATTET enable/reset control input Charge input voltage sense Charge input voltage sense Charge input voltage sense. This pin must be connected to VBUS pin. Charge input voltage sense. This pin must be connected to VBUS pin. Actival input source to the charger PMID Actival input source to the charger Positive battery connection point Switch input voltage sense. Converter output connection point Switch input source to the charger Positive battery connection point Switch input source to the charger Positive battery connection point Switch input source to the charger Actival input source to the charger Positive battery connection point Switch input source to the charger Actival input source to the charger Converter output connection point Switch input source to the charger Converter output connection point Switch input source to the charger Converter output connection point Switching node connecting to output inductor Switching node connecting to output inductor Switching node connecting to output inductor Positive battery connection point to the positive terminal of the battery pack. The internal BATFET not carmic capacitor from VBUs to PGMD and place it as close as possible to C. 2. It is recommended to be the versus blocking MOSFET (BBFET) and the derian of HSFET. Put 10 µF ceramic capacitor in PMD to SMD. Converter output connection point Switching node connecting to output inductor Switching node connecting to output inductor Switching node connecting to output inductor Possitive battery co	INT	7	Optional	INT resistor		10 kΩ		-	
Active low Charge Enable pin Competition of Sequence Sequence	NC	8, 10	0.11					No connect	Vacable wire fleet
Temperature qualification voltage inputs for JETA 11 Required Ts resistors and themistor in themistors. Connect a negative temperature coefficient themistors. Connect a negative temperature coefficient themistors. Accommend J03AT-2 themistors. Lifthornistor is not used, set Ts pin voltage within normal range. 2. If themistor is used, program temperature window with a resistor divider from REGN to Ts to GND. Charge suspends when Ts pin is out of range. Actual reput voltage sense Charge input voltage sense Charge input voltage sense Actual reput source to the charger PMID 23 Required PMID caps 8.2 pf 10 pf PMID caps 8.2 pf 10 pf Required STS Caps 10 pf Converter output connection point Converter output connection point Switching node connecting to output industors Switching node connecting of output industors Switching node connecting for output connection point Switching node connecting to output industors Switching node connecting of output industors Switching node connec			Optional					Active law Charge Enghle win	keep the pins float
To respect ture qualification voltage inputs for JETA In Required To resistors and thermistor To resistors and thermistor To resistors and thermistor Connect a negative temperature coefficient thermistors. BATECT enable/reset control input BATECT enable/reset control input BATECT enable/reset control input If not used, leave it float. 2 The prin contains an internal pull-up to maintain default high logic 3. When early ange. BATECT enable/reset control input If not used, leave it float. 2 The prin contains an internal pull-up to maintain default high logic 3. When early ange. Charge input voltage sense. Charge input voltage sense. Charge input voltage sense. Charge input voltage sense. This pin must be connected to VBUS pin. Charge input voltage sense. PMID 23 Required VBUS caps 1uf Charge input voltage Actual input source to the charger Connected to the drain of the reverse blocking MOSET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND. Positive battery connection point Settley connected to be the positive terminal of the battery pack. The internal BATECT and current terming when battery is not connected. SYS caps 10uf Converter output connection point Connected to upput inductor. The charger device has internal logo compensator. Switching node connecting to output inductor Switching node connecting to output inductor. Switching node output. Connected to output inductor. The charger device has inter	/CF	9						Active low charge chable pin	
TS 11 Required Ts resistors and thermistor Connect a negative temperature coefficient thermistors. Connect a negative temperature coefficient thermistors.	762	Ĵ	Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[4] = 1 and CE pin = Low.
Recommend 103AT-2 thermistors. Recommend 103AT-2 thermistors.								Temperature qualification voltage inputs for JEITA	DECN REON
Actual input voltage sense Charge input voltage Charge input voltage sense Charge input voltage sense Charge input voltage sense Charge input voltag	TS	11	Required						temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of
Actual input voltage sense Charge input voltage Charge input voltage sense Charge input voltage sense Charge input voltage sense Charge input voltag								BATFET enable/reset control input	
VBUS 24 Required VBUS caps 1uF Charge input voltage 1. Place a 1-μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10μF capacitance at VBUS & PMID for USB input compliance. Actual input source to the charger Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 μF ceramic capacitor on PMID to GND. Positive battery connection point Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 μF closely to the BAT pin. 2. Charger may operal normally when battery is not connected. Connect a 20 μF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or XSR. Switching node connecting to output inductor SW Resistor SW Cap SW Cap * F SW Caps SW Cap SW Caps SW Cap SW Caps SW Cap SW Cap SW Caps SW Cap SW Caps SW Cap SW Ca	/QON	12	Optional			Switch			BATFET is in ship mode, a logic low of tSHIPMODE duration turns on BATFET to exit shipping mode. When VBUS is not pluggeD-in, a logic low of tQON_RST (minimum 8 s) duration resets SYS (system power) by turning BATFET off for tBATFET_RST (minimum 250 ms) and then re-enable BATFET to provide full system
VBUS 24 Required VBUS caps 1uF Charge input voltage 1. Place a 1-μF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10μF capacitance at VBUS & PMID for USB input compliance. Actual input source to the charger Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 μF ceramic capacitor on PMID to GND. Positive battery connection point Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 μF closely to the BAT pin. 2. Charger may operal normally when battery is not connected. Connect a 20 μF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or XSR. Switching node connecting to output inductor SW Resistor SW Cap SW Cap * F SW Caps SW Cap SW Caps SW Cap SW Caps SW Cap SW Cap SW Caps SW Cap SW Caps SW Cap SW Ca								Charge input voltage sense	
Charge input voltage Page	VAC	1	Required						Charge input voltage sense. This nin must be connected to VRUS nin
VBUS 24 Required VBUS caps 1uf			240					Charge input voltage	and ge input votage sense. This primitist be connected to 1905 prim
Actual input source to the charger PMID 23 Required PMID Caps 8.2 uf 10 uf	VBUS	24	Required	VBUS caps	1uF				
BAT 13-14 Required BAT caps 10uF 10uF 20uF 20uF 20uF 20uF 20uF 20uF 20uF 2								Actual input source to the charger	
BAT 13-14 Required BAT caps 10 μ 10 μ 10 μ 10 μ 2.2 μ	PMID	23	Required	PMID caps	8.2uF	10uF			
BAT Laps 10uF 10uF 10uF 20uF 20uF 20uF 20uF 20uF 20uF 20uF 2								Positive battery connection point	
SYS 15-16 Required SYS caps 10uF 20uF 20uF Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 6V or higher rating, X7R or X5R. Switching node connecting to output inductor 19-20 Required Output inductor 1uH 2.2uH Switching node connecting to output inductor Optional SW Resistor • Ω Optional SW Cap • F Switching converter snubber circuit Shubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs. PWM high side driver positive supply. PWM high side driver positive supply. Connect the 0.047µF bootstrap capacitor from SW to BTST.	BAT	13-14	Required	BAT caps	10uF	10uF			sensing is connected between SYS and BAT. 1. Connect a 10 μF closely to the BAT pin. 2. Charger may operat
SW 19-20 Required SYS caps 10uF 20uF 20uF Switching node connecting to output inductor 19-20 Required Output inductor 1 uH 2.2 uH Optional SW Resistor Optional SW Cap								Converter output connection point	
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Optional SW Resistor	3W	19-20	Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
Optional SW Cap * F Switching converter snubber circuit designs. PWM high side driver positive supply. Required BTST-SW cap 0.047uF			Optional	SW Resistor		* Ω			
81S1 21 Required BTST-SW cap 0.047uF 0.047uF 0.047uF Connect the 0.047µF bootstrap capacitor from SW to BTST.				SW Cap		* F			
	BTST	21	Descripted	DTCT CIM	0.047.5	0.047. 5	0.047.5		Country of College Col
Upuonat B1ST resistor *Ω Bootstrap capacitor snubbing resistor Help with EMI performance. Recommend unpopulated footprint on new designs.			· · · · · · · · · · · · · · · · · · ·		U.U47uF		U.U47uF		<u> </u>
			Optional	BTST resistor		* Ω		Bootstrap capacitor snubbing resistor	Help with EMI performance. Recommend unpopulated footprint on new designs.

REGN	22						PWM low side driver positive supply output.	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10 Vrating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of the TS pin.
							Power ground	
GND	17-18	Required						On PCB layout, connect directly to ground connection of input and output capacitors of the charger. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.
Thermal PAD		Required						Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.