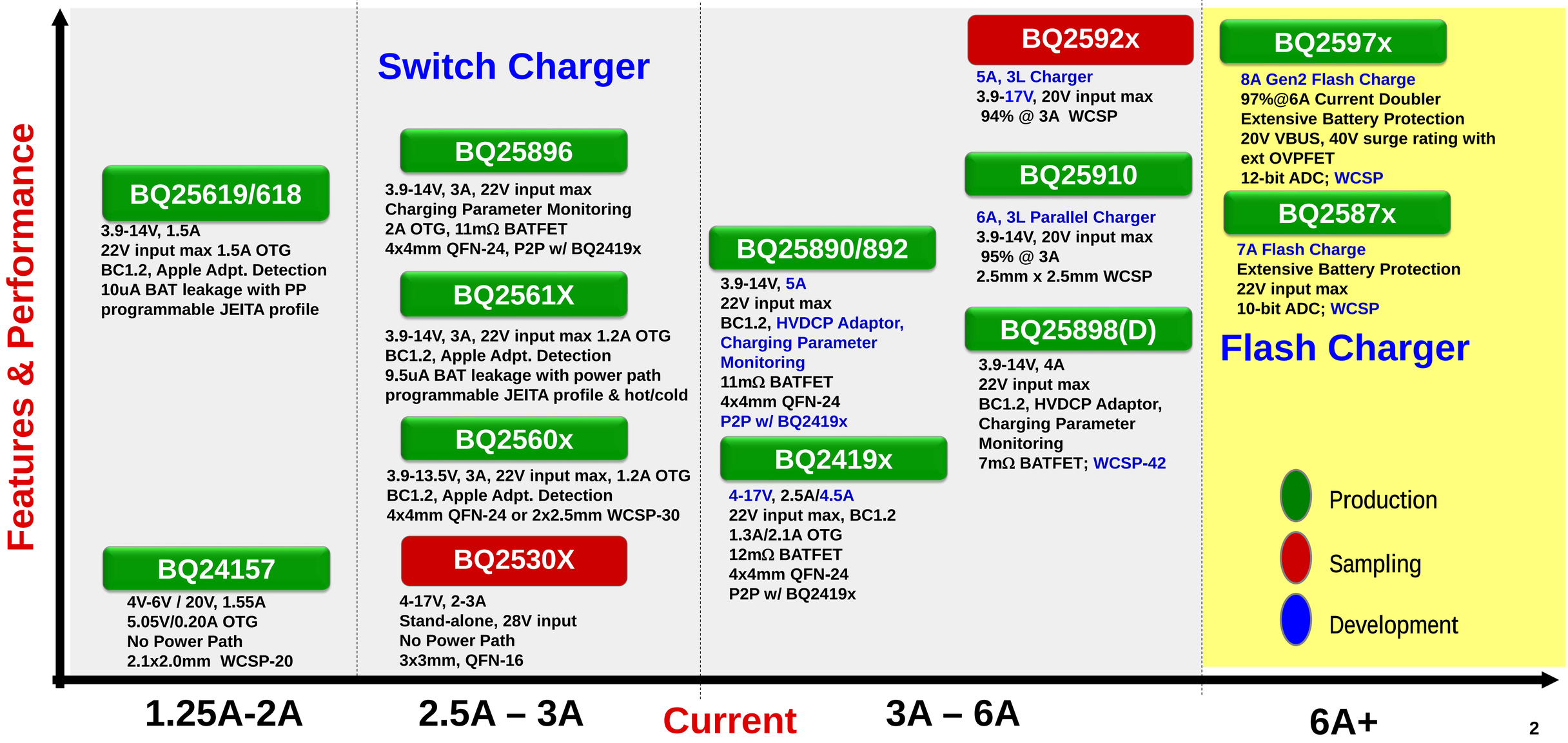
BQ25611 Product Overview

BMS-BCP

Single cell switch-mode charger roadmap



BQ25611 I2C 1-Cell 3A Charger

Features

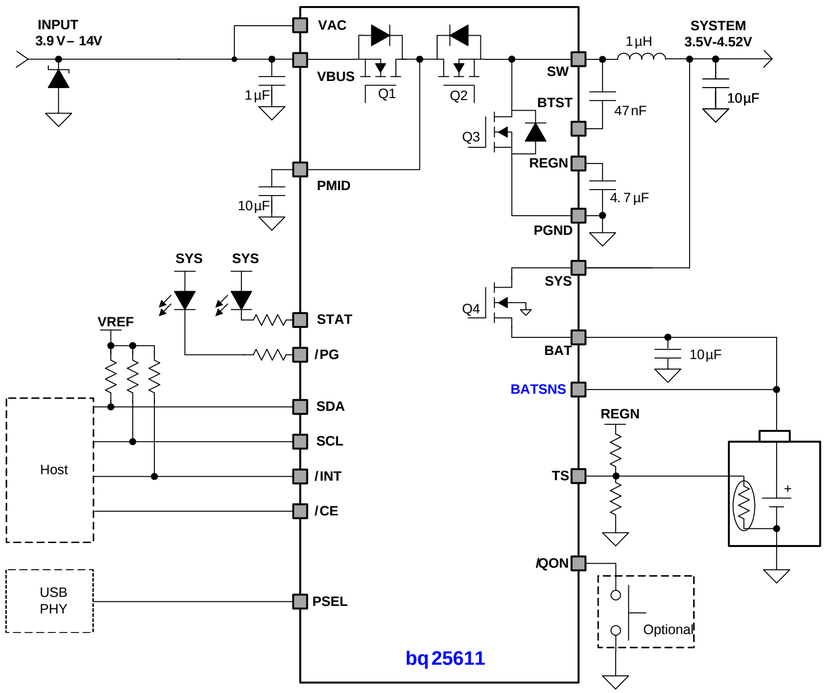
- USB-Compliant Switch Mode 3A NVDC Charger
  - Input Voltage from 3.9V to 13.5V, 22V Max
  - Adapter over-voltage protection 14.2V
  - 130ns Internal Input OVP Response Time
- Instant System on with Deeply Discharged Battery or No Battery with power path.
- Charger efficiency: 92% @ 2A at 5V Input, Boost Output voltage: 91% @ 1A
- Extremely low 9.5uA BAT leakage in system standby, and 7uA in shipping mode.
- I2C Flexibility Configuration
  - 3.5V - 4.52V battery voltage
  - 4.6V/4.85V/5V/5.15V OTG CV voltage and 0.5A/1.2A OTG CC current
  - Programmable battery JEITA and hot/cold profile
- Support VIN and IIN Based Dynamic Power Management
- High Integration and Low BOM
  - Integrated 19.5mΩ BATFET, and all power path/current sensing FETs
  - Remote BATSNS to reduce charge time
  - VREG is on BAT if BATSNS is open or short to GND
- High Safety
  - Input Over-voltage Protection
  - Charge Safety Timer
  - Thermal Regulation and Thermal Shutdown
- Package: QFN-24 4x4mm2

Benefits

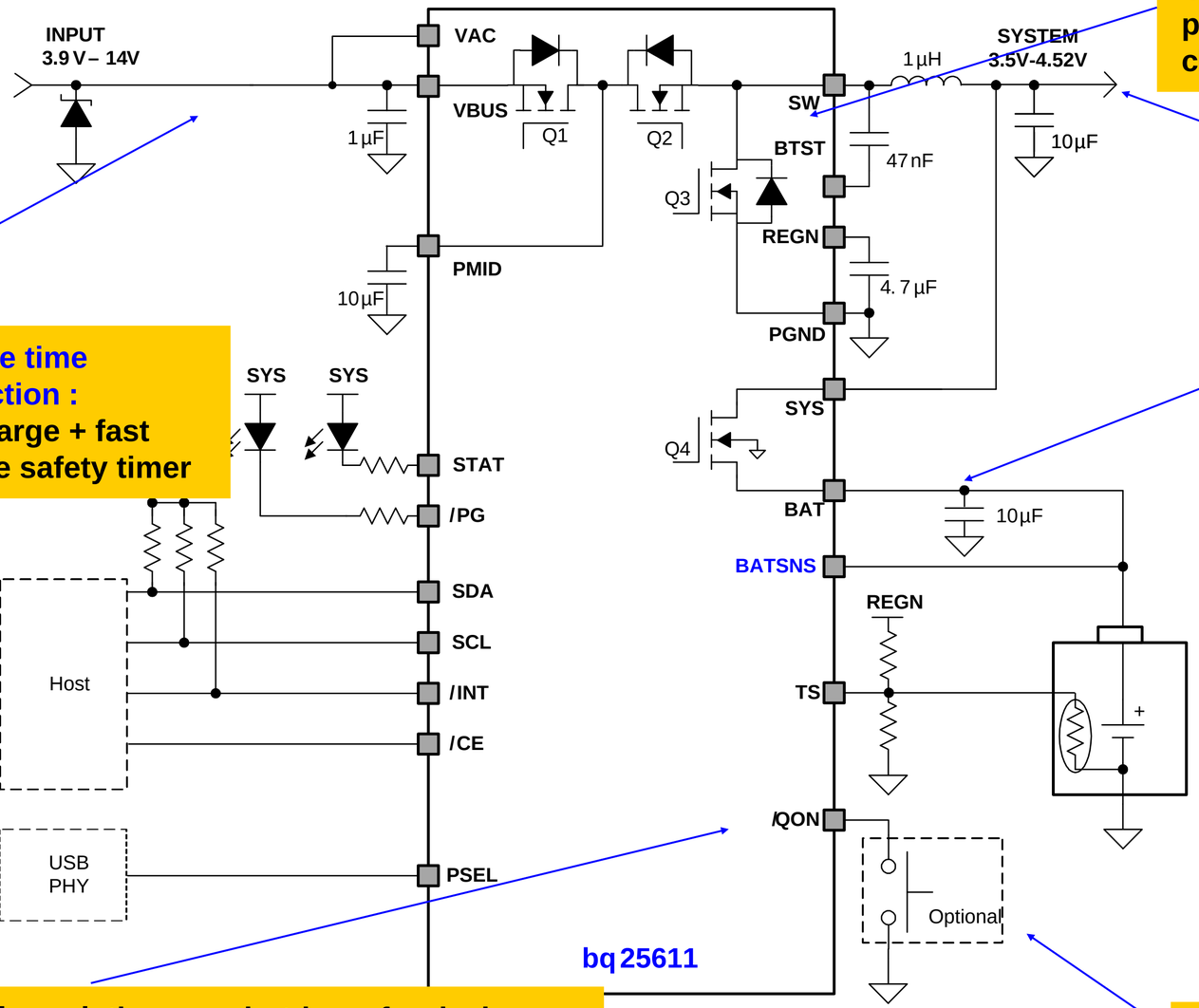
- VREG 10mV step to optimize battery voltage setting
- Reduce charge time with BAT remote sense
- Long battery run time with 19.5mΩ Battery FET
- Programmable JEITA and hot/cold profile setting
- OTG CV/CC regulation and over current and short current protection

Applications

- Smart Phone, Portable Devices
- Portable Accessories



BQ25611 Application Diagram



Cycle-by-Cycle OCP: Over current protection for charging and OTG

VINDPM and IINDPM : input volatge and current limit

SYSOVP : System Overvoltage Protection f

Charge time protection : Precharge + fast charge safety timer

BATOCP: Up to 3.0A Charge Current and 6A Discharge Current

BATOVP : Protection from Overcharge

BAT temp protection Buck/Boost : Thermistor Monitoring for Battery overtemp / undertemp

Thermal protection Thermal regulations or shutdown for device overtemp

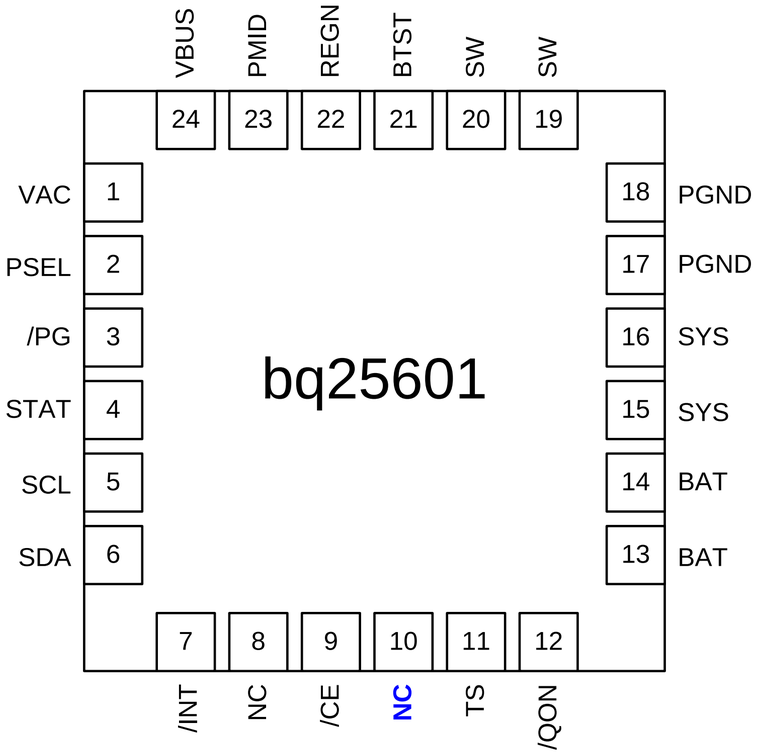
/QON: Shipping Mode and System Reset

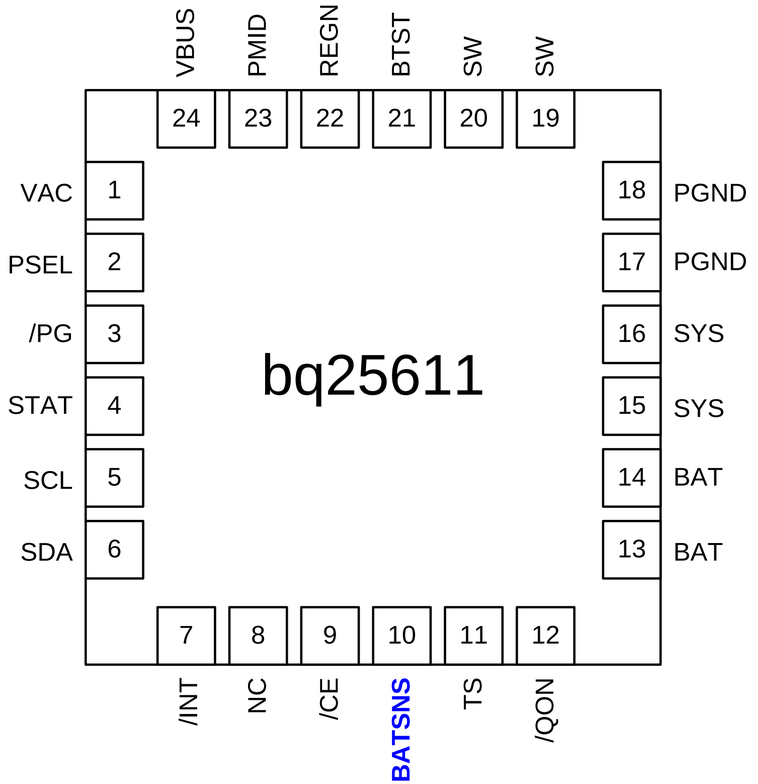
BQ25611 vs BQ25601

Features	BQ25601	BQ25611
Battery Only Quiescent Current (typical) when adapter is not present	57uA with Q4 on	9.5uA with Q4 on
	17uA with Q4 off (shipmode)	7uA with Q4 off
Battery Voltage	3.856V -4.624V, 32mV/step	3.5V-4.3V (100mV/step)
		4.3V-4.52V (10mV/step)
	Default 4.208V (VSYSMIN 3.5V)	Default 4.200V (VSYSMIN 3.5V)
Input OV Threshold	VBUS OV 6.5V	VBUS OV 14V
Battery Remote Sense with Open/Short Detection	No	Yes (611 drop-in replacement of 601)
TS profile	JEITA with fixed temperature, and adjustable ICHG/VREG	JEITA with adjustable T2/T3, more ICHG/VREG options (REG0C)
OTG V/I Regulation	CV on PMID 4.85V/5V/5.15V/5.3V	CV on PMID 4.6V/4.75V/5V/5.15V
	CC 0.5A/1.2A	CC 0.5A/1.2A

BQ25611 Drop-in Replacement for BQ25601

- BQ25611 and BQ25601 are pin-to-pin compatible
- BATSNS on BQ25611 is for battery remote sense to reduce charge time
- BATSNS pin can be floated or short if not used



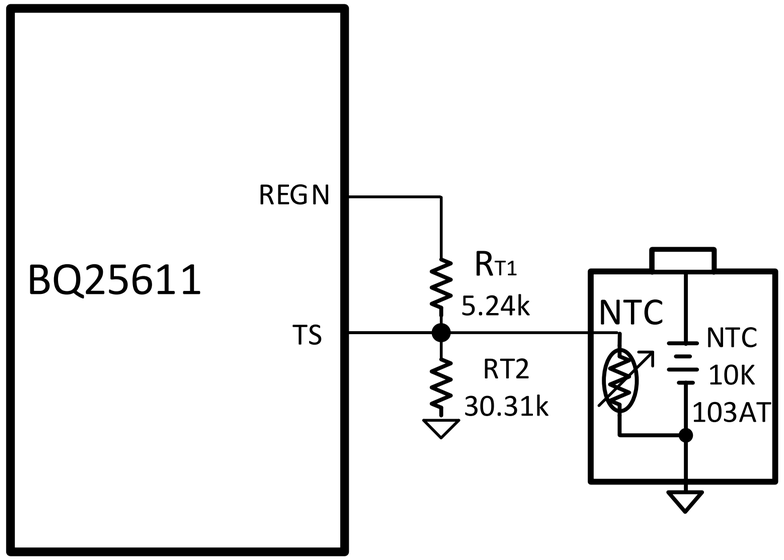


Battery voltage setting

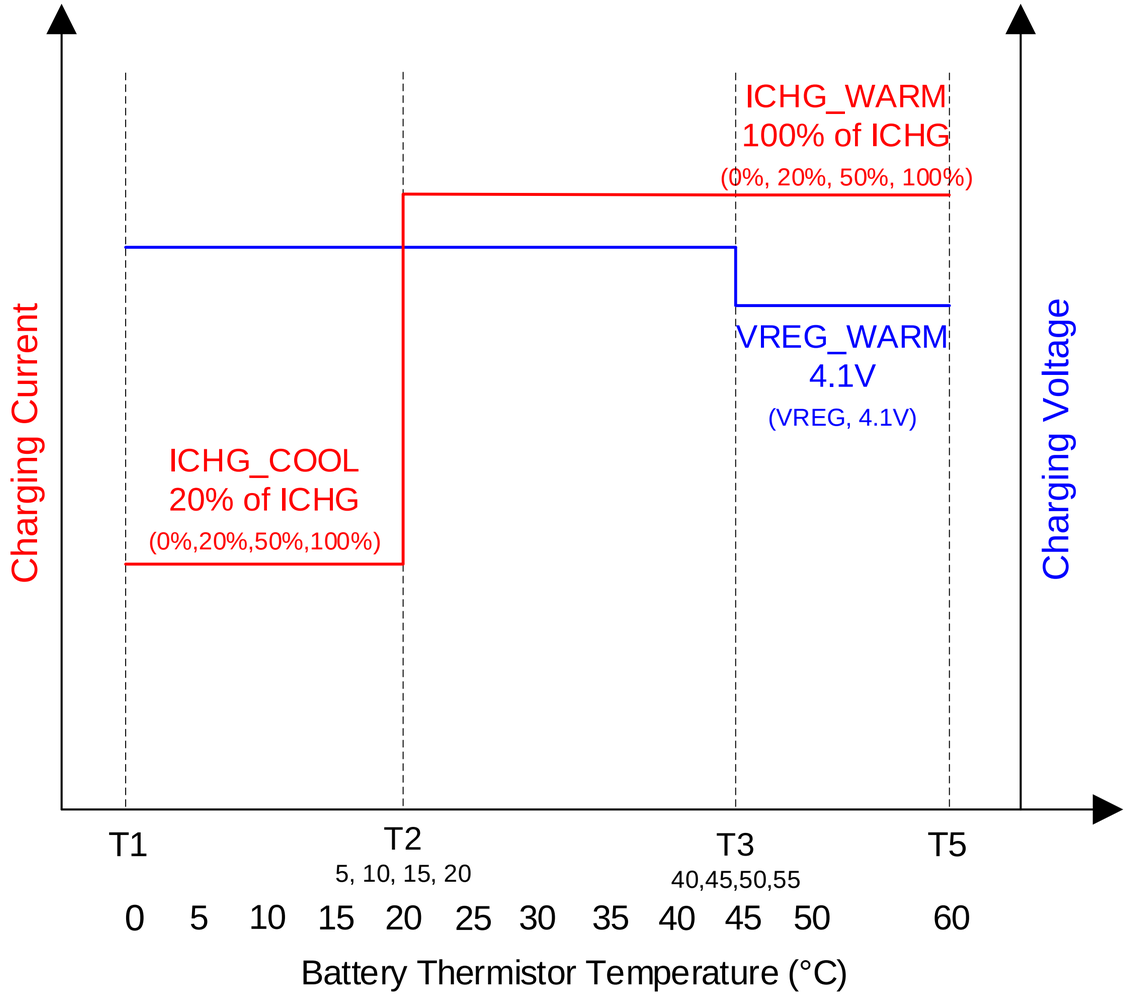
Registers	BATREG (V)
	BQ25611
00000	3.50
00001	3.60
00010	3.70
00011	3.80
00100	3.90
00101	4.00
00110	4.10
00111	4.15
01000	4.20
01001	4.30
01010	4.31
01011	4.32
01100	4.33
01101	4.34
01110	4.35
01111	4.36
10000	4.37

Registers	BATREG (V)
	BQ25611
10001	4.380
10010	4.390
10011	4.400
10100	4.410
10101	4.420
10110	4.430
10111	4.440
11000	4.450
11001	4.460
11010	4.470
11011	4.480
11100	4.490
11101	4.500
11110	4.510
11111	4.520

Programmable JEITA or hot/cold setting



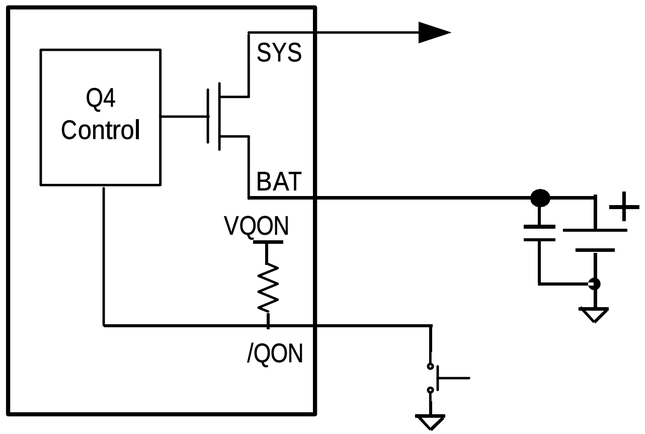
- T1 and T5 are resistor RT1 / RT2 programmable
- JEITA profile:
  - T2 is programmable by register bits: 5C/10C/15C/20C for T1 = 0C and T5 = 60C
  - T3 is programmable by register bits: 40C/45C/50C/55C for T1 = 0C and T5 = 60C
- Hot/Cold profile:
  - Set 100% during T1-T2
  - Disable charge during T3-T5.



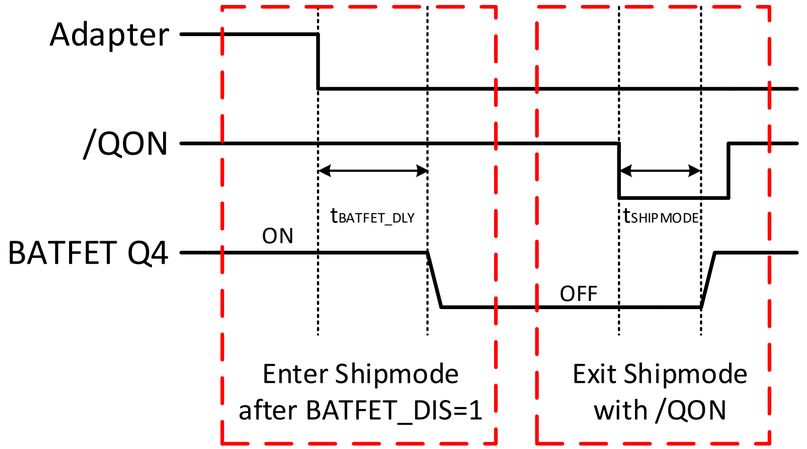
TS Setting For Cold/Hot

- 0°C to 45°C Cold/Hot Setting
  - Select 10k thermistor 103AT-2,3, $\beta = 3435K$
  - Set T1 = 0°C and T5 = 60 °C by selecting RT1 = 5.23kΩ and RT2 = 30.9kΩ
  - T2 = 10°C and T3 = 45°C by default with above setting
  - Set ICHG = 100% at Cool by setting JEITA_COOL_ISET [1,0] = 11
  - Disable warm charge by setting JEITA_WARM_ISET [1, 0] = 00
- 0°C to 53°C Cold/Hot Setting
  - Select 10k thermistor 103AT-2,3, $\beta = 3435K$
  - Set T1 = 0°C and T5 = 70°C by selecting RT1 = 3.74kΩ and RT2 = 16.9kΩ
  - T2 = 15.5°C and T3 = 53°C by default with above setting
  - Set ICHG = 100% at Cool by setting JEITA_COOL_ISET [1,0] = 11
  - Disable warm charge by setting JEITA_WARM_ISET [1, 0] = 00

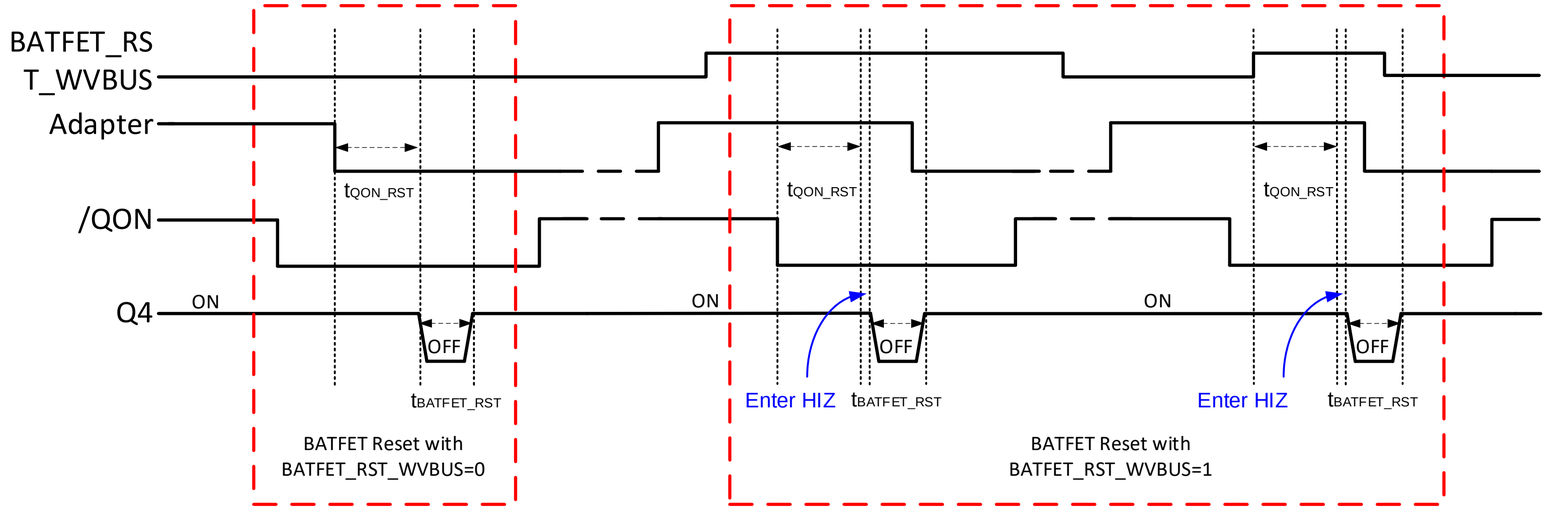
Push button for shipmode and power cycle



Shipmode Exit with /QON



System reset with or without adapter



BQ25601 and BQ25611 Register Comparison

REG00

BQ2560x

Table 6. REG00 Field Descriptions

Bit	Field	POR	Type[1]	Reset	Description	Comment
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	0 – Disable, 1 – Enable	Enable HIZ Mode 0 – Disable (default) 1 – Enable
6	EN_ICHG_MON[1]	0	R/W	by REG_RST	00 - Enable STAT pin function (default) 01 - Reserved 10 - Reserved 11 - Disable STAT pin function (float pin)	
5	EN_ICHG_MON[0]	0	R/W	by REG_RST		
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input Current Limit Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default:2400 mA (10111), maximum input current limit, not typical. IINDPM bits are changed automatically after input source detection is completed Host can over-write IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

(1) LEGEND: R/W = Read/Write; R = Read only

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Table 7. REG00 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	HIZ mode enable in buck mode. 0 – Disable (default) 1 – Enable	
6	TS_IGNORE	0	R/W	by REG_RST	When charger does not monitor the NTC, host sets this bit to 1 to ignore the TS pin condition during charging and boost mode. 0 – Include TS pin into charge and boost mode enable conditions. (default) 1 – Ignore TS pin. Always consider TS is good to allow charging and boost mode. NTC_FAULT bits are 000 to report normal status.	
5	BATSNS_DIS	0	R/W	by REG_RST	Select either BATSNS pin or BAT pin to regulate battery voltage. 0 – Enable BATSNS in battery CV regulation. If the device fails BATSNS open/short detection (BATSNS_STAT = 1). Battery voltage is regulated through BAT pin. (default) 1 – Disable BATSNS. Use BAT pin in battery CV regulation.	
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input current limit setting (maximum limit, not typical) Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default: 2400 mA (10111) IINDPM bits are changed automatically after Input Source Type Detection (IINDPM Threshold) is completed PSEL HIGH = 500 mA PSEL LOW = 2.4 A Host can reprogram IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

LEGEND: R/W = Read/Write; R = Read only

REG04

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Figure 32. Register REG04

7	6	5	4	3	2	1	0
VREG[4]	VREG[3]	VREG[2]	VREG[1]	VREG[0]	TOPOFF_TIMER[1]	TOPOFF_TIMER[0]	VRECHG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 10. REG04 Field Descriptions

Bit	Field	POR	Type[1]	Reset	Description	Comment
7	VREG[4]	0	R/W	by REG_RST by Watchdog	512 mV	Charge Voltage Offset: 3.847 V Range: 3.847 V to 4.615 V (11000) Default: 4.199 V (01011) Special Value: (01111): 4.343 V Note: Value above 11000 (4.615 V) is clamped to register value 11000 (4.615 V)
6	VREG[3]	1	R/W	by REG_RST by Watchdog	256 mV	
5	VREG[2]	0	R/W	by REG_RST by Watchdog	128 mV	
4	VREG[1]	1	R/W	by REG_RST by Watchdog	64 mV	
3	VREG[0]	1	R/W	by REG_RST by Watchdog	32 mV	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes	The extended time following the termination condition is met. When disabled, charge terminated when termination conditions are met
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog		
0	VRECHG	0	R/W	by REG_RST by Watchdog	0 – 100 mV 1 – 200 mV	Recharge threshold Default: 100mV (0)

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Table 11. REG04 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBATREG[4]	0	R/W	by REG_RST by Watchdog	Battery voltage setting, also called VREG. Default: 4.200 V (01000) 00000 – 3.504 V 00001 – 3.6 V 00010 – 3.696 V 00011 – 3.8V 00100 – 3.904 V 00101 – 4.0 V 00110 – 4.10 V 00111 – 4.15 V 01000 – 4.20 V 01001 - 11111 – 4.30 V - 4.52 V, 10 mV/step 01110 4.35 V, 10011 4.4 V, 11000 4.45 V, 11101 4.5 V
6	VBATREG[3]	1	R/W	by REG_RST by Watchdog	
5	VBATREG[2]	0	R/W	by REG_RST by Watchdog	
4	VBATREG[1]	0	R/W	by REG_RST by Watchdog	
3	VBATREG[0]	0	R/W	by REG_RST by Watchdog	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	Top-off timer setting. 00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog	
0	VRECHG	0	R/W	by REG_RST by Watchdog	Battery recharge threshold setting. 0 – 120 mV (default) 1 – 210 mV

LEGEND: R/W = Read/Write; R = Read only

REG05

BQ2560x

Figure 33. Register REG05

7	6	5	4	3	2	1	0
EN_TERM	Reserved	WATCHDOG[1]	WATCHDOG[0]	EN_TIMER	CHG_TIMER	TREG	JEITA_ISET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 11. REG05 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	EN_TERM	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable	Default: Enable termination (1)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved	Reserved
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	00 – Disable timer, 01 – 40 s, 10 – 80 s,11 – 160 s	Default: 40 s (01)
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog		
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Enable both fast charge and precharge timer	Default: Enable (1)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	0 – 5 hrs 1 – 10 hrs	Default: 10 hours (1)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 - 90°C 1 - 110°C	Default: 110°C (1)
0	JEITA_ISET (0C-10C)	1	R/W	by REG_RST by Watchdog	0 – 50% of ICHG 1 – 20% of ICHG	Default: 20% (1)

(1) LEGEND: R/W = Read/Write; R = Read only

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Table 12. REG05 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	EN_TERM	1	R/W	by REG_RST by Watchdog	Battery charging termination enable. 0 – Disable 1 – Enable (default)
6	Reserved	0	R/W	by REG_RST by Watchdog	
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	Watchdog timer setting. 00 – Disable timer 01 – 40 s (default) 10 – 80 s 11 – 160 s
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog	
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	Battery charging safety timer enable, including both fast charge and pre-charge timers. Precharge timer is 2 hours. Fast charge timer is set by REG05[2] 0 – Disable 1 – Enable timer (default)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	Battery fast charging safety timer setting. 0 – 20 hrs 1 – 10 hrs (default)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 – 90°C 1 – 110°C (default)
0	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	Battery voltage setting during JEITA warm (T3 - T5, typically 45C - 60C) 0 – Set Charge Voltage to 4.1 V (max) (default) 1 – Set Charge Voltage to VREG

LEGEND: R/W = Read/Write; R = Read only

REG07

BQ2560x

7	6	5	4	3	2	1	0
IINDET_EN	TMR2X_EN	BATFET_DIS	JEITA_VSET	BATFET_DLY	BATFET_RST_EN	VDPM_BAT_TRACK[1]	VDPM_BAT_TRACK[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. REG07 Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description	Comment
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	0 - Not in input current limit detection 1 - Force input current limit detection when VBUS is present	Returns to 0 after input detection is complete
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	0 – Disable 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool, or thermal regulation	
5	BATFET_DIS	0	R/W	by REG_RST	0 – Allow Q4 turn on, 1 – Turn off Q4 with t_{BATFET_DLY} delay time (REG07[3])	Default: Allow Q4 turn on(0)
4	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	0 – Set Charge Voltage to 4.1V (max), 1 – Set Charge Voltage to VREG	
3	BATFET_DLY	1	R/W	by REG_RST	0 – Turn off BATFET immediately when BATFET_DIS bit is set 1 –Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set	Default: 1 Turn off BATFET after t_{BATFET_DLY} (typ. 10 s) when BATFET_DIS bit is set
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	0 – Disable BATFET reset function 1 – Enable BATFET reset function	Default: 1 Enable BATFET reset function
1	VDPM_BAT_TRACK[1]	0	R/W	by REG_RST	00 - Disable function (VINDPM set by register) 01 - VBAT + 200mV 10 - VBAT + 250mV 11 - VBAT + 300mV	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VDPM_BAT_TRACK
0	VDPM_BAT_TRACK[0]	0	R/W	by REG_RST		

(1) LEGEND: R/W = Read/Write; R = Read only

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Table 14. REG07 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	Force input source type detection. After the detection is complete, this bit returns to 0. 0 – Not in input current limit detection. (default) 1 – Force input current limit detection when VBUS is present.
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	Safety timer is slowed by 2X during input DPM, JEITA cool/warm or thermal regulation. 0 – Disable. Safety timer duration is set by REG05[2]. 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool/warm (except ICHG=100%), or thermal regulation. (default)
5	BATFET_DIS	0	R/W	by REG_RST	BATFET Q4 ON/OFF control. Set this bit to 1 to enter ship mode. To reset the device with adapter present, the host shall set BATFET_RST_WVBUS to 1 and then BATFET_DIS to 1. 0 – Turn on Q4. (default) 1 – Turn off Q4 after t_{BATFET_DLY} delay time (REG07[3])
4	BATFET_RST_WVBUS	0	R/W	by REG_RST	Start BATFET full system reset with or without adapter present. 0 – Start BATFET full system reset after adapter is removed from VBUS. (default) 1 – Start BATFET full system reset when adapter is present on VBUS.
3	BATFET_DLY	1	R/W	by REG_RST	Delay from BATFET_DIS (REG07[5]) set to 1 to BATFET turn off during ship mode. 0 – Turn off BATFET immediately when BATFET_DIS bit is set. 1 – Turn off BATFET after t_{BATFET_DLY} (typ 10 s) when BATFET_DIS bit is set. (default)
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	Enable BATFET full system reset. The time to start of BATFET full system reset is based on the setting of BATFET_RST_WVBUS bit. 0 – Disable BATFET reset function 1 – Enable BATFET reset function when REG07[5] is also 1. (default)
1	VINDPM_BAT_TRACK[1]	0	R/W	by REG_RST	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and VBAT + VINDPM_BAT_TRACK. 00 – Disable function (VINDPM set by register) (default) 01 – VBAT + 200 mV 10 – VBAT + 250 mV 11 – VBAT + 300 mV
0	VINDPM_BAT_TRACK[0]	0	R/W	by REG_RST	

LEGEND: R/W = Read/Write; R = Read only

Reg0A

BQ2560x

Figure 38. Register REG0A

7	6	5	4	3	2	1	0
VBUS_GD	VINDPM_STAT	IINDPM_STAT	Reserved	TOPOFF_ACTIVE	ACOV_STAT	VINDPM_INT_MASK	IINDPM_INT_MASK
R	R	R	R	R	R	R/W	R/W

Table 16. REG0A Field Descriptions

Bit	Field	POR	Type(1)	Reset	Description
7	VBUS_GD	x	R	NA	0 – Not VBUS attached, 1 – VBUS Attached
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM, 1 – in VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM, 1 – in IINDPM
4	Reserved	x	R	NA	
3	TOPOFF_ACTIVE	x	R	NA	0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	x	R	NA	0 – Device is NOT in ACOV 1 – Device is in ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow VINDPM INT pulse 1 - Mask VINDPM INT pulse
0	IINDPM_INT_ MASK	0	R/W	by REG_RST	0 - Allow IINDPM INT pulse 1 - Mask IINDPM INT pulse

(1) LEGEND: R/W = Read/Write; R = Read only

BQ2561x

Table 17. REG0A Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_GD	x	R	NA	0 – VBUS does not pass poor source detection 1 – VBUS passes poor source detection
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM 1 – In VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM 1 – In IINDPM
4	BATSNS_STAT	x	R	NA	0 – BATSNS pin is in good connection. Regulation battery voltage through BATSNS pin. 1 – BATSNS pin is open/short. Regulate battery voltage through BAT pin.
3	TOPOFF_ACTIVE	x	R	NA	0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	x	R	NA	0 – Not in ACOV 1 – In ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	Allow or block $\overline{INT}$ pulse assertion to host during VINDPM. 0 – $\overline{INT}$ is asserted to host during VINDPM (default) 1 – No $\overline{INT}$ pulse asserted to host during VINDPM
0	IINDPM_INT_ MASK	0	R/W	by REG_RST	Allow or block $\overline{INT}$ pulse assertion to host during IINDPM 0 – $\overline{INT}$ is asserted to host during IINDPM (default) 1 – No $\overline{INT}$ pulse asserted to host during IINDPM

LEGEND: R/W = Read/Write; R = Read only

REG0C

BQ2560x

No REG0C

BQ2561x

Table 19. REG0C Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	JEITA_COOL_ISET [1]	0	R/W	by REG_RST by Watchdog	Fast charge current setting during cool temperature range (T1 - T2), as percentage of ICHG in REG02[5:0]. 00 – No Charge 01 – 20% of ICHG (default) 10 – 50% of ICHG 11 – 100% of ICHG (safety timer does not become 2X)
6	JEITA_COOL_ISET [0]	1	R/W	by REG_RST by Watchdog	
5	JEITA_WARM_ISET [1]	1	R/W	by REG_RST by Watchdog	Fast charge current setting during warm temperature range (T3 - T5), as percentage of ICHG in REG02[5:0]. 00 – No Charge 01 – 20% of ICHG 10 – 50% of ICHG 11 – 100% of ICHG (safety timer does not become 2X) (default)
4	JEITA_WARM_ISET [0]	1	R/W	by REG_RST by Watchdog	
3	JEITA_VT2 [1]	0	R/W	by REG_RST by Watchdog	00 – VT2% = 70.75% (5.5°C) 01 – VT2% = 68.25% (10°C) (default) 10 – VT2% = 65.25% (15°C) 11 – VT2% = 62.25% (20°C)
2	JEITA_VT2 [0]	1	R/W	by REG_RST by Watchdog	
1	JEITA_VT3 [1]	0	R/W	by REG_RST by Watchdog	00 – VT3% = 48.25% (40°C) 01 – VT3% = 44.75% (44.5°C) (default) 10 – VT3% = 40.75% (50.5°C) 11 – VT3% = 37.75% (54.5°C)
0	JEITA_VT3 [0]	1	R/W	by REG_RST by Watchdog	

LEGEND: R/W = Read/Write; R = Read only