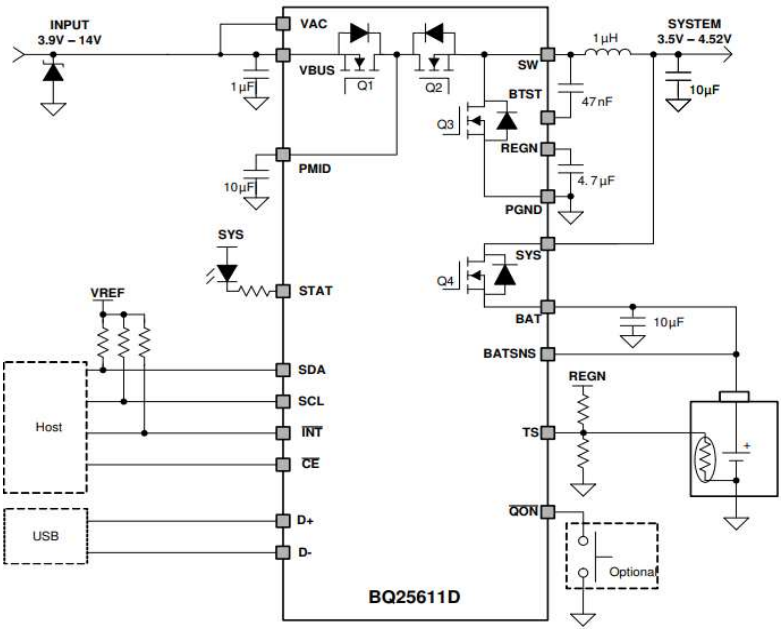
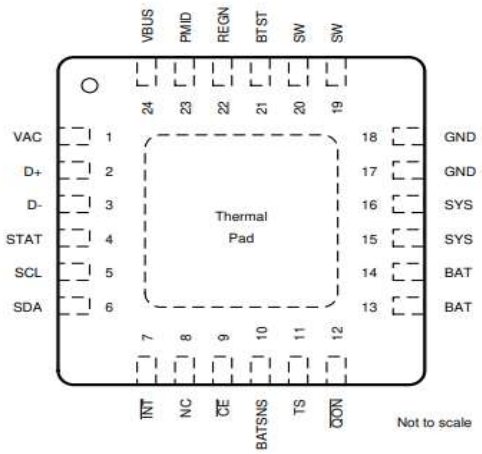
BQ25611D TYPICAL SCHEMATIC



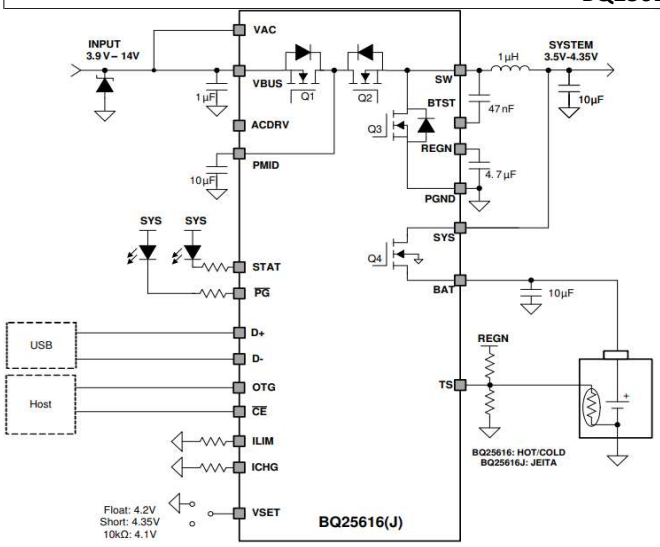


BQ25611D SCHMATIC CHECKLIST

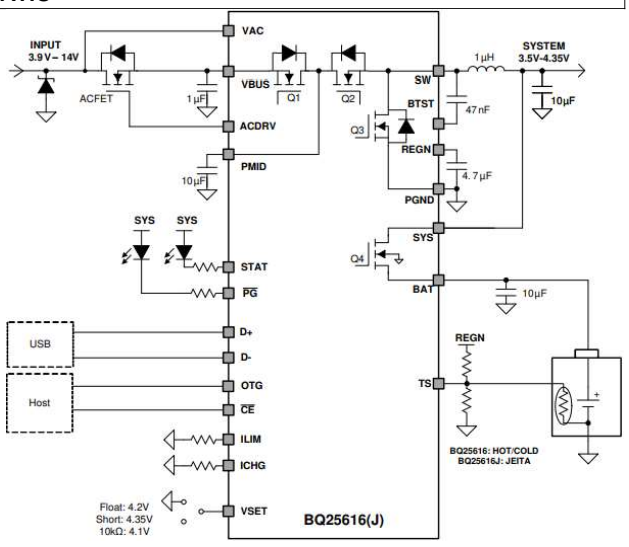
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							USB data line pair	
D+/D-	2,3	Optional					Positive line of the USB data line pair.	1. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and non-standard adaptors.
		Optional					Negative line of the USB data line pair.	
							Open drain charge status output	
STAT	4	Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it floating. 2. The STAT pin indicates charger status. Connect a current limiting resistor and an LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses
							I2C Interface clock and data	
SCL/SDA	5-6	Optional	SCL resistor		10 kΩ		Connect SCL to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
		Optional	SDA resistor		10 kΩ		Connect SDA to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
							Open-drain Interrupt Output	
INT	7	Optional	INT resistor		10 kΩ		Connect the INT to a logic rail via 10-kΩ resistor.	1. If not used, leave it floating. 2. The INT pin sends an active low, 256-µs pulse to host to report charger device status and fault.
							No connect	
NC	8	Optional						Float this pin
							Active low Charge Enable pin	
/CE	9	Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[4] = 1 and CE pin = Low.
							Battery voltage sensing pin for charge voltage regulation	
BATSNS	10	Optional					In order to minimize the parasitic trace resistance during charging, BATSNS pin is connected to the positive terminal of battery pack as close as possible	If BATSNS pin is open, BATSNS_STAT bit is set to 1 and charger regulates the battery voltage through BAT pin. If BATSNS is unused, this pin should be floating.
							Temperature qualification voltage inputs for JEITA	
TS	11	Optional if TS_IGNORE=1	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	 1. If thermistor is not used, set TS pin voltage within normal range or set TS_IGNORE to 1 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
							BATFET enable/reset control input	
/QON	12	Optional			Switch			1.If not used, leave it floating. 2.The pin contains an internal pull-up to maintain default high logic. 3.When BATFET is in ship mode, a logic low of tSHIPMODE duration turns on BATFET to exit ship mode. When the BATFET is not in ship mode, a logic LOW of tQON_RST (minimum 8 s) duration resets SYS (system power) by turning BATFET off for tBATFET_RST (minimum 250ms) and then re-enables BATFET to provide full system power reset. The host chooses the BATFET reset function with VBUS unplugged or not through I2C bit BATFET_RST_WVBUS.
							Charge input voltage sense	
VAC	1	Required						Charge input voltage sense. This pin must be connected to VBUS pin.
							Charge input voltage	
VBUS	24	Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
							Actual input source to the charger	
PMID	23	Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
		Optional	PMID caps		1nF			For optimal EMC add a 1nF, 0402 capacitor with a minimal loop to GND
							Positive battery connection point	
BAT	13-14	Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.
							Converter output connection point	
SYS	15-16	Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 10V or higher rating, X7R or X5R.

SW	19-20						**Switching node connecting to output inductor**	
		Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	21						**PWM high side driver positive supply.**	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047μF, 25V rated bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor series snubbing resistor	Helps with EMI performance. Recommend a 0ohm, 0402 on new designs.
REGN	22						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 μF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN must serve as the bias rail of the TS pin.
GND	17-18						**Power ground**	
		Required						On the PCB layout, connect the input and output capacitors of the charger directly to GND. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.
Thermal PAD		Required						Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.

BQ25616(J) TYPICAL SCHEMATIC

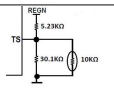


Without external ACFET



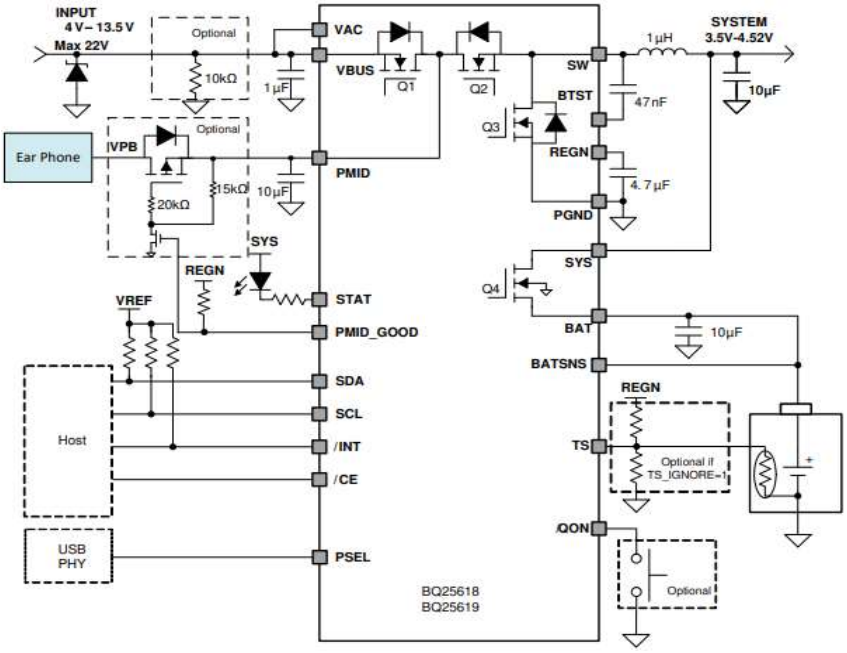
With external ACFET

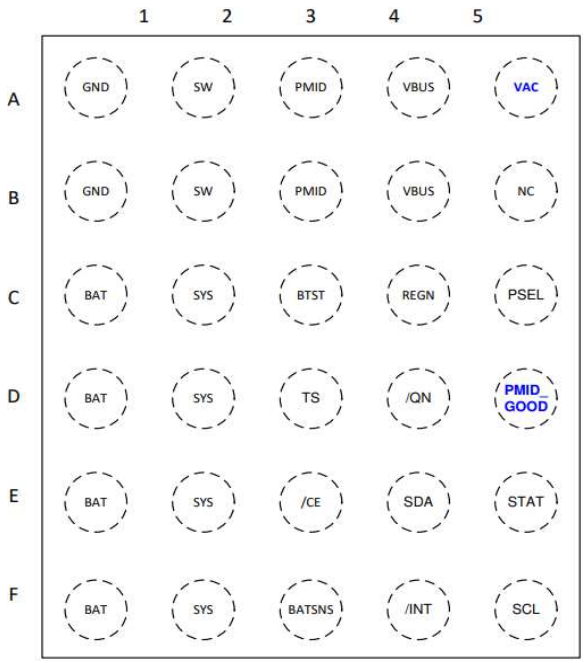
BQ25616(J) SCHMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
D+/D-	3,4						**USB data line pair**	
		Optional					Positive line of the USB data line pair.	1. D+/D- based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and non-standard adaptors.
		Optional					Negative line of the USB data line pair.	
STAT	5						**Open drain charge status output**	
		Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it floating. 2. The STAT pin indicates charger status. Connect a current limiting resistor and an LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses
OTG	6						**Active high boost mode enable pin**	
		Optional						1. If OTG boost mode is not used, short it to ground. 2. When this pin is pulled HIGH, OTG is enabled. 3. OTG cannot be floating
/PG	7						**Open drain active low power good indicator.**	
		Optional	PG resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 10-kΩ resistor.	LOW indicates a good input source if the input voltage is between UVLO and ACOV, above SLEEP mode threshold, and current limit is above 30 mA.
ACDRV	2						**Charge pump output to drive external N-channel MOSFET (ACFET)**	
		Optional	ACFET					It provides 6V voltage above VBUS as gate drive to turn on ACFET when VAC voltage is below ACOV threshold (14.2- V) and above UVLO. Leave ACDRV floating if external OVP is not being used.
/CE	9						**Active low Charge Enable pin**	
		Required						When this pin is driven low, battery charging is enabled.
ILIM	8						**Input current limit setting**	
		Required	ILIM resistor		* Ω		A resistor is connected from ILIM pin to ground to set the input current limit	1.The acceptable range for ILIM current is 500 mA - 3200 mA. 2. The resistor based input current limit is effective only when the input adapter is detected as unknown. Otherwise, the input current limit is determined by D+/D– detection outcome. IINDPM = KILIM/RILIM
ICHG	10						**Charge current limit setting**	
		Required	ICHG resistor		* Ω		A resistor is connected from ICHG pin to ground to set charge current limit	The acceptable range for charge current is 300 mA – 3000 mA. ICHG = KICHG/RICHG.
TS	11						**Temperature qualification voltage inputs for JEITA**	
		Required	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	  1. If thermistor is not used, set TS pin voltage within normal range. 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
VSET	12						**Default battery charge voltage setting**	
		Required	VSET resistor		* Ω		Program battery regulation voltage with a resistor pull-down from VSET to GND.	RPD > 50kΩ (float pin) = 4.2V RPD < 500Ω (short to GND) = 4.35V 5kΩ < RPD < 25kΩ = 4.1V
VAC	1						**Charge input voltage sense**	
		Required						Optional external n-channel ACFET is placed between VAC and VBUS. When VAC voltage is below ACOV threshold (14.2-V) and above UVLO, ACFET turns on to connect VAC to VBUS, and power up the charger IC. Short VAC and VBUS if ACFET is not to be used.
VBUS	24						**Charge input voltage**	
		Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
PMID	23						**Actual input source to the charger**	
		Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
		Optional	PMID caps		1nF			For optimal EMC add a 1nF, 0402 capacitor with a minimal loop to GND
BAT	13-14						**Positive battery connection point**	
		Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.
SYS	15-16						**Converter output connection point**	
		Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 10V or higher rating, X7R or X5R.
SW	19-20						**Switching node connecting to output inductor**	
		Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	21						**PWM high side driver positive supply.**	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF, 25V rated bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor series snubbing resistor	Helps with EMI performance. Recommend a 0ohm, 0402 on new designs.
REGN	22						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10 Vrating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN also serves as bias rail of the TS pin.

							Power ground	
GND	17-18	Required						On the PCB layout, connect the input and output capacitors of the charger directly to GND. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.
Thermal PAD		Required						Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. 1) Provide an electrical ground connection for the device. 2. Provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

BQ25618 TYPICAL SCHEMATIC



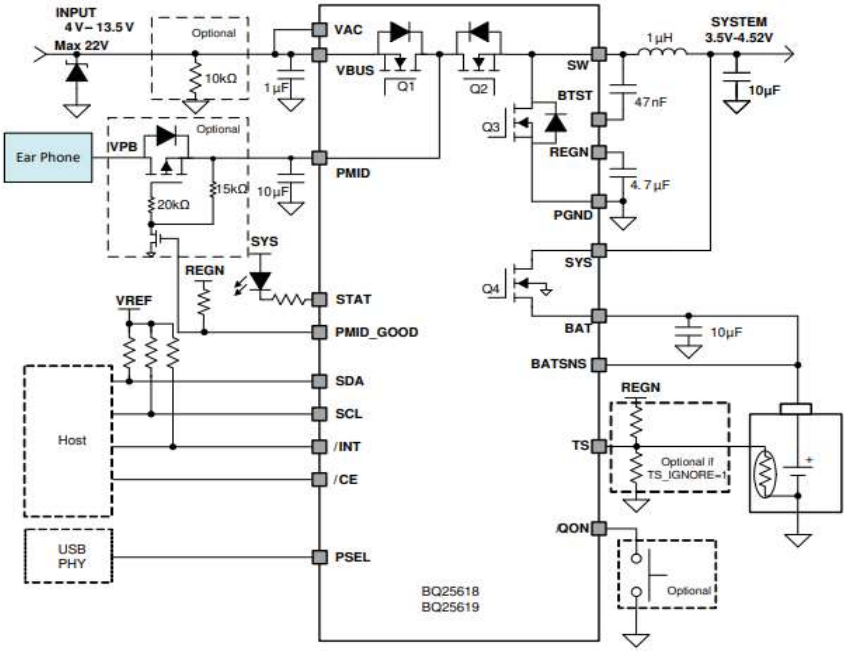


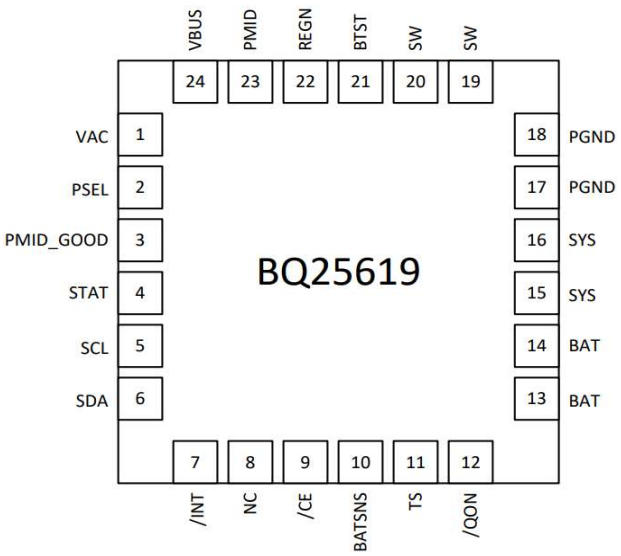
BQ25618 SCHMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							Power Source Selection Input	
PSEL	C5	Required						HIGH indicates 500 mA input current limit. LOW indicates 2.4A input current limit. Once the device gets into host mode, the host can program a different input current limit to the IINDPM register.
							Open drain active high PMID good output	
PMID_GOOD	D5	Optional					Connect to the pull up rail REGN through 10 kΩ resistor	HIGH indicates PMID voltage is below 5.2V and the current through Q1 is below 110% of input current limit. This signal can be used to drive external PMOS FET to disconnect the PMID under charging load when boost mode output voltage is too high or output current is too high.
							Open drain charge status output	
STAT	E5	Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it floating. 2. The STAT pin indicates charger status. Connect a current limiting resistor and an LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses
							I2C Interface clock and data	
SCL/SDA	F5,E4	Optional	SCL resistor		10 kΩ		Connect SCL to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
		Optional	SDA resistor		10 kΩ		Connect SDA to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
							Open-drain Interrupt Output	
INT	F4	Optional	INT resistor		10 kΩ		Connect the INT to a logic rail via 10-kΩ resistor.	1. If not used, leave it floating. 2. The INT pin sends an active low, 256-µs pulse to host to report charger device status and fault.
							No connect	
NC	B5	Optional						Float this pin
							Active low Charge Enable pin	
/CE	E3	Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[4] = 1 and CE pin = Low.
							Battery voltage sensing pin for charge voltage regulation	
BATSNS	F3	Optional					In order to minimize the parasitic trace resistance during charging, BATSNS pin is connected to the positive terminal of battery pack as close as possible	If BATSNS pin is open, BATSNS_STAT bit is set to 1 and charger regulates the battery voltage through BAT pin. If BATSNS is unused, this pin should be floating.
							Temperature qualification voltage inputs for JEITA	
TS	D3	Optional if TS_IGNORE=1	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	 1. If thermistor is not used, set TS pin voltage within normal range or set TS_IGNORE to 1 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
							BATFET enable/reset control input	
/QON	D4	Optional			Switch			1.If not used, leave it floating. 2.The pin contains an internal pull-up to maintain default high logic. 3.When BATFET is in ship mode, a logic low of tSHIPMODE duration turns on BATFET to exit ship mode. When the BATFET is not in ship mode, a logic LOW of tQON_RST (minimum 8 s) duration resets SYS (system power) by turning BATFET off for tBATFET_RST (minimum 250ms) and then re-enables BATFET to provide full system power reset. The host chooses the BATFET reset function with VBUS unplugged or not through I2C bit BATFET_RST_WVBUS.
							Charge input voltage sense	
VAC	A5	Required						Charge input voltage sense. This pin must be connected to VBUS pin.
							Charge input voltage	
VBUS	A4,B4	Optional	VBUS resistor		10 kΩ			Place a 10 kΩ pulldown resistor from VBUS to GND. This component is recommended for applications that make use of the boost mode (OTG) functionality
		Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
							Actual input source to the charger	
PMID	23	Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
		Optional	PMID caps		1nF			For optimal EMC add a 1nF, 0402 capacitor with a minimal loop to GND
							Positive battery connection point	
BAT	C1,D1, E1,F1	Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.

SYS	C2,D2, E2,F2						**Converter output connection point**	
		Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 10V or higher rating, X7R or X5R.
SW	A2,B2						**Switching node connecting to output inductor**	
		Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	C3						**PWM high side driver positive supply.**	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF, 25V rated bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor series snubbing resistor	Helps with EMI performance. Recommend a 0ohm, 0402 on new designs.
REGN	C4						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN must serve as the bias rail of the TS pin.
GND	A1,B1						**Power ground**	
		Required						On the PCB layout, connect the input and output capacitors of the charger directly to GND. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.

BQ25619 TYPICAL SCHEMATIC





BQ25619 SCHMATIC CHECKLIST

PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
PSEL	2						**Power Source Selection Input**	
		Required						HIGH indicates 500 mA input current limit. LOW indicates 2.4A input current limit. Once the device gets into host mode, the host can program a different input current limit to the IINDPM register.
PMID_GOOD	3						**Open drain active high PMID good indicator.**	
		Optional					Connect to the pull up rail REGN through 10 kΩ resistor	HIGH indicates PMID voltage is below 5.2V and the current through Q1 is below 110% of input current limit. This signal can be used to drive external PMOS FET to disconnect the PMID under charging load when boost mode output voltage is too high or output current is too high.
STAT	4						**Open drain charge status output**	
		Optional	STAT resistor		2.2 kΩ	10 kΩ	Connect to the pull up rail via 2.2-kΩ or 10-kΩ resistor.	1. If not used, leave it floating. 2. The STAT pin indicates charger status. Connect a current limiting resistor and an LED from a rail to this pin. 3. Charge in progress: LOW; Charge complete or charger in SLEEP mode: HIGH; Charge suspend (fault response): 1-Hz, 50% duty cycle Pulses
SCL/SDA	5-6						**I2C Interface clock and data**	
		Optional	SCL resistor		10 kΩ		Connect SCL to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
		Optional	SDA resistor		10 kΩ		Connect SDA to the logic rail through a 10-kΩ resistor.	If I2C communication is not used, leave it floating.
INT	7						**Open-drain Interrupt Output**	
		Optional	INT resistor		10 kΩ		Connect the INT to a logic rail via 10-kΩ resistor.	1. If not used, leave it floating. 2. The INT pin sends an active low, 256-µs pulse to host to report charger device status and fault.
NC	8						**No connect**	
		Optional						Float this pin
/CE	9						**Active low Charge Enable pin**	
		Required						1. /CE pin must be pulled High or Low. 2. Battery charging is enabled when REG01[4] = 1 and CE pin = Low.
BATSNS	10						**Battery voltage sensing pin for charge voltage regulation**	
		Optional					In order to minimize the parasitic trace resistance during charging, BATSNS pin is connected to the positive terminal of battery pack as close as possible	If BATSNS pin is open, BATSNS_STAT bit is set to 1 and charger regulates the battery voltage through BAT pin. If BATSNS is unused, this pin should be floating.
TS	11						**Temperature qualification voltage inputs for JEITA**	
		Optional if TS_IGNORE=1	TS resistors and thermistor				Connect a negative temperature coefficient thermistors. Recommend 103AT-2 thermistors.	 1. If thermistor is not used, set TS pin voltage within normal range or set TS_IGNORE to 1 2. If thermistor is used, program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range.
/QON	12						**BATFET enable/reset control input**	
		Optional			Switch			1.If not used, leave it floating. 2.The pin contains an internal pull-up to maintain default high logic. 3.When BATFET is in ship mode, a logic low of tSHIPMODE duration turns on BATFET to exit ship mode. When the BATFET is not in ship mode, a logic LOW of tQON_RST (minimum 8 s) duration resets SYS (system power) by turning BATFET off for tBATFET_RST (minimum 250ms) and then re-enables BATFET to provide full system power reset. The host chooses the BATFET reset function with VBUS unplugged or not through I2C bit BATFET_RST_WVBUS.
VAC	1						**Charge input voltage sense**	
		Required						Charge input voltage sense. This pin must be connected to VBUS pin.
VBUS	24						**Charge input voltage**	
		Optional	VBUS resistor		10 kΩ			Place a 10 kΩ pulldown resistor from VBUS to GND. This component is recommended for applications that make use of the boost mode (OTG) functionality
		Required	VBUS caps	1uF				1. Place a 1-µF ceramic capacitor from VBUS to PGND and place it as close as possible to IC. 2. It is recommended to have a total of ~10uF capacitance at VBUS & PMID for USB input compliance.
PMID	23						**Actual input source to the charger**	
		Required	PMID caps	8.2uF	10uF			Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Put 10 µF ceramic capacitor on PMID to GND.
		Optional	PMID caps		1nF			For optimal EMC add a 1nF, 0402 capacitor with a minimal loop to GND
BAT	13-14						**Positive battery connection point**	
		Required	BAT caps	10uF	10uF			Battery connection point to the positive terminal of the battery pack. The internal BATFET and current sensing is connected between SYS and BAT. 1. Connect a 10 µF closely to the BAT pin. 2. Charger may operate normally when battery is not connected.

SYS	15-16						**Converter output connection point**	
		Required	SYS caps	10uF	20uF	20uF		Connect a 20 µF closely to the SYS pin. The preferred ceramic capacitor is 10V or higher rating, X7R or X5R.
SW	19-20						**Switching node connecting to output inductor**	
		Required	Output inductor	1uH		2.2uH		Switching node output. Connected to output inductor. The charger device has internal loop compensator.
		Optional	SW Resistor		* Ω		Switching converter snubber circuit	Snubber circuit values empirically determined if required. Recommend unpopulated footprint on new designs.
		Optional	SW Cap		* F			
BTST	21						**PWM high side driver positive supply.**	
		Required	BTST-SW cap	0.047uF	0.047uF	0.047uF		Connect the 0.047µF, 25V rated bootstrap capacitor from SW to BTST.
		Optional	BTST resistor		* Ω		Bootstrap capacitor series snubbing resistor	Helps with EMI performance. Recommend a 0ohm, 0402 on new designs.
REGN	22						**PWM low side driver positive supply output.**	
		Required	REGN cap	4.7uF	4.7uF	4.7uF		Connect a 4.7 µF (10V rating) ceramic capacitor from REGN to analog GND. The capacitor should be placed close to the IC. REGN must serve as the bias rail of the TS pin.
GND	17-18						**Power ground**	
		Required						On the PCB layout, connect the input and output capacitors of the charger directly to GND. A single point connection is recommended between power GND and the analog GND near the IC PGND pin.
Thermal PAD		Required						Thermal pad and ground reference. This pad is ground reference for the device and it is also the thermal pad used to conduct heat from the device. This pad should be tied externally to a ground plane through PCB vias under the pad.