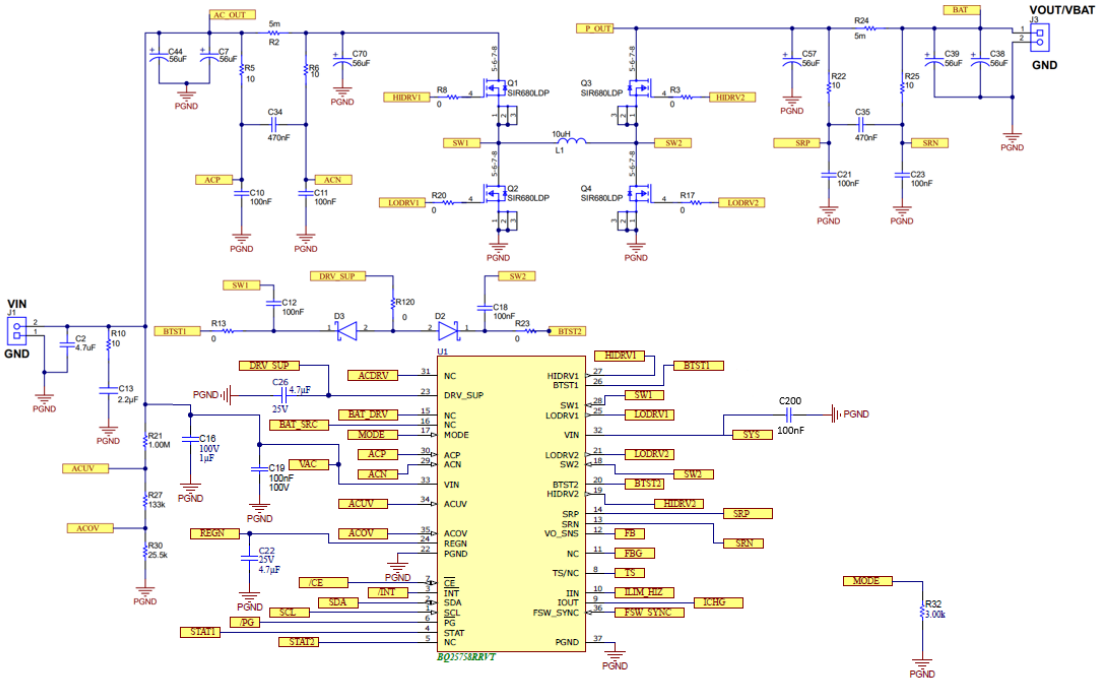
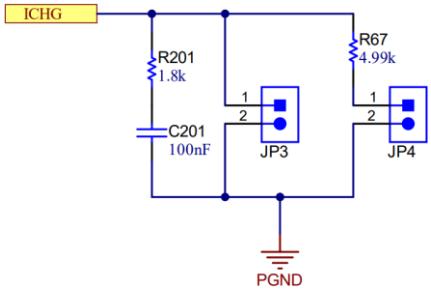
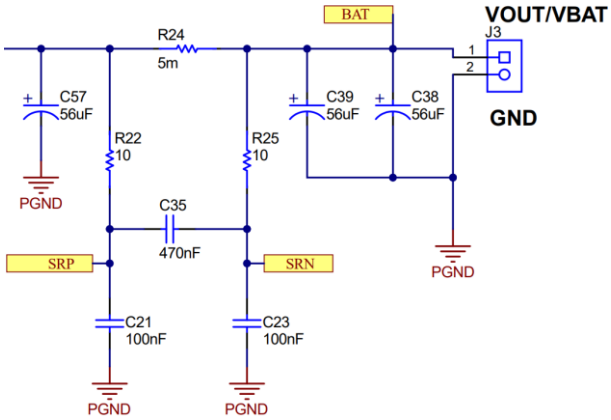
BQ25758 Schematic Checklist

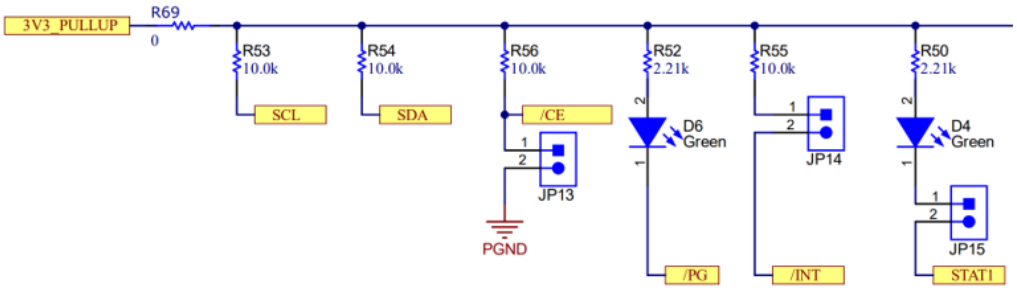


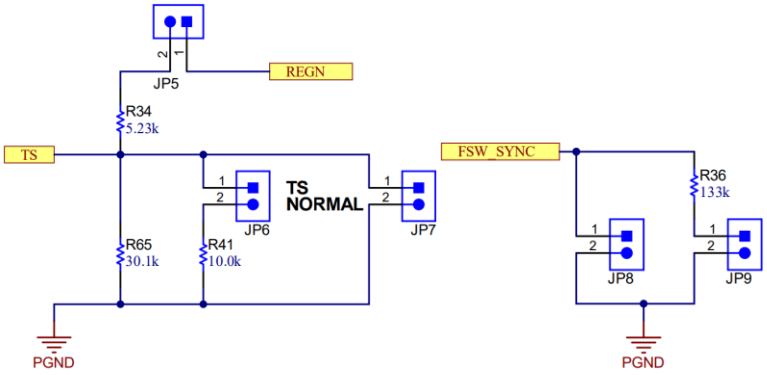
INPUT POWER- DESIGN CHECKLIST								
PIN NAME		REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
		Differential input current sensing and current limit setting						
ACP-ACN, IIN_HIZ	30,29,10	Optional	R2(RAC)	0mΩ		5mΩ	Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecutre of the charger.	R2(RAC) is not required if input current limit functionality is not needed. Short ACP and ACN to VAC if R2(RAC) is not being used.Refer to section **8.2.2.7 Sense Resistor (RAC_SNS and RBAT_SNS) and Current Programming** for choosing the correct resistor value if input current limit functionality is needed.
		Optional	R5,R6		10Ω		Input current sense switching noise and common mode and noise filtering	Can be removed if R2(RAC) is not going to be used.
		Optional	C10,C11		100nF			Can be removed if R2(RAC) is not going to be used.
		Optional	C34		470nF		Differential mode noise filtering	Can be removed if R2(RAC) is not going to be used.
		Optional	R66	0kΩ	2.5kΩ	50kΩ	Resistor to PGND	Refer to section **7.3.4.3.1.1 IIN Pin** of the datasheet for choosing the correct resistor values.
		Required	C44, C7, C70	80uF	160uF		bulk input capacitance	The caps should be a mixture of ceramic and electrolytic. The caps C44, C7 and C70 need to spread and balanced across the sense resistors. The caps don't need to be exact. The ratio between the caps on both sides of the sense resistor can be as great as 1 to 10.
REGN	24	Internal LDO output						
		Required	C22	4.7µF	4.7µF		Internal LDO output stabilizing capacitor	Placed close to the IC REGN pin.
HIDRV1	27	Converter (Forward Buck Mode) High-Side N-Channel MOSFET gate driver						
		Required	Q1				Converter (forward buck mode) active High-Side N-Channel MOSFET	This is also the reverse boost mode synchronous High-Side MOSFET.
		Recommended	RHIDRV1	0Ω			Q1 High-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q1 turn-on and turn-off. Do not add any pull down resistor from the gate to the source of Q1.
LODRV1	25	Converter (Forward Buck Mode) Low-Side N-Channel MOSFET gate driver						
		Required	Q2				Converter (forward buck mode) active Low-Side N-Channel MOSFET	This is also the reverse boost mode synchronous Low-Side MOSFET.
		Recommended	RLORV1	0Ω			Q2 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q2 turn-on and turn-off. Do not add any pull down resistor from the gate to the source of Q2.
SW1-SW2, BTST1, BTST2, DRV-SUP	28-18, 26,20, 23	Buck-boost switching nodes and High-Side MOSFET bootstrap network						
		Required	L1	2.2µH	10µH	15µH	Converter inductor	SW1 and SW2 should be connected to minimize the inductive path from the IC pin to the Inductor
		Required	D2,D3		-		BTST1/BTST2 Diode-OR	BTST diodes should use a Schottky diode to minimize reverse recovery loss
		Required	C26		4.7µF		Connected between DRV-SUP and PGND	
		Required	C12		100nF		Converter bootstrap capacitor for Q1 High-Side N Channel MOSFET gate driver	Capacitor needs to be placed close to the IC.
		Recommended	R13		0Ω		Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q1 turn-on.
		Required	C18		100nF		Converter bootstrap capacitor for Q4 High-Side N Channel MOSFET gate driver	Capacitor needs to be placed close to the IC.
		Recommended	R23		0Ω		Bootstrap capacitor discharge current limiting resistor F	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q4 turn-on.
HIDRV2	19	Converter (Forward Boost Mode) High-Side N-Channel MOSFET gate driver						
		Required	Q3				Converter (forward boost mode) active High-Side N-Channel MOSFET	This is also the reverse buck mode synchronous High-Side MOSFET.
		Recommended	RHIDRV2	0Ω			Q3 High-Side MOSFEt gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q3 turn-on and turn-off. Do not add any pull down resistor from the gate to the source of Q3.
LODRV2	21	Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver						
		Required	Q4				Converter (forward boost mode) active Low-Side N-Channel MOSFET	This is also the reverse buck mode synchronous Low-Side MOSFET.
		Recommended	RLORV2	0Ω			Q4 Low-Side MOSFET gate drive strength limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q4 turn-on and turn-off. Do not add any pull down resistor from the gate to the source of Q4.
ACUV, ACOV	34, 35	Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver						
		Optional	R21		*Ω		Resistor divider from VAC to PGND to program the undervoltage and overvoltage protection.	Refer to section **8.2.1.2.1 ACUV/ACOV Input Voltage Operating Window Programming** of the datasheet for choosing the correct resistor values. Tie ACOV to GND and ACUV to VAC to set the widest operating window
		Optional	R27		*Ω			
		Optional	R30		*Ω			
VAC	33,32	Input Voltage Detection and Power						
		Required	C16		1µF		Input voltage noise decoupling capacitor	Place close to the VAC Pin. Short pin 33 and 32 together.





OUTPUT POWER- DESIGN CHECKLIST								
PIN NAME		REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
					Differential charge current sensing			
SRP,SRN	14,13	Required	R24	-	5mΩ	-	Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecutre of the charger.	The battery sense resistor between SRP and SRN is fixed at 5mΩ. Using a different value is not recommend.
		Required	R22,R25		10Ω		Input current sense switching noise and common mode and noise filtering	
		Required	C21,C23		100nF			
		Required	C35		470nF		Differential mode noise filtering	
		Required	C57,C39, C38	80uF	160uF		bulk output capacitance	The caps should be a mixture of ceramic and electrolytic. The caps C57, C39 and C38 need to spread and balanced across the sense resistors. The caps don't need to be exact. The ratio between the caps on both sides of the sense resistor can be as great as 1 to 10.
					Charge Current Limit setting			
IOUT	9	Optional	R67	0kΩ	5kΩ	100kΩ	Resistor to PGND	Refer to section **7.3.4.2 Charge Current Programming (ICHG pin and ICHG_REG)** of the datasheet for choosing the correct resistor values. This pin can be tied to GND if not used.
					Output voltage			
VO_SNS	12	Required			-		Kelvin connect directly to the output voltage regulation point	





COMMUNICATION AND MISC INPUT/OUTPUT SIGNAL- DESIGN CHECKLIST								
PIN NAME		REQUIREMENTS	Component	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
SCL,SDA	1,2	I2C Open-drain communication input and output						
		Optional	R53,R54		10kΩ		Pullup resistors for the open-drain I2C clock and data communication bus. The pull up voltage can be between 1.8V to 5V	The BQ25756 can operate in standalone by setting the charge current and voltage through external resistor on ICHG and FB, FBG pin. The 10kohm resistor is required if host control configuration is desired
STAT1	4	Open Drain Charge Status Output						
		Optional	R50		2.21KΩ		STAT1 pull up resistor to 3.3V	This pin can be left floating if not used
			D4		-		STAT1 LED Indicator	
/PG or STAT3	6	Open Drain Active Low Power Good Indicator						
		Optional	R52		2.21KΩ		/PG pull up resistor to 3.3V	This pin can be left floating if not used
			D6		-		/PG LED Indicator	
/CE or STAT4	7	Charge Enable pin						
		Required	R56		10kΩ		/CE pull up resistor to 3.3V	/CE must be pulled High or Low, do not leave floating.
TS	8	Battery temperature qualification voltage input						
		Optional	R34		*Ω		Resistor divider from REGN to TS to PGND	TS pin function can be disabled with EN_TS register bit. In this case, the resistor network does not need to be populated
		Optional	R65		*Ω			
		Optional	R41		103AT-2 10 kΩ			
/INT	3	Open Drain Interrupt Output						
		Optional	R55		10kΩ		/INT pull up resistor to 3.3V	This pin can be left floating if not used
FSW_SYNC	36	Switching Frequency and Synchronization Input						
		Required	R36	40kΩ	-	200kΩ	Used to set the nominal switching frequency	A clock can be provided on this pin in the range of 200 – 600kHz for switching frequency synchronization. R36 can also be calculated with the following formula $R_{FSW} = \frac{1}{10 \times \left(f_{SW} \times 5 \times 10^{-12} - 500 \times 10^{-9}\right)}$
MODE	17	Mode programing						
		Required	-		*Ω		Connect a resistor from this pin to GND for mode progaming	Refer to seciton **7.3.3.2** of the datasheet for MODE pin configuraiton
PGND	22	GND						
		Required	-		-		Tie this pin to PGND	
NC PINS	5	NC PINS						
		Required	-		-		Leave this pin NC, do not tie to ground	
	15	Required	-		-		Leave this pin NC, do not tie to ground	
	16	Required	-		-		Leave this pin NC, do not tie to ground	
	31	Required	-		-		Leave this pin NC, do not tie to ground	
PGND	37	Power Ground Return						
		Required	-		-		IC Ground Return	

BQ25758 Layout Guidelines

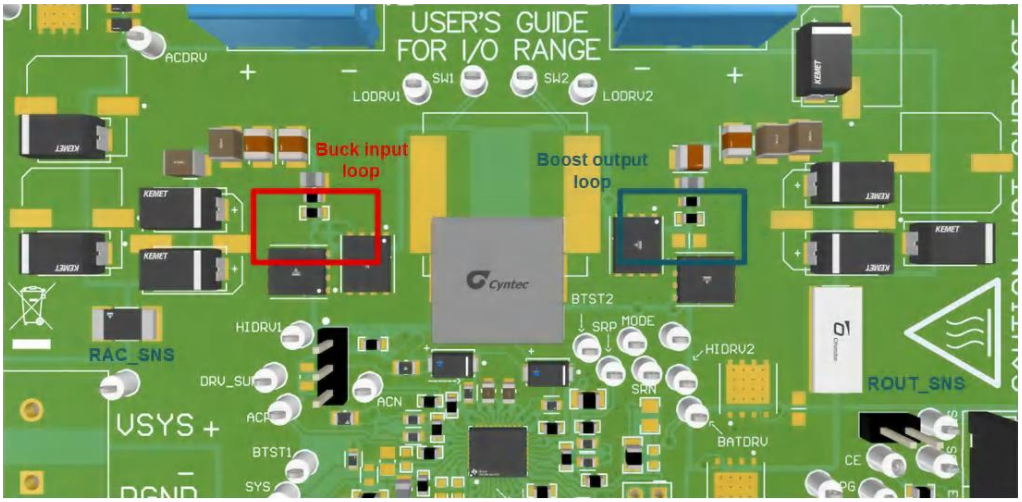
Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout.

Components	Function	Impact	Guidelines
Buck high side FET, Buck low side FET, input capacitors	Buck input loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the input of the buck. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place input ceramic capacitors close to the switching FETs.
Boost low side FET, boost high side FET, output capacitors	Boost output loop	High frequency noise, ripple, efficiency	This path forms a high frequency switching loop due to the pulsating current at the output of the boost. Place components on the same side of the board. Minimize loop area to reduce parasitic inductance. Maximize trace width to reduce parasitic resistance. Place output ceramic capacitors close to the switching FETs.
Sense resistors, Switching FETS, inductor	Current path	Efficiency	The current path from input to output through the power stage and sense resistors have low impedance. Pay attention to via resistance if they are not on the same side. The number of vias can be estimated as 1 to 2-A per via for a 10-mil via with 1oz. copper thickness.
Switching FETs, inductor	Power stage	Thermal, efficiency	The switching FETs and inductor are the components with highest power loss. Allow enough copper area for heat dissipation. Multiple thermal vias can be used to connect more copper layers together and dissipate more heat.
DRV_SUP, BTST1, BTST2, capacitors	Switching FET gate drive	High frequency noise, parasitic ringing, gate drive integrity	The DRV_SUP capacitors are used to supply the power to drive the low side FETs. The BTST capacitors are used to drive the high side FETs. It is recommended to place the capacitors as close as possible to the IC

LODRV1, LODRV2	Low side gate drive	High frequency noise, parasitic ringing, gate drive integrity	LODRV1 and LODRV2 supplies the gate drive current to turn on the low side FETs. The return of LODRV1 and LODRV2 is PGND. As current take the path of least impedance, a ground plane close to the low side gate drive traces is recommended. Minimize gate drive length and aim for at least 20 mil gate drive trace width.
HIDRV1, HIDRV2, SW1 (pin trace), SW2 (pin trace)	High side gate drive	High frequency noise, parasitic ringing, gate drive integrity	HIDRV1 and HIDRV2 supplies the gate drive current to turn on the high side FETs. The return of HIDRV1 and HIDRV2 are SW1 and SW2, respectively. Route HIDRV1/SW1 and HIDRV2/SW2 pair next to each other to reduce gate drive parasitic inductance. Minimize gate drive length and aim for at least 20 mil gate drive trace width.
Current limit resistors, FSW_SYNC resistor	IC programmable settings	Regulation accuracy, Switching integrity	Pin voltage determines the setting for input current limit, output current limit and switching frequency. Ground noise on these could lead to inaccuracy. Minimize ground return from these resistors to the IC ground pin.
Input (ACP, CAN) and output (SRP, SRN) current sense	Current regulation	Regulation accuracy	Use Kelvin-sensing technique for input and output current sense resistors. Connect the current sense traces to the center of the pads, and run current sense traces as differential pairs, away from switching nodes.
Input (ACUV), and output (FB, VO_SNS) voltage sensing	Voltage sense and Regulation	Regulation accuracy	ACUV divider sets internal input voltage regulation in forward mode (V_{ACUV_DPM}). FB divider sets battery voltage regulation in forward mode (V_{FB_ACC}). Route the top of the divider point to the target regulation location Avoid routing close to high power switching nodes.
Bypass capacitors	Noise filter	Noise immunity	Place lowest value cap+B7:D12acitors closest to the IC

Layout Example:

Based on the above layout guidelines, the buck-boost PCB layout example top view is shown below including all the key power components.



For both input and output current sensing resistors, differential sensing and routing method are suggested and highlighted in the Image below. Use wide trace for gate drive traces, minimum 20 mil trace width. Connect all analog grounds to a dedicated low-impedance copper plane, which is tied to the power ground underneath the IC exposed pad.