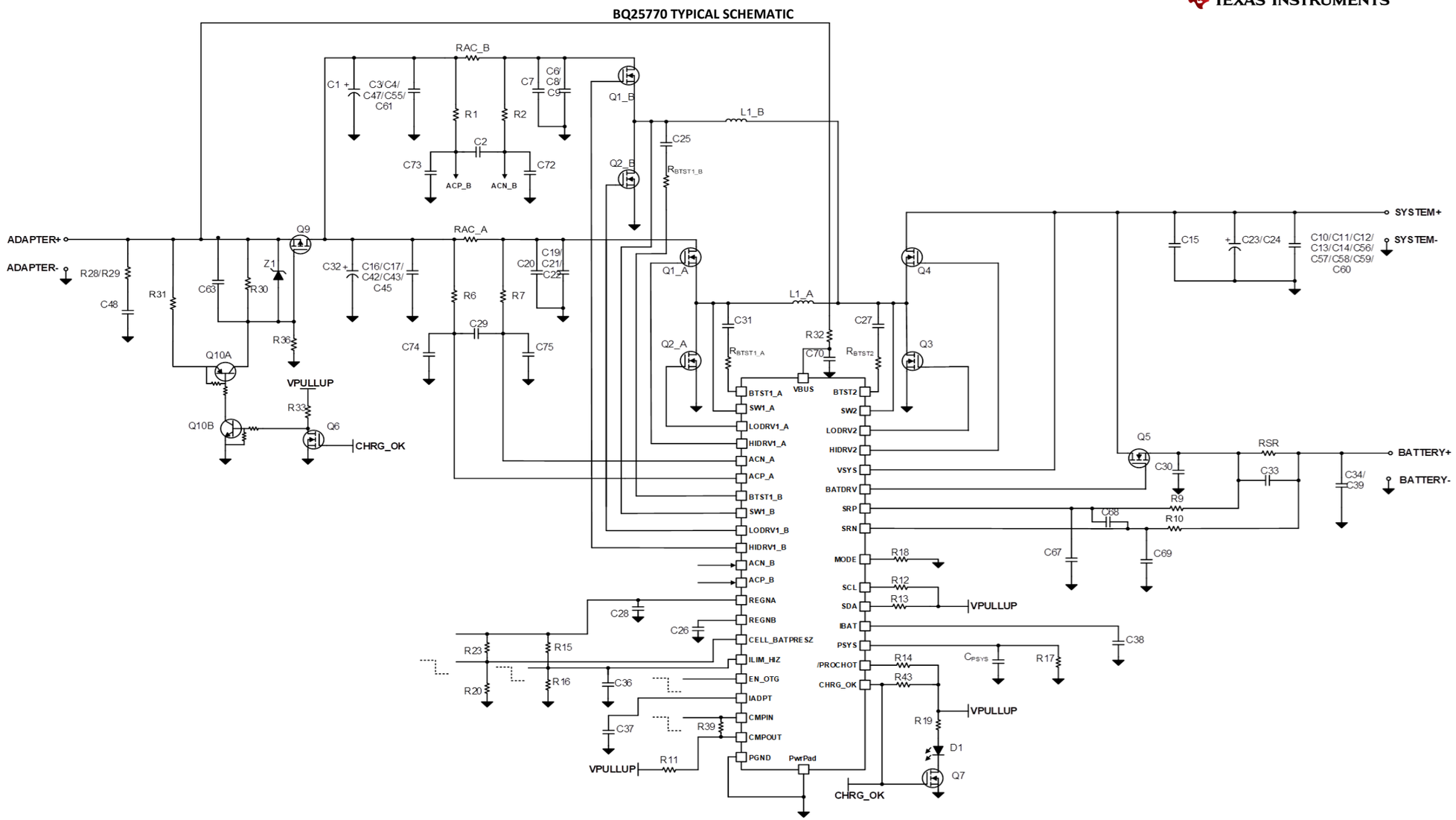
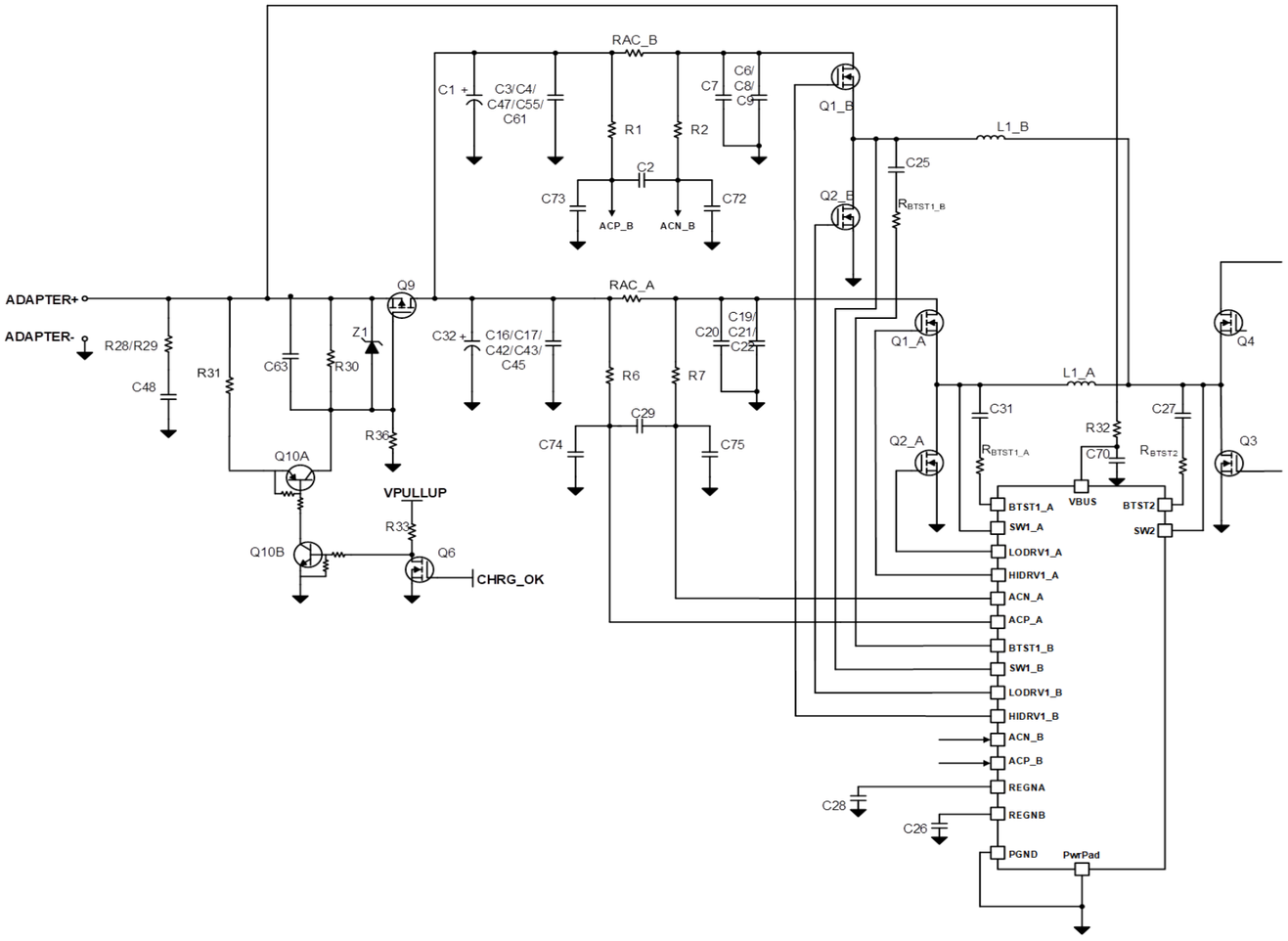
Rev. B Updated: 11/15/2024
unlock sheet with 'bms'

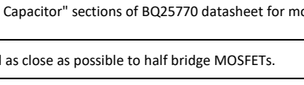
TEXAS INSTRUMENTS

BQ25770 TYPICAL SCHEMATIC



BQ25770 - Input Power Design

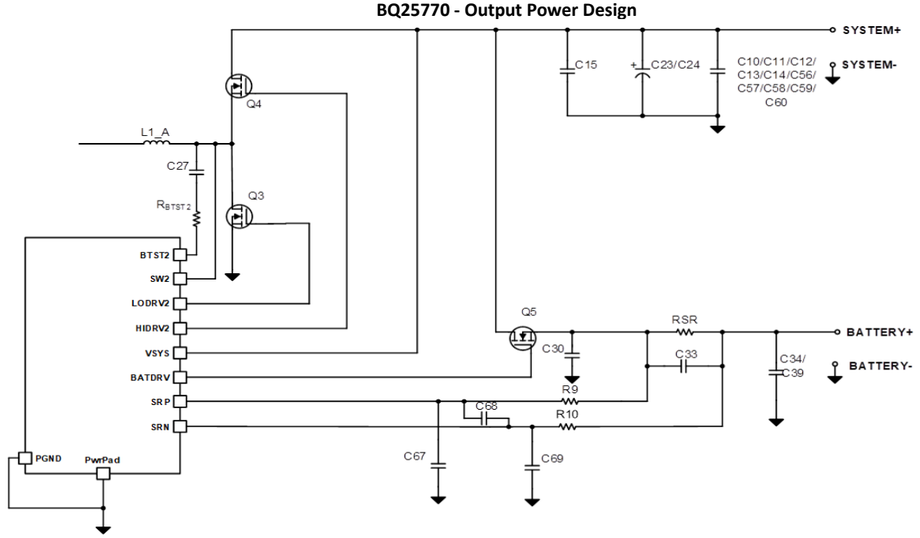


INPUT POWER - DESIGN CHECKLIST								
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
							Input source to the charger	Note:
ADAPTER+ / ADAPTER-	-	Required	C16+C17+C42+C43+C45	20 uF	30 uF		Forward Mode: Ceramic high frequency filtering input capacitors; Reverse Mode: Converter ceramic output filtering capacitors	For a 100W SYS load, use at least (2x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase A) For a 140W SYS load, use at least (3x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase A) For a 180W SYS load, use at least (4x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase A) Refer to "Table 10-2, 10-3, 10-4. Minimum Input Capacitance Requirement" and "10.2.2.3 Input Capacitor" sections of BQ25770 datasheet for more information.
		Required	C3+C4+C47+C55+C61	20 uF	30 uF		Forward Mode: Ceramic high frequency filtering input capacitors; Reverse Mode: Converter ceramic output filtering capacitors	For a 100W SYS load, use at least (2x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase B) For a 140W SYS load, use at least (3x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase B) For a 180W SYS load, use at least (4x) 10 uF capacitors with an extra (1x) 10 uF DNP. (Phase B) Refer to "Table 10-2, 10-3, 10-4. Minimum Input Capacitance Requirement" and "10.2.2.3 Input Capacitor" sections of BQ25770 datasheet for more information.
		Required	C1+C32		33 uF		Forward Mode: Tantalum polymer high frequency filtering input capacitor; Reverse Mode: Converter tantalum polymer output filtering capacitor	For 28V and 36V input, use at least (1x) 33 uF tantalum polymer capacitor. (Phase A+Phase B) Refer to "Table 10-2, 10-3, 10-4. Minimum Input Capacitance Requirement" and "10.2.2.3 Input Capacitor" sections of BQ25770 datasheet for more information. Note: If there is a ferrite bead or filter inductor before the input caps, minimum 22uF polymer cap is required.
		Required	C20		10 uF		Forward Mode: Ceramic high frequency filtering input capacitors; Reverse Mode: Converter ceramic output filtering capacitors	Total input capacitance should meet minimum requirement. Refer to "Table 10-2, 10-3, 10-4. Minimum Input Capacitance Requirement" and "10.2.2.3 Input Capacitor" sections of BQ25770 datasheet for more information.
		Required	C19+C21+C22		10nF+1nF		EMI filter caps	1*10nF+1nF 0402 package MLCC capacitors (EMI filter purpose) are recommended to be placed as close as possible to half bridge MOSFETs.
		Required	C7		10 uF		Forward Mode: Ceramic high frequency filtering input capacitors; Reverse Mode: Converter ceramic output filtering capacitors	Total input capacitance should meet minimum requirement. Refer to "Table 10-2, 10-3, 10-4. Minimum Input Capacitance Requirement" and "10.2.2.3 Input Capacitor" sections of BQ25770 datasheet for more information.
		Required	C6+C8+C9		10nF+1nF		EMI filter caps	1*10nF+1nF 0402 package MLCC capacitors (EMI filter purpose) are recommended to be placed as close as possible to half bridge MOSFETs.
		Recommended-DNP	R28, R29		3.9 Ω		Input hot-plug snubber circuit	For systems with high input cable or trace inductance and hot plug use cases, add experimentally derived RC snubber to limit inrush current and input voltage overshoot. R28 and R29 in parallel should be sized appropriately to handle the inrush current.
			C48		1 uF			
		Optional	Q9				ACFET (P-Ch. MOSFETs)	Size Q9 appropriately to handle input power, optimize losses, and allow for smooth turn-on and turn off. Select delay and control circuits to avoid conflicts with charger timing. **Note**: If the Q9 input protection circuit is in place, R32 (*See VBUS*) must be connected to the Source of Q9.
		Optional	R36				Input protection turn-on/turn-off delay	
			R30					
			C63					
		Optional	R31				Input protection turn-on/turn-off control	
			Q10A/Q10B					
			Q6					
			R33		10 kΩ			
		Optional	Z1				Input protection gate-source Zener clamping diode	Size to clamp maximum allowable VGS for Q9.
							Differential input current sensing	
ACPx-ACNx	10-9, 8-7	Required	RAC_A, RAC_B	5 mΩ	10 mΩ		Input current sensing resistor. This is used for both input current limit regulation and for inductor current sensing of the average current mode control architecutre of the charger.	This will impact the IADPT and PSYS pin measurements. In IINDPM regulation, the input current limit is regulated as a differential voltage across R_{AC}, such that: $V_{RAC} = R_{AC}$ x Minimum{ IIN_HOST() Register Setting, ILIM_HIZ pin setting } (appliable in typical applications).
		Required	R1, R2, R6, R7		4.99 Ω		Input current sense switching noise and common mode noise filtering	Select R6 / C74 and R7 / C75 such that the filter time constant is between 47 ns and 200 ns
			C72, C73, C74, C75		33 nF			
		Recommended	C2, C29		0.1 uF		Differential mode noise filtering	
							IC input voltage rail	
VBUS	6	Required	C70	0.47 uF	0.47 uF		Input voltage noise decoupling capacitor	Placed close to the IC VBUS pin. X7R capacitor is recommended.
		Recommended	R32		1 Ω		Input voltage rail inrush current limiting	Size appropriately to handle large input overshoots and current spikes. 
							Internal LDO output	
REGN_A, REGN_B	2, 32	Required	C26, C28	2.2 uF	2.2 uF		Internal LDO output stabilizing capacitor	Placed close to the IC REGN pin. X7R capacitor is recommended. REGN_A is internally connected to REGN_B. Special Note: When charging without a battery, suggest adding a diode + resistor pair to prebias VBAT rail from REGNA.

HIDRV1_A, HIDRV1_B	4, 35	**Converter (Forward Buck Mode) High-Side N-Channel MOSFET gate driver**					
		Required	Q1_A, Q1_B			Converter (forward buck mode) active High-Side N-Channel MOSFET	This is also the reverse boost mode synchronous High-Side MOSFET. Refer to "Typical Application" section of the datasheet for more details on the Power Stage MOSFET selection criterion.
LODRV1_A, LODRV1_B	1, 33	**Converter (Forward Buck Mode) Low-Side N-Channel MOSFET gate driver**					
		Required	Q2_A, Q2_B			Converter (forward buck mode) synchronous Low-Side N-Channel MOSFET	This is also the reverse boost mode active Low-Side MOSFET. Refer to "Typical Application" section of the datasheet for more details on the Power Stage MOSFET selection criterion.
SW1_A, SW1_B, SW2, BTST1_A, BTST1_B, BTST2	5, 36, 28, 3, 34, 30	**Buck-boost switching nodes and High-Side MOSFET bootstrap network**					
		Required	refer to EVM			Converter inductor	SW1 _A, SW1_B and SW2 should be connected to minimize the inductive path from the IC pin to the inductors L1_A and L1_B. Refer to EVM
		Required	C31, C25		100 nF	Converter bootstrap capacitor for Q1_A/Q1_B High-Side N-Channel MOSFET gate driver	
		Recommended	R_{BTST1}	0 Ω		Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q1 _A/Q1_B turn-on.
		Required	C27		100 nF	Converter bootstrap capacitor for Q4 High-Side N-Channel MOSFET gate driver	
		Recommended	R_{BTST2}	0 Ω		Bootstrap capacitor discharge current limiting resistor	For non-ideal layouts with EMI contraints, add an experimentally derived resistance to slow down the Q4 turn-on.
HIDRV2	29	**Converter (Forward Boost Mode) High-Side N-Channel MOSFET gate driver**					
		Required	Q4			Converter (forward boost mode) synchronous High-Side N-Channel MOSFET	This is also the reverse buck mode High-Side MOSFET. Refer to "Typical Application" section of the datasheet for more details on the Power Stage MOSFET selection criterion.
LODRV2	31	**Converter (Forward Boost Mode) Low-Side N-Channel MOSFET gate driver**					
		Required	Q3			Converter (forward boost mode) active Low-Side N-Channel MOSFET	This is also the reverse buck mode Low-Side MOSFET. Refer to "Typical Application" section of the datasheet for more details on the Power Stage MOSFET selection criterion.

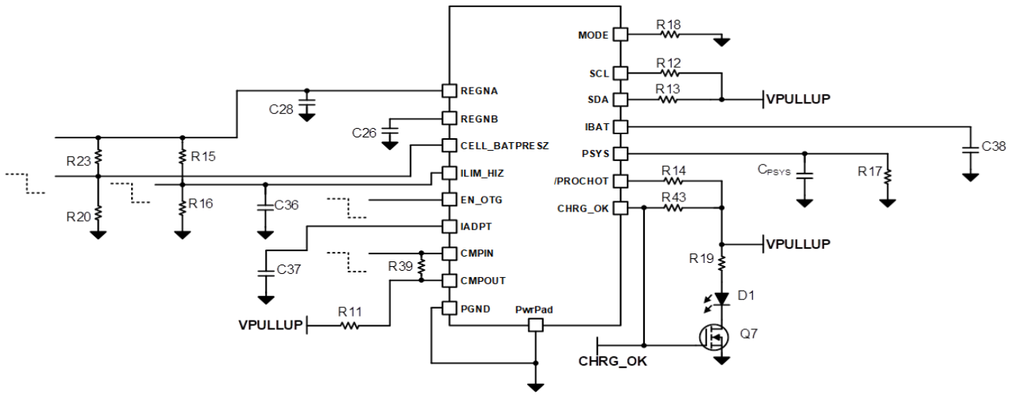
	VBUS = 20 V	VBUS = 28 V	VBUS = 36 V
Fsw=600 kHz	2.2 µH	2.2 µH	3.3 µH
Fsw=800 kHz	1.5 µH	1.5 µH	2.2 µH

BQ25770 - Output Power Design



OUTPUT POWER - DESIGN CHECKLIST								
PIN NAME		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
		System output either from converter regulation of input source or battery						
SYSTEM+ / SYSTEM-	-	Required	C10+C11+C12+C13+C14+C56+C57+C58+C59+C60 ($C_{SYSTEM+}$)	70 uF	90 uF		Forward Mode: Converter ceramic output filtering capacitors; Reverse Mode: Ceramic high frequency filtering input capacitors	For a 100W SYS load, use at least (7x) 10 uF capacitors with an extra (2x) 10 uF DNP. For a 140 W to 180 W SYS load, use at least (9x) 10 uF capacitors with an extra (2x) 10 uF DNP. X7R capacitors are recommended. Refer to "Table 10-5. Minimum Output Capacitance Requirement" and "10.2.2.4 Output Capacitor" sections of BQ25770 datasheet for more information. These caps can be placed at next stage converter input terminal not need to be at charger output terminals.
		Required	C23+C24 ($C_{SYSTEM+}$)	33 uF	66 uF		Forward Mode:Converter tantalum polymer output filtering capacitors; Reverse Mode: Tantalum polymer high frequency filtering input capacitor	For 100W SYS loads, use at least (1x) 33 uF tantalum polymer capacitor. For 140W to 180W SYS loads, use at least (2x) 33 uF tantalum polymer capacitors. Refer to "Table 10-5. Minimum Output Capacitance Requirement" and "10.2.2.4 Output Capacitor" sections of BQ25770 datasheet for more information. These caps can be placed at next stage converter input terminal not need to be at charger output terminals.
		System output regulation sensing point						
VSYS	27	Required	-		-		-	VSYS must be Kelvin connected to the output filter stage connected to SYSTEM+. The connection should be tied as close the output resonant filter portion of the system rail ($C_{SYSTEM+}$) as possible. Take precaution to not Kelvin connect this pin significantly far away from the output filter and/or IC SYS pin, such that a large IR loss from the system load is sensed by VSYS.
		Battery or battery pack connection to the charger						
BATTERY+ / BATTERY-	-	Required	C34, C39	20 uF	Refer to device EVM		Charge current regulation stability and filtering capacitor	Connected to the SRN pin, this capacitor is critical for accurate battery voltage sensing. From the SRN pin, the Constant Voltage (CV) phase of charging will regulate the voltage to the MaxChargeVoltage() Register setting. When charging is disabled and the SRN voltage is above the MinSysVoltage() Register setting, the sensed voltage on the SRN pin is also used as a reference to regulate the SYS pin voltage such that: **$V_{VSYS} = V_{SRN}$ + 160 mV / 150 mV .** X7R capacitor is recommended.
		Differential charge current sensing						
SRP-SRN	25-24	Required	RSR	2mΩ	5 mΩ	5 mΩ	Charge current sensing resistor	This will impact the IBAT and PSYS pin measurements. In Charge Current regulation for the Constant Current (CC) phase of charging, the ICHG current is regulated as a differential voltage across R_{SR}, such that " **$V_{RSR} = R_{SR}$ x ChargeCurrent() Register setting "**. If the charger is either in IINDPM, VINDPM, or other protections, the regulated charge current may be lower than the programmed value.
		Required	C30	1 uF	1 uF		Noise filter capacitor	
		Required	C33		0.1 uF		Differential mode noise filtering	
		Required	R9, R10		10 Ω	10 Ω	Battery reverse polarity protection resistors	Sized with a low power rating such that in the event of a reverse polarity event with the battery pack, the resulting unintended current flow will damage R9 or R10 first rather than the charger or the system. This acts as a crude form of reverse polarity protection.
		Recommended-DNP	C67, C68, C69				Noise filter capacitor	These noise filtering caps are reserved for charger operating in boost mode.
		External battery MOSFET driver						
BATDRV	26	Required	Q5		-		External battery to system power path N-Channel MOSFET (BATFET)	Note that BATFET is N-FET.

BQ25770 other pins



BQ25770 other pins - DESIGN CHECKLIST

PIN		REQUIREMENT	COMPONENT	MIN	TYP	MAX	DESCRIPTION	COMMENTS AND RELEVANT EQUATIONS
								Default charging and system parameter setting
CELL_BATPRESZ	23	Required	R23		*kΩ		Resistor divider network referenced to the REGN_A rail to set the default charging voltage, default minimum system voltage, and maximum system voltage. Also input to signal charger of a battery absense.	The CELL_BATPRESZ cell count settings is determined once REGN_A is powered, typically after a valid input source is applied. If CELL_BATPRESZ is pulled LOW externally, this indicates to the charger that the battery has been removed. This will reset the ChargeCurrent() Register setting to 0mA. If enabled in the ProchotOption1() Register setting, this will also trigger the ProchotStatus() register flag.
			R20		*kΩ			
								External input current limit setting and converter high impedance control
ILIM_HIZ	13	Required	R15		*kΩ		Resistor divider network to set an external input current limit.	The voltage set at this pin through the resistor divider network determines the externally set input current limit setting.
			R16		*kΩ			$V_{ILIM} = 1V + 40 \times IINDPM \times R_{AC}$
		Recommended-DNP	C36		*uF		Noise decoupling capacitor	Place close to the IC ILIM_HIZ pin.
								Input current measurement output
IADPT	14	Optional	C36		100 pF		Noise decoupling capacitor	Place close to the IC IADPT pin.
								OTG enable
EN_OTG	12	Optional	-		-		Enable OTG mode	Pull HIGH to enable OTG mode.
								Programmable PWM switching frequency and compensation level
MODE	16	Required	R18	-2%	*kΩ	+2%	Resistor used to program the PWM switching frequency and compensation level	Please refer to "Table 9-1 Mode pin programming table" of the BQ25770 datasheet for details.
								Independent comparator input and output
CMPIN, CMPOUT	22, 21	Optional	R11		10 kΩ		Pullup resistor for CMPOUT open-drain output	
			R39				Refer to datasheet and EVM	
								I2C or SMBus Open-drain communication input and output
SCL, SDA	20, 19	Required	R13, R12		10 kΩ		Pullup resistors for the open-drain I2C or SMBus clock and data communication bus	I2C or SMBus communication is required for charging to operate on this device as intended. This is a host controlled charging buck-boost controller. Charging is not autonomous without host intervention.
								Analog battery current measurement output
IBAT	15	Optional	C38		100 pF		Analog voltage output representing the battery charge or discharge current measurement	Place close to the IC IBAT pin. The IBAT_GAIN setting is programmable in the ChargeOption0() Register.
								Analog system power measurement output
PSYS	17	Optional	R17		15 kΩ		Analog current output representing the system power, measured as a voltage across R17.	Note that the max PSYS output current is 260uA, max PSYS output voltage is 3.3V. Choose PSYS_RATIO=0.25uA/W for PSYS>260W.
		Optional	C_{PSYS}		100 pF		Noise decoupling capacitor	Place close to the IC PSYS pin.
								Active LOW open-drain output signal for Proccessor Hot flags
/PROCHOT	18	Optional	R14		10 kΩ		Pullup resistor for/PROCHOT open-drain output	
								Active HIGH open-drain output signal of input source status
CHRG_OK	11	Optional	R43				Pullup resistor for CHRG_OK open-drain output	Open drain active high indicator to inform the system good power source is connected to the charger input. Connect to the pullup rail via 10-kΩ resistor.
		Optional	R19				CHRG_OK LED indictation control	
			D1					
			Q7					
								IC Thermal dissipation pad
PwrPad	37	Required	-		-		Main point of heat dissipation for the IC	Connect to a large Power Ground plane(s) and/or layer(s) with at least 5-point via connections

R15 (TOP)	R16 (BOT)	VILIM (V)	ILIM@10mohm
200k	300k	3	5A
133K	113K	2.3	3.25A
140K	110K	2.2	3A
243K	115K	1.6	1.5A
93.1K	29.4K	1.2	0.5A

R23	R20	%of REGNA	Cell Setting
150k	100k	40	2S
82k	100k	55	3S
33k	100k	75	4S
1k	100k	100	5S

Table 9-1. MODE Pin Programming Table

MODE_STAT BIT	MINIMUM RESISTANCE	TYPICAL RESISTANCE	MAXIMUM RESISTANCE	TOPOLOGY	COMPENSATION ADJUSTMENT	PWM_FREQ BIT
000b	0 kΩ	3.57 kΩ	3.79 kΩ	Quasi dual phase buck-boost	Normal	1b (600 kHz)
001b	4.42 kΩ	4.64 kΩ	4.87 kΩ	Quasi dual phase buck-boost	Normal	0b (800 kHz)
010b	5.76 kΩ	6.04 kΩ	6.34 kΩ	Quasi dual phase buck-boost	Slow	1b (600 kHz)
011b	7.87 kΩ	8.25 kΩ	8.66 kΩ	Quasi dual phase buck-boost	Slow	0b (800 kHz)
High Fault (000b)	47.5 kΩ	--	Open circuit	Quasi dual phase buck-boost	Normal	1b (600 kHz)