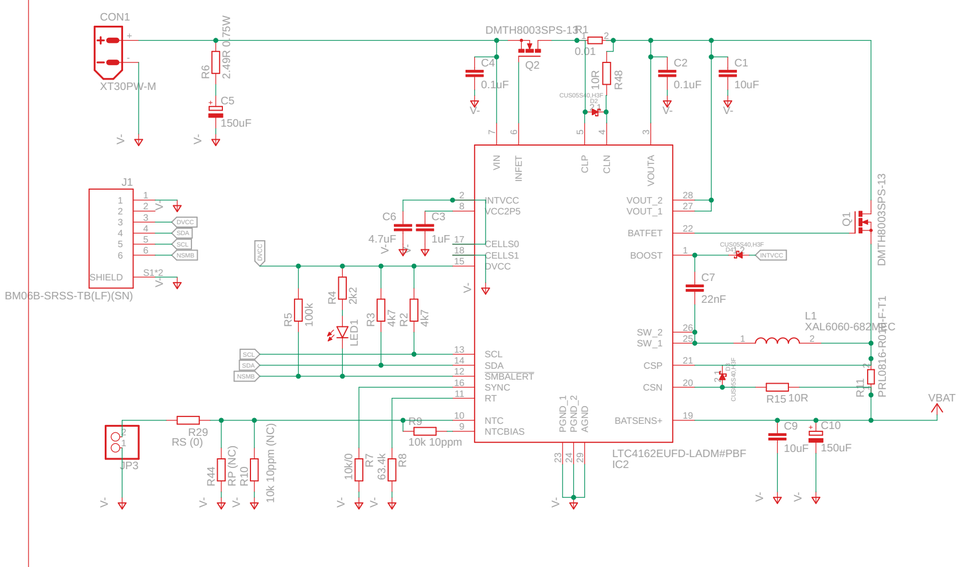
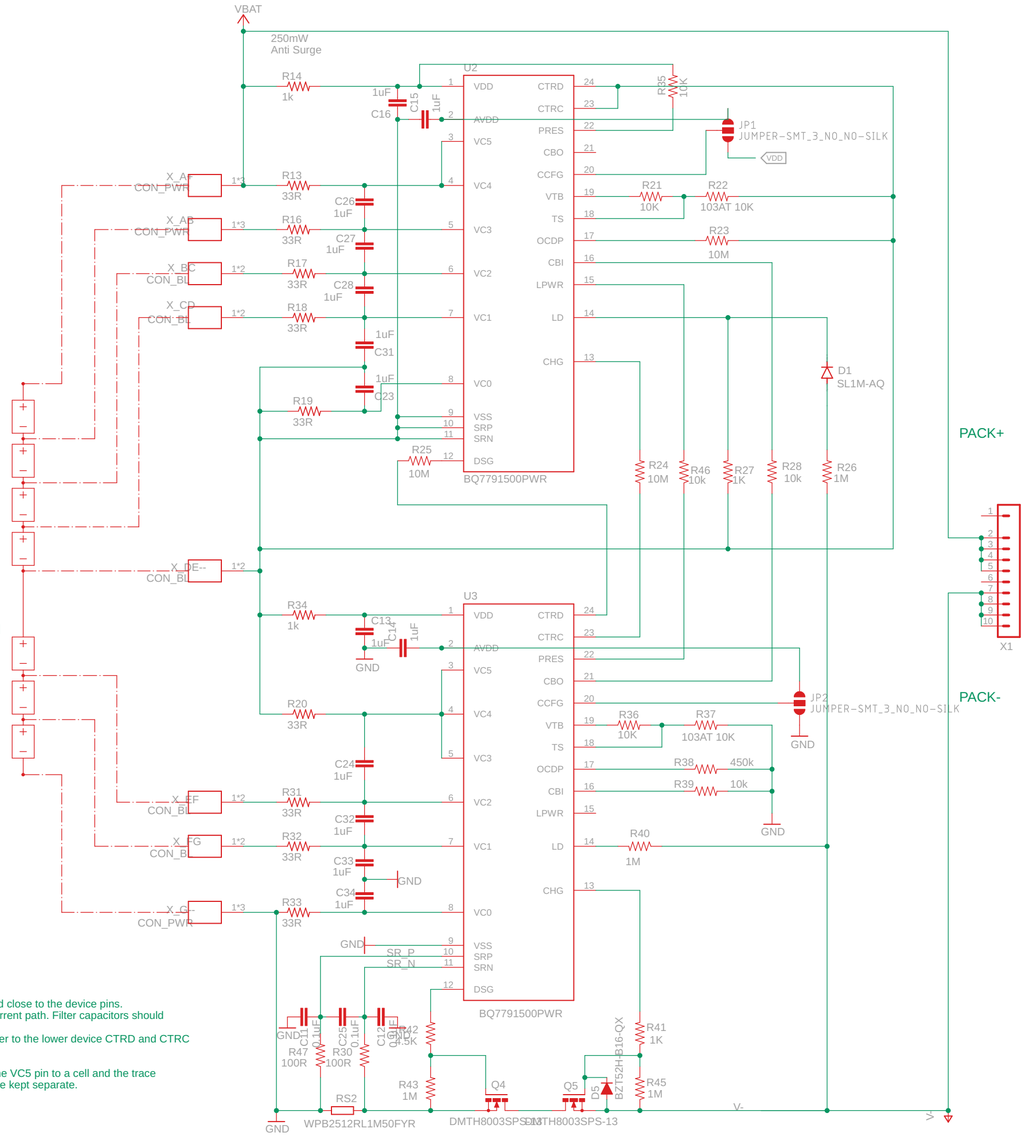



Hinweis Datenblatt:
Verify each device's CCFG pin is configured appropriately
for its specific number of cells (that is, three, four, or five cells).




Hinweis, Datenblatt:
Connect a higher cell count to the upper devices
(for example, for a 7-series configuration, connect
four cells on the upper device and three cells on the
bottom device). This provides a stronger CTRx signal
to the bottom device.

Layout Guidelines
1. Match SRN and SRP traces.
2. RIN filters, VDD, AVDD filters, and the CVDD capacitor should be placed close to the device pins.
3. Separate the device ground plane (low current ground) from the high current path. Filter capacitors should reference to the low current ground path or device Vss.
4. In a stack configuration, the RCTRD and RCTRC should be placed closer to the lower device CTRD and CTRC pins.
5. RGS should be placed near the FETs.
6. In a stacked configuration, verify in the PCB layout that the trace from the VC5 pin to a cell and the trace from the VC0 pin of the next upper device to the immediately higher cell are kept separate.