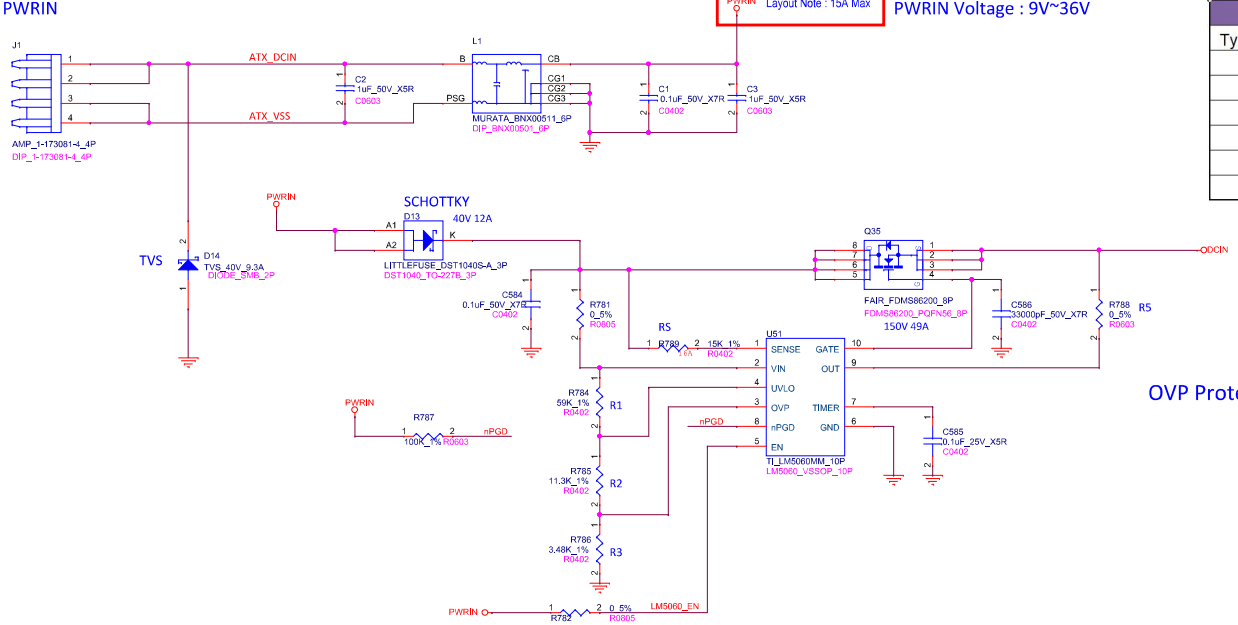
PWRIN

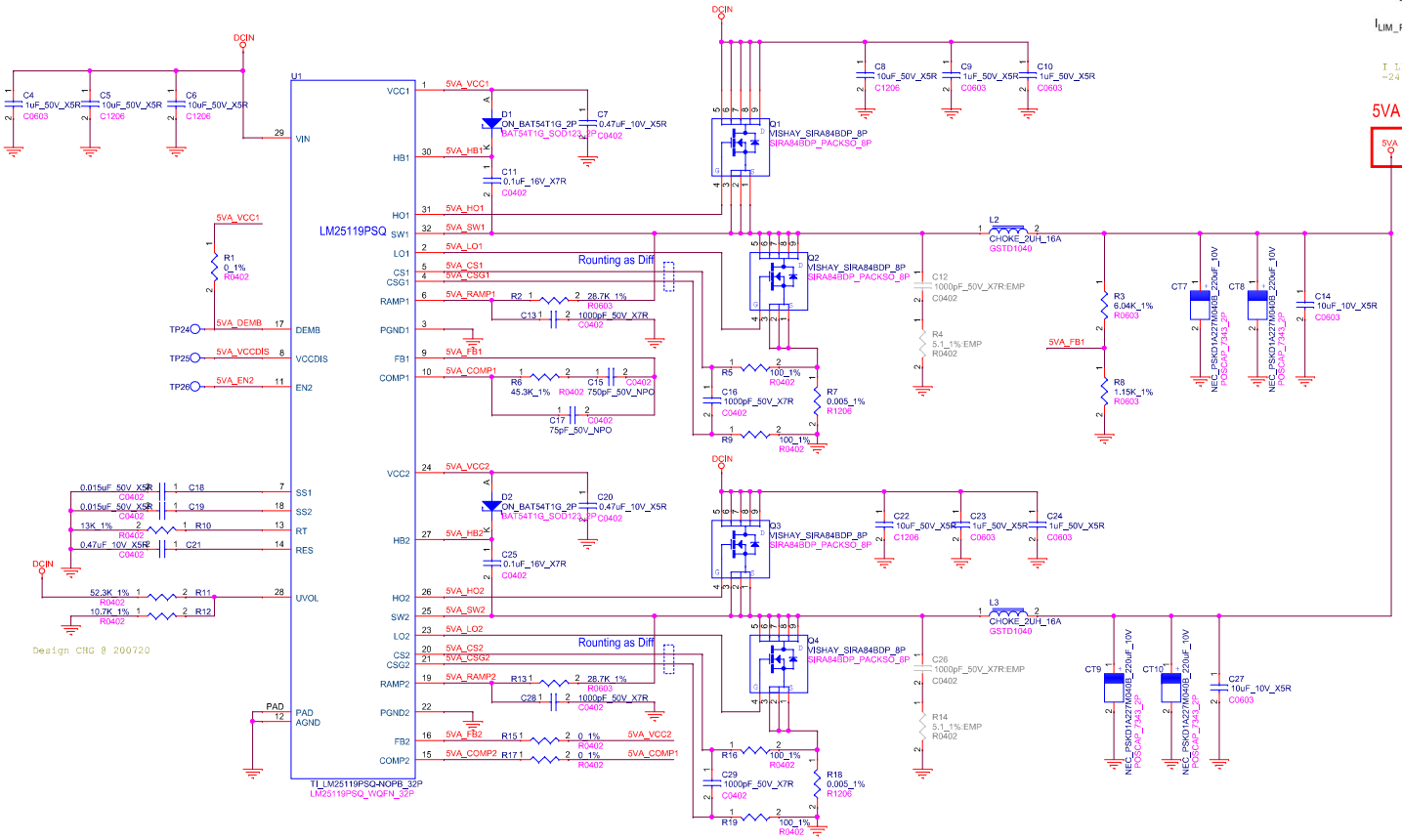
PWRIN Layout Note : 15A Max

PWRIN Voltage : 9V~36V

	Settings	Units
Typical Over-Current Threshold	16.00	A
Startup Delay Time	33.33	ms
Over-Current Fault Delay	18.18	ms
Upper OVLO Threshold	42.73	V
Lower OVLO Threshold	37.64	V
Upper UVLO Threshold	8.31	V
Lower UVLO Threshold	7.59	V

R1 =	59	kΩ
R2 =	11.30	kΩ
R3 =	3.48	kΩ
Rs =	15.00	kΩ
R5=	0	kΩ
C_{Timer} =	100.00	nF
C_{in} =	100	nF
C_{Gate} =	31	nF
C_{Load} =	220	µF





$$I_{LIM\_PEAK} = \frac{V_{CS(TH)}}{R_S} + \frac{V_{IN(MAX)} t_{ON(MIN)}}{L}$$

where

- $t_{ON(MIN)}$ is the minimum HO on-time which is nominally 100 ns

$$I_{LIM\_PEAK} = \frac{0.12}{0.008\Omega} + \frac{36\ V \times 100\ ns}{6.8\ \mu H} = 15.53A$$

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I_LIM_PEAK= (0.12/0.005R)+(36*(100/10^-9))/(6.8*10^-6)
=24.18A
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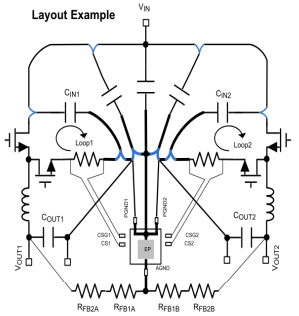
5VA

5VA Layout Note : 30A Max

Layout Example



The bold lines indicate a solid ground plane. Make the traces to the widest and the shortest and use the star ground technique.

These lines indicate the high current paths. Make the traces as wide and short as possible

These lines indicate the small signal paths. The traces can be narrow but keep them away from any radiated noise and away from traces that may couple noise capacitively

These points require the maximum bypassing of the high frequency switching noise. Isolate each channel from the high frequency switching noise of the other channel.

Figure 23. Recommended PCB Layout

Yamashita Systems R&D Center

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