GENERAL DESCRIPTION

The CM6803 is a 8-pin Green PFC/PWM controller for power factor corrected, switched mode power supplies that offers very low start-up and operating currents. For the power supply less than 500Watt, its input current shaping PFC performance could be very close to CM6800 or ML4800 architecture.

Power Factor Correction (PFC) offers the use of smaller, lower cost bulk capacitors, reduces power line loading and stress on the switching FETs, and results in a power supply fully compliant to IEC1000-3-2 specifications. The CM6803 includes circuits for the implementation of a leading edge, input current shaping technique "boost" type PFC and a trailing edge, PWM.

The CM6803's PFC and PWM operate at the same frequency, 67kHz. An PFC OVP comparator shuts down the PFC section in the event of a sudden decrease in load. The PFC section also includes peak current limiting for enhanced system reliability.

Both PFC and PWM have the Green Mode Functions. PFC Green Mode cannot be disabled by the design. PWM Green Mode will happen when the PWMCMP (PWM Comparator) Duty Cycle is less than ~ 6%, in the next cycle, the PWMOUT pulse will be removed until PWMCMP Duty Cycle is greater than 6%, then the next cycle, PWMOUT pulse appears.

FEATURES

- Patent Filed #5,565,761, #5,747,977, #5,742,151, #5,804,950, #5,798,635
- Both PFC and PWM have the Green Mode to meet blue angel and energy star spec.
- 8-Pin SOIC package
- PWM pulse skipping for the green mode
- It can use the HV bipolar to start up the chip and it help green mode.
- Enable lowest BOM for power supply with PFC
- Internally synchronized PFC and PWM in one IC
- Patented slew rate enhanced voltage error amplifier with advanced input current shaping technique
- Universal Line Input Voltage
- CCM boost or DCM boost with leading edge modulation PFC using Input Current Shaping Technique
- PFCOVP, VCCOVP, Precision -1V PFC ILIMIT, Tri-Fault Detect comparator to meet UL1950
- No bleed resistor required
- Low supply currents; start-up: 100uA typical, operating current: 2mA typical.
- Synchronized leading PFC and trailing edge modulation PWM to reduce ripple current in the storage capacitor between the PFC and PWM sections and to reduce switching noise in the system
- VINOK Comparator to guarantee to enable PWM when PFC reach steady state
- High efficiency trailing-edge current mode PWM
- UVLO, REFOK, and brownout protection
- Digital PWM softstart
- Precision PWM 1.5V current limit for current mode operation

24 Hours Technical Support---WebSIM

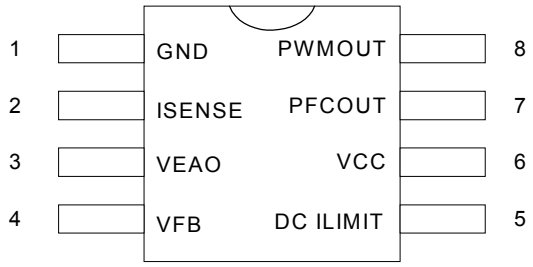
Champion provides customers an online circuit simulation tool called WebSIM. You could simply logon our website at www.champion-micro.com for details.

APPLICATIONS

- Desktop PC Power Supply
- AC Adaptor
- Internet Server Power Supply
- IPC Power Supply
- UPS
- Battery Charger
- DC Motor Power Supply
- Monitor Power Supply
- Telecom System Power Supply
- Distributed Power

PIN CONFIGURATION

PSOP-8 (PS08)
Top View



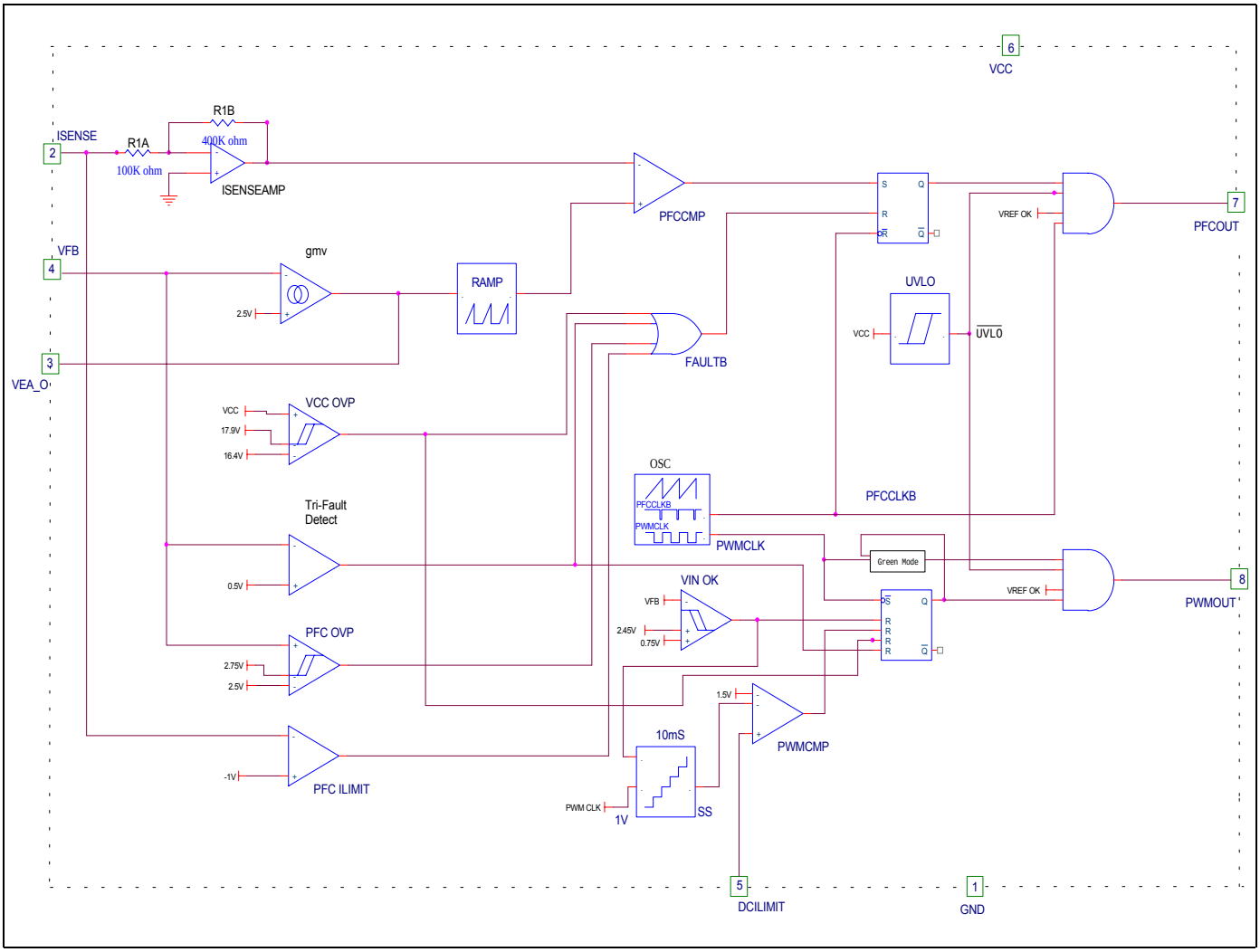
PIN DESCRIPTION

Pin No.	Symbol	Description	Operating Voltage			
			Min.	Typ.	Max.	Unit
1	GND	Ground				
2	I_{SENSE}	Current sense input to the PFC current limit comparator	-5		0.7	V
3	VEAO	PFC transconductance voltage error amplifier output	0		6	V
4	V_{FB}	PFC transconductance voltage error amplifier input	0	2.5	3	V
5	DC I_{LIMIT}	PWM current limit comparator input	0		1.5	V
6	V_{CC}	Positive supply	10	15	20	V
7	PFC OUT	PFC driver output	0		VCC	V
8	PWM OUT	PWM driver output	0		VCC	V

ORDERING INFORMATION

Part Number	Temperature Range	Package
CM6803IS	-40℃ to 125℃	8-Pin PSOP (PS10)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum ratings are those values beyond which the device could be permanently damaged.

Parameter	Min.	Max.	Units
V_{CC} MAX		20	V
I_{SENSE} Voltage	-5	0.7	V
PFC OUT	GND – 0.3	VCC + 0.3	V
PWM OUT	GND – 0.3	VCC + 0.3	V
VEAO	0	6.3	V
Voltage on Any Other Pin	GND – 0.3	VREF + 0.3	V
I_{CC} Current (Average)		40	mA
Peak PFC OUT Current, Source or Sink		0.5	A
Peak PWM OUT Current, Source or Sink		0.5	A
PFC OUT, PWM OUT Energy Per Cycle		1.5	μJ
Junction Temperature		150	℃
Storage Temperature Range	-65	150	℃
Operating Temperature Range	-40	125	℃
Lead Temperature (Soldering, 10 sec)		260	℃
Thermal Resistance (θ_{JA})		80	℃/W

ELECTRICAL CHARACTERISTICS **Unless otherwise stated, these specifications apply Vcc=+15V, T_A=Operating Temperature Range (Note 1)**

Symbol	Parameter	Test Conditions	CM6803			Unit
			Min.	Typ.	Max.	
Voltage Error Amplifier (g_{mv})						
	Input Voltage Range		0		5	V
	Transconductance	V_{NONINV} = V_{INV}, VEAO = 3.75V	30	65	90	µmho
	Feedback Reference Voltage		2.45	2.5	2.55	V
	Input Bias Current	Note 2		-0.5	-1.0	µA
	Output High Voltage		5.8	6.0		V
	Output Low Voltage			0.1	0.4	V
	Sink Current	V_{FB} = 3V, VEAO = 6V	-20	-35		µA
	Source Current	V_{FB} = 1.5V, VEAO = 1.5V	30	40		µA
	Open Loop Gain		50	60		dB
	Power Supply Rejection Ratio	11V < V_{CC} < 16.5V	50	60		dB
VCC OVP Comparator						
	Threshold Voltage		17.4	17.9	18.4	V
	Hysteresis		1.4	1.5	1.65	V
PFC OVP Comparator						
	Threshold Voltage		2.70	2.77	2.85	V
	Hysteresis		230		290	mV
PFC I_{LIMIT} Comparator						
	Threshold Voltage		-0.9	-1	-1.15	V
	Delay to Output			150	300	ns
V_{IN} OK Comparator						
	Threshold Voltage		2.35	2.45	2.55	V
	Hysteresis		1.65	1.75	1.85	V
PWM Digital Soft Start						
	Digital Soft Start Timer (Note 2)	Right After Start Up (CM6803)		10		ms
DC I_{LIMIT} Comparator						
	Threshold Voltage		1.4	1.5	1.6	V
	Delay to Output (Note 2)			150	300	ns
Tri-Fault Detect Comparator						
	Fault Detect HIGH		2.70	2.77	2.85	V
	Time to Fault Detect HIGH	V_{FB}=$V_{FAULT\ DETECT\ LOW}$ to V_{FB} = OPEN, 470pF from V_{FB} to GND		2	4	ms
	Fault Detect LOW		0.4	0.5	0.6	V
Oscillator						
	Initial Accuracy	T_A = 25℃	62	67	74	kHz
	Voltage Stability	10V < V_{CC} < 15V		1		%
	Temperature Stability			2		%
	Total Variation	Line, Temp	60	67	74.5	kHz
	PFC Dead Time (Note 2)		0.3	0.45	0.65	µs

ELECTRICAL CHARACTERISTICS (Conti.) Unless otherwise stated, these specifications apply

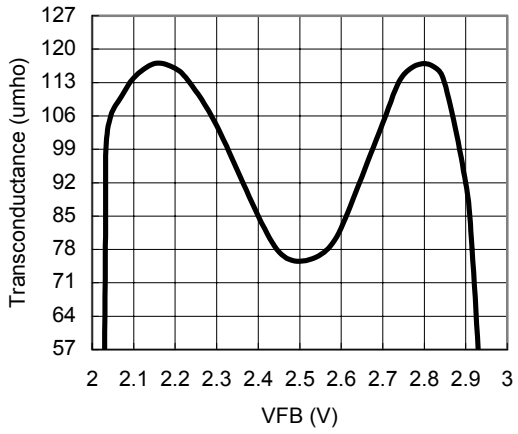
Vcc=+15V, R_T = 52.3kΩ, C_T = 470pF, T_A=Operating Temperature Range (Note 1)

Symbol	Parameter	Test Conditions	CM6803			Unit
			Min.	Typ.	Max.	
PFC						
	Minimum Duty Cycle	V_{FB}=2.55V, I_{SENSE} = -100V			0	%
	Maximum Duty Cycle	V_{FB}=2.0V, I_{SENSE} = 0V	90	95		%
	Output Low Rdson			15	22.5	ohm
	Output Low Voltage	I_{OUT} = -100mA		0.8	1.5	V
		I_{OUT} = -10mA, V_{CC} = 8V		0.4	0.8	V
	Output High Rdson			30	45	ohm
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time (Note 2)	C_L = 1000pF		50		ns
PWM						
	Duty Cycle Range	CM6803	0-49.5		0-50	%
	Output Low Rdson			15	22.5	ohm
	Output Low Voltage	I_{OUT} = -100mA		0.8	1.5	V
		I_{OUT} = -10mA, V_{CC} = 8V		0.7	1.5	V
	Output High Rdson			30	45	ohm
	Output High Voltage	I_{OUT} = 100mA, V_{CC} = 15V	13.5	14.2		V
	Rise/Fall Time (Note 2)	C_L = 1000pF		50		ns
Supply						
	Start-Up Current	V_{CC} = 11V, C_L = 0		100	150	uA
	Operating Current	V_{CC} = 15V, C_L = 0		2	4.0	mA
	Undervoltage Lockout Threshold		14.7	15	15.3	V
	Undervoltage Lockout Hysteresis		4.85	5	5.15	V

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

Note 2: Guaranteed by design, not 100% production test.

TYPICAL PERFORMANCE CHARACTERISTIC



Voltage Error Amplifier (g_{mv}) Transconductance

Functional Description

The CM6803 consists of an ICST (Input Current Shaping Technique), CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) boost PFC (Power Factor Correction) front end and a synchronized PWM (Pulse Width Modulator) back end. The CM6803 is designed to replace FAN4803 (8 pin SOP package), which is the second generation of the FAN4803 with 8 pin package. It is distinguished from earlier combo controllers by its low count, innovative input current shaping technique, and very low start-up and operating currents. The PWM section is dedicated to peak current mode operation. It uses conventional trailing-edge modulation, while the PFC uses leading-edge modulation. This patented Leading Edge/Trailing Edge (LETE) modulation technique helps to minimize ripple current in the PFC DC buss capacitor.

The main improvements from FAN4803 are:

1. Add Green Mode Functions for both PFC and PWM
2. Remove the one pin error amplifier and add back the slew rate enhancement gmv, which is using voltage input instead of current input. This transconductance amplifier will increase the transient response 5 to 10 times from the conventional OP
3. VFB PFC OVP comparator
4. Tri-fault Detect for UL1950 compliance and enhanced safety
5. VINOK comparator is added to guaranteed PWM cannot turn on until VFB reaches 2.5V in which PFC boost output is about steady state, typical 380V.
6. A 10mS digital PWM soft start circuit is added
7. 8 pin SOP package
8. No internal Zener but with VCCOVP comparator

The CM6803 operates both PFC and PWM sections at 67kHz. This allows the use of smaller PWM magnetic and output filter components, while minimizing switching losses in the PFC stage.

Several protection features have been built into the CM6803. These include soft-start, redundant PFC overvoltage protection, Tri-Fault Detect, VINOK, peak current limiting, duty cycle limiting, under-voltage lockout, reference ok comparator and VCCOVP.

Detailed Pin Descriptions

DCILIMIT (Pin 5)

This pin is tied to the primary side PWM current sense resistor or transformer. It provides the internal pulse-by-pulse current limit for the PWM stage (which occurs at 1.5V) and the peak current mode feedback path for the current mode control of the PWM stage. Besides current information, the optocouple also goes into DCILIMIT pin. Therefore, it is the SUM Amplifier input.

VCC (Pin 6)

VCC is the power input connection to the IC. The VCC start-up current is 100uA. The no-load ICC current is 2mA. VCC quiescent current will include both the IC biasing currents and the PFC and PWM output currents. Given the operating frequency and the MOSFET gate charge (Qg), average PFC and PWM output currents can be calculated as IOUT = Qg x F. The average magnetizing current required for any gate drive transformers must also be included. The VCC pin is also assumed to be proportional to the PFC output voltage. Internally it is tied to the VCC OVP comparator (17.9V) providing redundant high-speed over-voltage protection (OVP) of the PFC stage. VCC also ties internally to the UVLO circuitry and VREFOK comparator, enabling the IC at 15V and disabling it at 10V. VCC must be bypassed with a high quality ceramic bypass capacitor placed as close as possible to the IC. Good bypassing is critical to the proper operation of the CM6803.

VCC is typically produced by an additional winding off the boost inductor or PFC Choke, providing a voltage that is proportional to the PFC output voltage. Since the VCC OVP max voltage is 17.9V, an internal shunt limits VCC overvoltage to an acceptable value. An external clamp, such as shown in Figure 1, is desirable but not necessary.

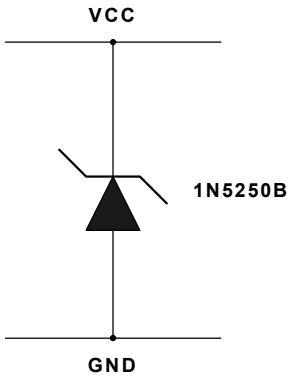


Figure 1. Optional VCC Clamp

This limits the maximum VCC that can be applied to the IC while allowing a VCC which is high enough to trip the VCC OVP. An RC filter at VCC is required between boost trap winding and VCC.

PFCOUT (Pin 7) and PWM OUT (Pin 8)
PFC OUT and PWM OUT are the high-current power driver capable of directly driving the gate of a power MOSFET with peak currents up to -1A and +0.5A. Both outputs are actively held low when VCC is below the UVLO threshold level which is 15V or VREFOK comparator is low.

ISENSE (Pin 2)
This pin ties to a resistor which senses the PFC input current. This signal should be negative with respect to the IC ground. It internally feeds the pulse-by-pulse current limit comparator and the current sense feedback signal. The ILIMIT trip level is –1V. The ISENSE feedback is internally multiplied by a gain of four and compared against the internal programmed ramp to set the PFC duty cycle. The intersection of the boost inductor current downslope with the internal programming ramp determines the boost off-time.

It requires a RC filter between ISENSE and PFC boost sensing resistor.

VEAO (Pin 3)
This is the PFC slew rate enhanced transconductance amplifier output which needs to connected with a compensation network Ground.

VFB (Pin 4)
Besides this is the PFC slew rate enhanced transconductance input, it also tie to a couple of protection comparators, PFCOVP, and Tri-Fault Detect

Power Factor Correction
Power factor correction makes a nonlinear load look like a resistive load to the AC line. For a resistor, the current drawn from the line is in phase with and proportional to the line voltage, so the power factor is unity (one). A common class of nonlinear load is the input of most power supplies, which use a bridge rectifier and capacitive input filter fed from the line. The peak-charging effect, which occurs on the input filter capacitor in these supplies, causes brief high-amplitude pulses of current to flow from the power line, rather than a sinusoidal current in phase with the line voltage. Such supplies present a power factor to the line of less than one (i.e. they cause significant current harmonics of the power line frequency to appear at their input). If the input current drawn by such a supply (or any other nonlinear load) can be made to follow the input voltage in instantaneous amplitude, it will appear resistive to the AC line and a unity power factor will be achieved.

To hold the input current draw of a device drawing power from the AC line in phase with and proportional to the input voltage, a way must be found to prevent that device from loading the line except in proportion to the instantaneous line voltage. The PFC section of the CM6803 uses a boost-mode DC-DC converter to accomplish this. The input to the converter is the full wave rectified AC line voltage. No bulk filtering is applied following the bridge rectifier, so the input voltage to the boost converter ranges (at twice line frequency) from zero volts to the peak value of the AC input and back to zero.

By forcing the boost converter to meet two simultaneous conditions, it is possible to ensure that the current draws from the power line matches the instantaneous line voltage. One of these conditions is that the output voltage of the boost converter must be set higher than the peak value of the line voltage. A commonly used value is 385VFB, to allow for a high line of $270VAC_{rms}$. The other condition is that the current that the converter is allowed to draw from the line at any given instant must be proportional to the line voltage.

PFC Control: Leading Edge Modulation with Input Current Shaping Technique (I.C.S.T.)

The only differences between the conventional PFC control topology and I.C.S.T. is:
the current loop of the conventional control method is a close loop method and it requires a detail understanding about the system loop gain to design. With I.C.S.T., since the current loop is an open loop, it is very straightforward to implement it.

The end result of the any PFC system, the power supply is like a pure resistor at low frequency. Therefore, current is in phase with voltage.
In the conventional control, it forces the input current to follow the input voltage. In CM6803, the chip thinks if a boost converter needs to behave like a low frequency resistor, what the duty cycle should be.

The following equations is CM6803 try to achieve:

$$R_e = V_{in} / I_{in} \quad (1)$$

$$\bar{I}_l = I_{in} \quad (2)$$

Equation 2 means: average boost inductor current equals to input current.

$$\therefore V_{in} \times \bar{I}_l \approx V_{out} \times \bar{I}_d \quad (3)$$

Therefore, input instantaneous power is about to equal to the output instantaneous power.

For steady state and for the each phase angle, boost converter DC equation at continuous conduction mode is:

$$V_{out} / V_{in} = 1 / (1-d) \quad (4)$$

Rearrange above equations, (1), (2),(3), and (4) in term of Vout and d, boost converter duty cycle and we can get average boost diode current equation (5):

$$\bar{I}_d = (1-d)^2 \times V_{out} / R_e \quad (5)$$

Also, the average diode current can be expressed as:

$$\bar{I}_d = \frac{1}{T_{sw}} \int_0^{T_{off}} I_d(t) \cdot dt \quad (6)$$

If the value of the boost inductor is large enough, we can assume $I_d(t) \sim I_d$. It means during each cycle or we can say during the sampling, the diode current is a constant.

Therefore, equation (6) becomes:

$$\bar{I}_d = I_d \times t_{off} / T_{sw} = I_d \times d' = I_d \times (1-d) \quad (7)$$

Combine equation (7) and equation (5), and we get:

$$I_d \times d' = (d')^2 \times V_{out} / R_e$$

$$\therefore I_d = d' \times V_{out} / R_e \quad (8)$$

$$\therefore I_d = \frac{V_{out}}{R_e} \times \frac{t_{off}}{T_{sw}}$$

From this simple equation (8), we implement the PFC control section of the CM6803.

Leading/Trailing Modulation

Conventional Pulse Width Modulation (PWM) techniques employ trailing edge modulation in which the switch will turn ON right after the trailing edge of the system clock. The error amplifier output is then compared with the modulating ramp. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned OFF. When the switch is ON, the inductor current will ramp up. The effective duty cycle of the trailing edge modulation is determined during the ON time of the switch. Figure 2 shows a typical trailing edge control scheme.

In case of leading edge modulation, the switch is turned OFF right at the leading edge of the system clock. When the modulating ramp reaches the level of the error amplifier output voltage, the switch will be turned ON. The effective duty-cycle of the leading edge modulation is determined during OFF time of the switch. Figure 3 shows a leading edge control scheme.

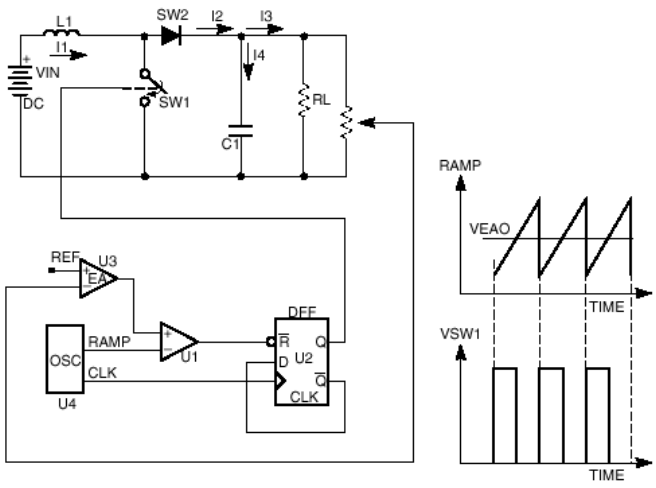


Figure 2. Typical Trailing Edge Control Scheme.

One of the advantages of this control technique is that it required only one system clock. Switch 1(SW1) turns OFF and switch 2 (SW2) turns ON at the same instant to minimize the momentary "no-load" period, thus lowering ripple voltage generated by the switching action. With such synchronized switching, the ripple voltage of the first stage is reduced. Calculation and evaluation have shown that the 120Hz component of the PFC's output ripple voltage can be reduced by as much as 30% using this method, substantially reducing dissipation in the high-voltage PFC capacitor.

Typical Applications

PFC Section:

PFC Voltage Loop Error Amp, VEAO

The ML4803 utilizes an one pin voltage error amplifier in the PFC section (VEAO). In the CM6803, it is using the slew rate enhanced transconductance amplifier, which is the same as error amplifier in the CM6800. The unique transconductance profile can speed up the conventional transient response by 10 times. The internal reference of the VEAO is 2.5V. The input of the VEAO is VFB pin.

PFC Voltage Loop Compensation

The voltage-loop bandwidth must be set to less than 120Hz to limit the amount of line current harmonic distortion. A typical crossover frequency is 30Hz.

The Voltage Loop Gain (S)

$$= \frac{\Delta V_{OUT}}{\Delta V_{EAO}} * \frac{\Delta V_{FB}}{\Delta V_{OUT}} * \frac{\Delta V_{EAO}}{\Delta V_{FB}}$$

$$\approx \frac{P_{IN} * 2.5V}{V_{OUTDC}^2 * \Delta V_{EAO} * S * C_{DC}} * GM_V * Z_{CV}$$

Z_{CV}: Compensation Net Work for the Voltage Loop
GM_V: Transconductance of VEAO
P_{IN}: Average PFC Input Power
V_{OUTDC}: PFC Boost Output Voltage; typical designed value is 380V.
C_{DC}: PFC Boost Output Capacitor

ΔV_{EAO}: This is the necessary change of the VEAO to deliver the designed average input power. The average value is 6V-3V=3V since when the input line voltage increases, the delta VEAO will be reduced to deliver the same to the output. To over compensate, we choose the delta VEAO is 3V.

Internal Voltage Ramp

The internal ramp current source is programmed by way of VEAO pin voltage. When VEAO increases the ramp current source is also increase. This current source is used to develop the internal ramp by charging the internal 30pF +12/ -10% capacitor. The frequency of the internal programming ramp is set internally to 67kHz.

Design PFC ISENSE Filtering

ISENSE Filter, the RC filter between Rs and ISENSE:

There are 2 purposes to add a filter at ISENSE pin:

1.) Protection: During start up or inrush current conditions, it will have a large voltage cross Rs, which is the sensing resistor of the PFC boost converter. It requires the ISENSE Filter to attenuate the energy.
2.) Reduce L, the Boost Inductor: The ISENSE Filter also can reduce the Boost Inductor value since the ISENSE Filter behaves like an integrator before going ISENSE which is the input of the current error amplifier, IEAO.

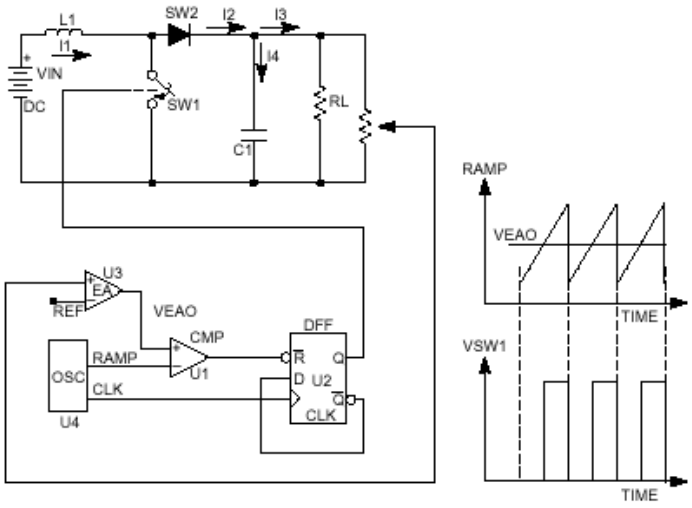


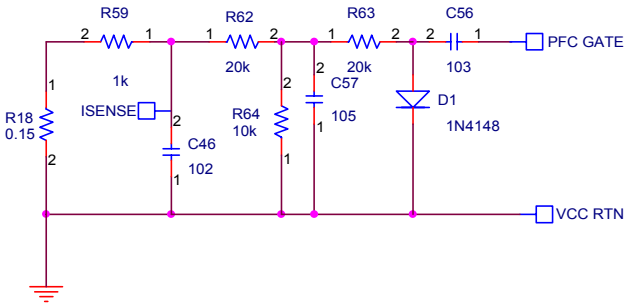
Figure 3 Typical Leading Edge Control Scheme

The I_{SENSE} Filter is a RC filter. The resistor value of the I_{SENSE} Filter is between 100 ohm and 50 ohm. By selecting R_{FILTER} equal to 50 ohm will keep the offset of the IEAO less than 5mV. Usually, we design the pole of I_{SENSE} Filter at fpfc/6, one sixth of the PFC switching frequency. Therefore, the boost inductor can be reduced 6 times without disturbing the stability. Therefore, the capacitor of the I_{SENSE} Filter, C_{FILTER}, will be around 283nF.

IAC, R_{AC}, Automatic Slope Compensation, DCM at high line and light load, and Startup current

PFC Current Sense Filtering

In DCM, the input current wave shaping technique used by the FAN4803 could cause the input current to run away. In order for this technique to be able to operate properly under DCM, the programming ramp must meet the boost inductor current down-slope at zero amps. Assuming the programming ramp is zero under light load, the OFF-time will be terminated once the inductor current reaches zero. Subsequently the PFC gate drive is initiated, eliminating the necessary dead time needed for the DCM mode. This forces the output to run away until the VCCOVP shuts down the PFC. This situation is corrected by adding an offset voltage to the current sense signal, which forces the duty cycle to zero at light loads. This offset prevents the PFC from operating in the DCM and forces pulse-keeping from the CCM to no-duty, avoiding DCM operation. External filtering to the current sense signal helps to smooth out the sense signal, expanding the operating range slightly into the DCM range, but this should be done carefully, as this filtering also reduces the bandwidth of the signal feeding the pulse-by-pulse current limit signal. The typical circuit for adding offset to ISENSE at light load as below.



PFC section wakes up after Start up period
After Start up period, PFC section will softly start since VEAO is zero before the start-up period. Since VEAO is a slew rate enhanced transconductance amplifier (see figure 3), VEAO has a high impedance output like a current source and it will slowly charge the compensation net work which needs to be designed by using the voltage loop gain equation.
Before PFC boost output reaches its design voltage, it is around 380V and VFB reaches 2.5V, PWM section is off.

PWM section wakes up after PFC reaches steady state
PWM section is off all the time before PFC VFB reaches 2.45V. Then internal 10mS digital PWM soft start circuit slowly ramps up the soft-start voltage.

PFC OVP Comparator
PFC OVP Comparator sense VFB pin which is the same the voltage loop input. The good thing is the compensation network is connected to VEAO. The PFC OVP function is a relative fast OVP. It is not like the conventional error amplifier which is an operational amplifier and it requires a local feedback and it make the OVP action becomes very slow. The threshold of the PFC OVP is 2.5V+10% =2.75V with 250mV hysteresis.

Tri-Fault Detect Comparator

To improve power supply reliability, reduce system component count, and simplify compliance to UL1950 safety standards, the CM6803 includes Tri-Fault Detect. This feature monitors VFB (Pin 4) for certain PFC fault conditions.

In case of a feedback path failure, the output of the PFC could go out of safe operating limits. With such a failure, VFB will go outside of its normal operating area. Should VFB go too low, too high, or open, Tri-Fault Detect senses the error and terminates the PFC output drive.

Tri-Fault detect is an entirely internal circuit. It requires no external components to serve its protective function.

VCC OVP and generate VCC
For the CM6803 system, if VCC is generated from a source that is proportional to the PFC output voltage and once that source reaches 17.9V, PFCOUT, PFC driver will be off.

The VCC OVP resets once the VCC discharges below 16.4V, PFC output driver is enabled. It serves as redundant PFC OVP function.
Typically, there is a bootstrap winding off the boost inductor. The VCC OVP comparator senses when this voltage exceeds 17.9V, and terminates the PFC output drive. Once the VCC rail has decreased to below 16.4V the PFC output drive be enabled. Given that 16V on VCC corresponds to 380V on the PFC output, 17.9V on VCC corresponds to an OVP level of 460V.
It is a necessary to put RC filter between bootstrap winding and VCC. For VCC=15V, it is sufficient to drive either a power MOSFET or a IGBT.

UVLO
The UVLO threshold is 15V providing 5V hysteresis.

PFCOUT and PWMOUT

Both PFCOUT and PWMOUT are CMOS drivers. They both have adaptive anti-shoot through to reduce the switching loss. Its pull-up is a 30ohm PMOS driver and its pull-down is a 15ohm NMOS driver. It can source 0.5A and sink 1A if the VCC is above 15V.

PWM Section

Green Mode
CM6803 has the green mode function to improve the light load efficiency. PWM Green Mode will happen when the PWMCMP (PWM Comparator) Duty Cycle is less than ~ 6%, in the next cycle, the PWMOUT pulse will be removed until PWMCMP Duty Cycle is greater than 6%, then the next cycle, PWMOUT pulse appears.

In other words, during the green mode, PWM switching frequency will reduce to improve the efficiency. With the proper external components, CM6803 can easily meet energy star and blue angel specification.

After 10mS digital soft start, CM6803's PWM is operating as a typical current mode. It requires a secondary feedback, typically, it is configured with CM431, and photo couple.

Since PWM Section is different from CM6800 family, it needs the emitter of the photo couple to connected with DCILIMIT instead of the collector. The PWM current information also goes into DCILIMIT. Usually, the PWM current information requires a RC filter before goes into the DCILIMIT.

Therefore, DCILIMIT actually is a summing node from voltage information which is from photo couple and CM431 and current information which is from one end of PWM sensing resistor and the signal goes through a single pole, RC filter then enter the DCILIMIT pin.

This RC filter at DCILMIT also serves several functions:
1.) It protects IC.
2.) It provides level shift for voltage information.
3.) It filters the switching noise from current information.

The pole location of the RC filter should be greater than one sixth of the PWM switching frequency which is 67Khz for CM6803. Since the typical photo couple should be biased around 1mA, the resistor of the RC filter should be around 1.5V/1mA~1.5K ohm and we suggest R is 1K ohm. Therefore, for CM6803, C should be around 14nF.

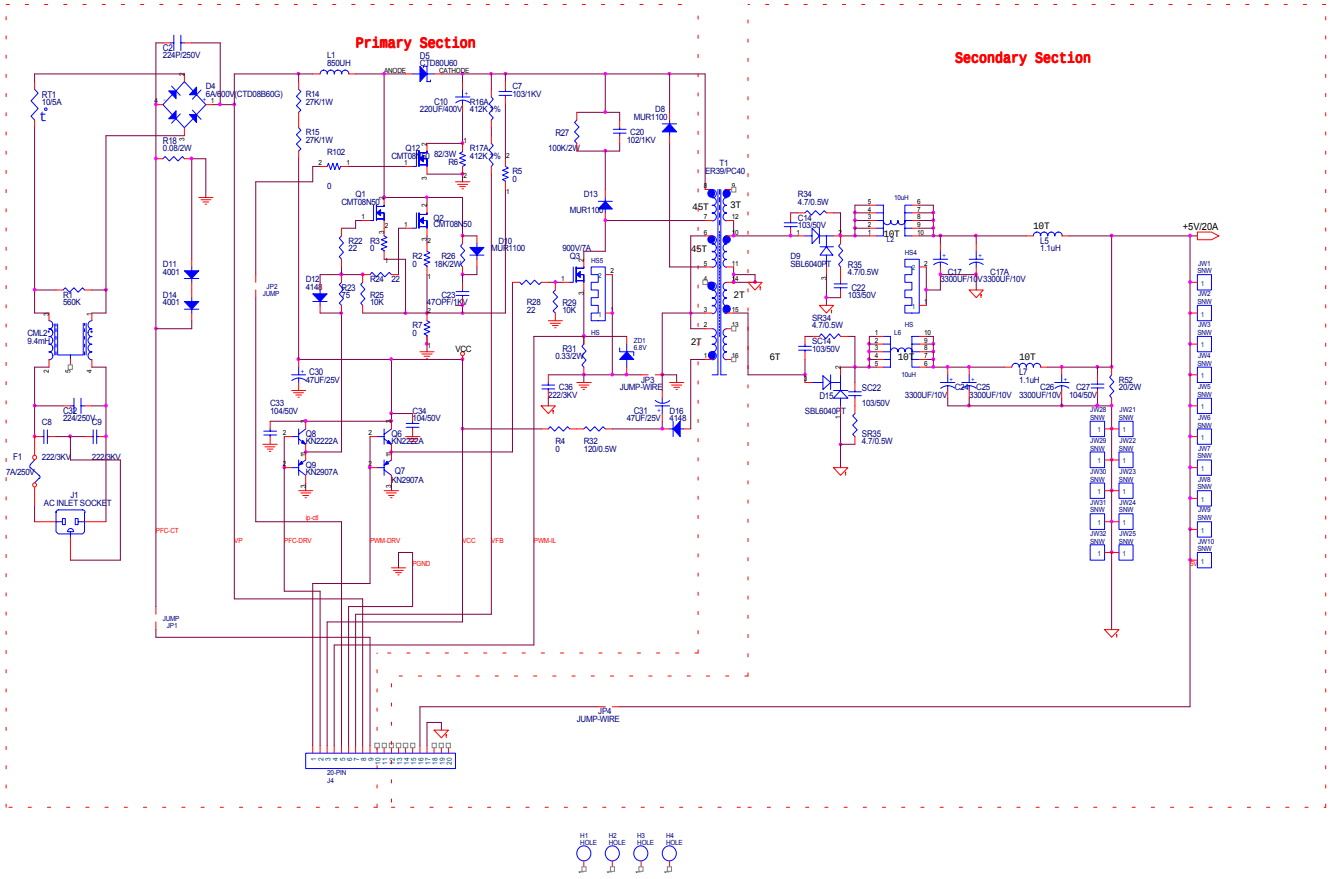
The maximum input voltage of the DCILIMIT pin is 1.5V.

Component Reduction
Components associated with the VRMS and IEAO pins of a typical PFC controller such as the CM6800 have been eliminated. The PFC power limit and bandwidth does vary with line voltage.

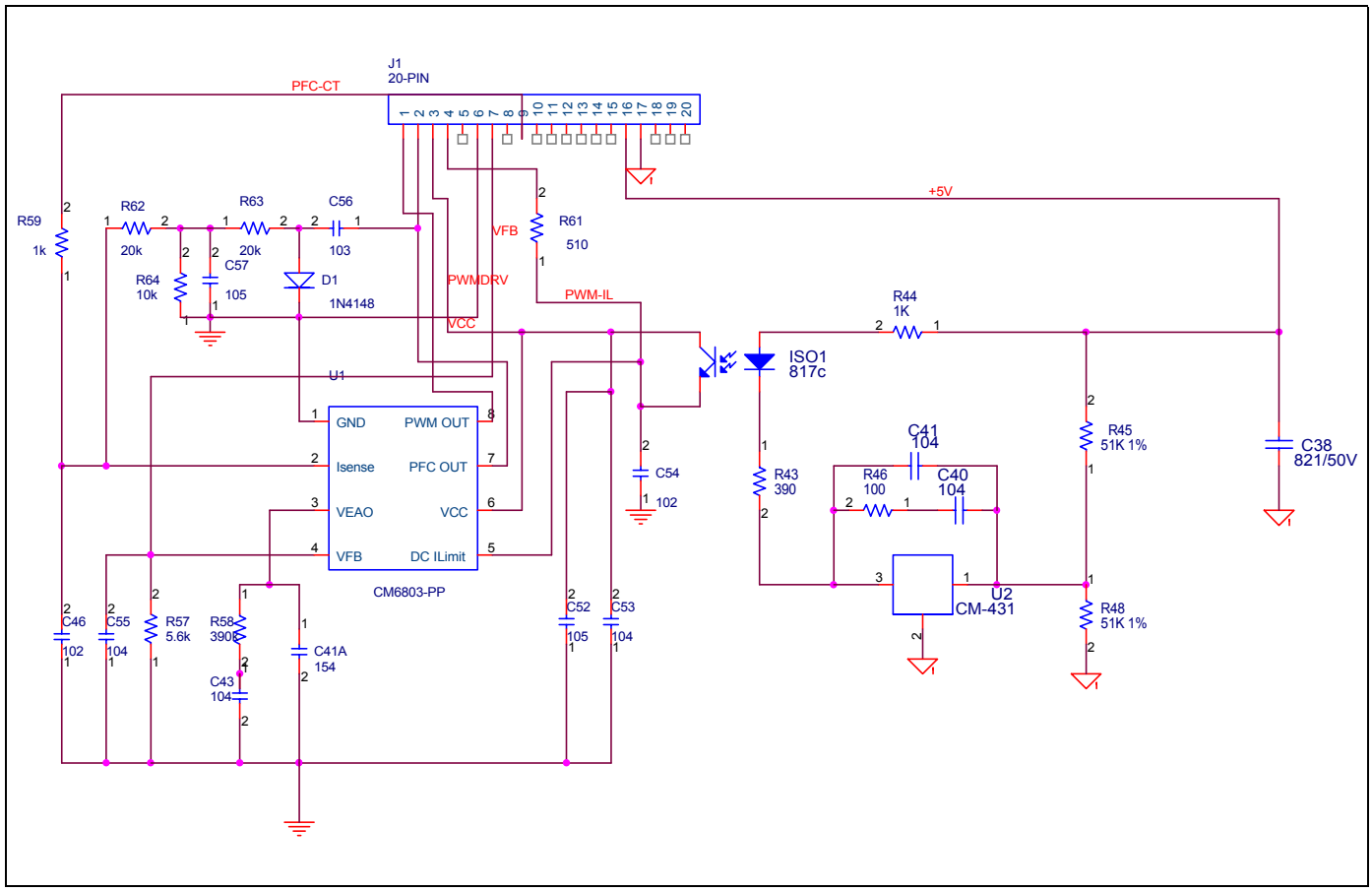
MAIN BOARD CIRCUIT

CM6800 DEMO BOARD (1 OUTPUT)

INPUT POWER: AC 90V-->5.8A
INPUT POWER: AC 260V-->1.9A
OUTPUT POWER: DC 250W
DATE:09-20-2002 3:00 PM

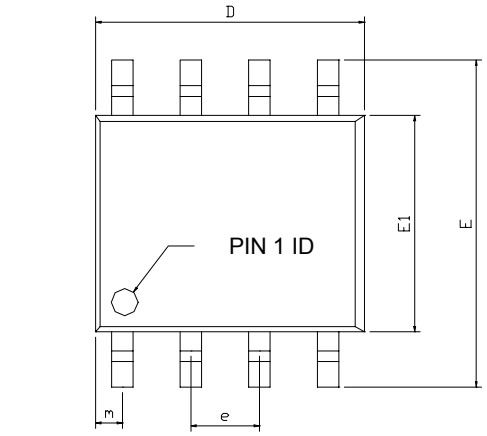


CONTROL BOARD CIRCUIT



PACKAGE DIMENSION

8-PIN SOP (S08)



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHS		
	MIN	NOM	MAX	MIN	NOM	MAX
A1	0.10	---	0.25	0.004	---	0.010
A2	1.40	---	1.55	0.055	---	0.061
b	0.30	---	0.51	0.012	---	0.020
C	0.15	---	0.26	0.006	---	0.010
D	4.60	---	5.06	0.169	---	0.199
E	5.79	---	6.20	0.228	---	0.244
E1	3.76	---	4.01	0.148	---	0.158
e	---	1.27	---	---	0.050	---
L	0.38	---	0.69	0.015	---	0.035
m	0.43	---	0.69	0.017	---	0.027
θ	0°	---	8°	0°	---	8°

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