CSD967201-Q1 Automotive Synchronous Buck Smart Power Stage

1 Features

- 3V to 20V input voltage range
- 60A nominal, 90A peak current capability
- AEC-Q100 qualified for automotive applications
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature range, T_A
  - Junction temperature: –40°C to +150°C, T_J
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- 87.7% power stage peak efficiency at 650kHz, 12V V_{IN}, 0.6V V_{OUT}
- 89.4% power stage peak efficiency at 650kHz, 12V V_{IN}, 0.8V V_{OUT}
- Reduced switch-node ringing
- High-frequency operation (up to 2MHz)
- Temperature compensated bi-directional current sense reporting (5µA/A)
- Body braking mode (BB)
- Fault detection
  - High-side short (HSS)
- Fault protection
  - Overtemperature (OT)
  - Cycle-by-cycle valley overcurrent limiting (IOC_{VALLEY})
  - Secondary peak over current protection (IOC_{PEAK})
  - Cycle-by-cycle negative overcurrent detection
- 5mm × 6mm × 0.75mm QFN industry common footprint package
- Green, RoHS compliant without exemption

2 Applications

- Automotive ADAS
- Automotive infotainment and cluster
- Software-defined vehicle: high-performance compute

3 Description

The CSD967201-Q1 power stage is a highly optimized design for use in an automotive qualified high-power, high-density synchronous buck converter. This device integrates the driver IC and power MOSFETs into one Pb-free monolithic design to complete the power stage switching function. This combination produces high-current, high-efficiency, and high-speed switching capability in a small industry standard 5mm × 6mm × 0.75mm footprint.

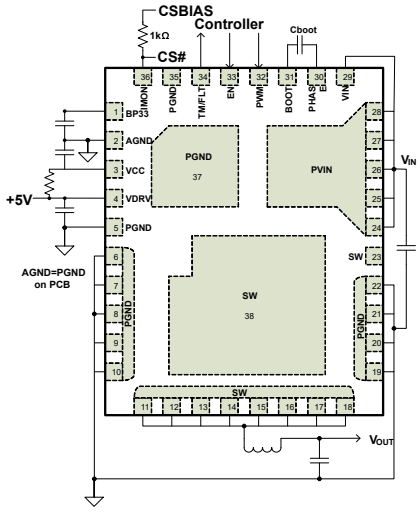
CSD967201-Q1 integrates accurate current sensing and temperature sensing functionality to simplify system design and improve accuracy. Protections include cycle-by-cycle overcurrent and negative overcurrent limiting, overtemperature shutdown, HS FET short, and UVLO on VCC, VIN, and BOOT.

The CSD967201-Q1 is compatible with the TPS64300-Q1 VRS-11 controller, as well as other standard VRS-11 controllers.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
CSD967201-Q1	VDK (WQFN-FCRLF, 38)	6mm × 5mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application Diagram

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4 Pin Configuration and Functions

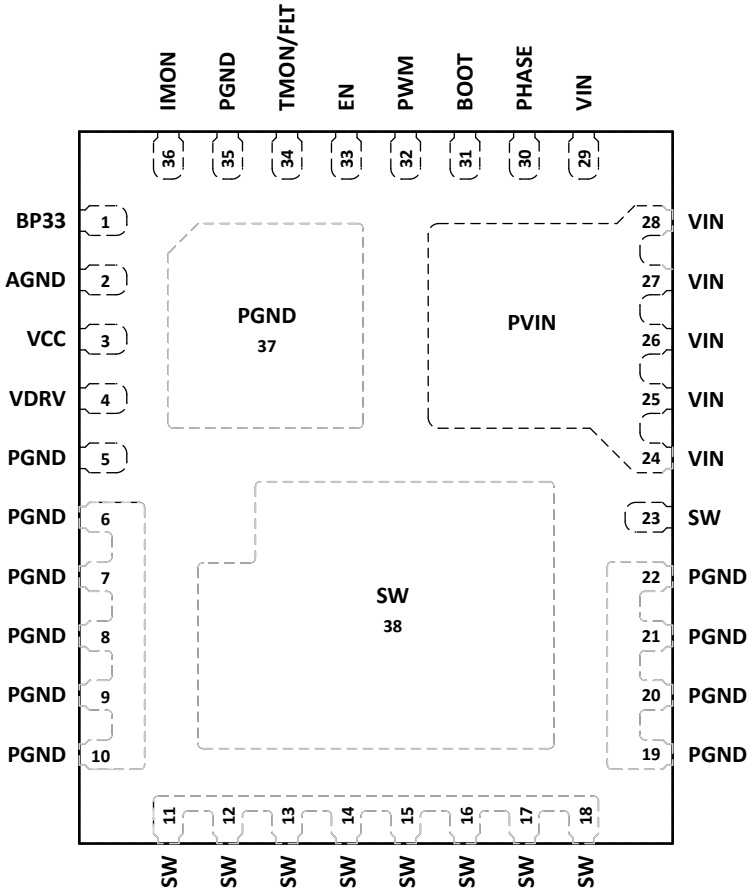

Figure 4-1. VDK Package 38-Pin WQFN-FCRLF (5mm × 6mm × 0.75mm) - Top View

Table 4-1. CSD967201-Q1 Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
AGND	2	GND	Analog ground
BOOT	31	I/O	Bootstrap capacitor connection. Connect a minimum 0.1µF, 16V, X5R ceramic capacitor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to switch HS FET. The bootstrap diode is integrated.
EN	33	I	This pin is used to enable the device. When EN is logic high, the gate driver responds to PWM inputs. When EN is logic low, both MOSFET gates are actively driven off.
IMON	36	O	Output of current sensing amplifier. The output of this pin is proportional to the inductor current with a gain of 5µA/A.
BP33	1	I/O	Connect a bypass capacitor from this pin to AGND. The recommendation is to use one 100nF, 16V, X7R capacitor on BP33.
PGND	5 6 – 10 19-22 35, 37	GND	Power ground for the internal power stage.
PHASE	30	O	Phase pin. Bootstrap capacitor connection return path for the HS FET floating driver. This pin is connected to VSW internally. Connect a minimum 0.1µF, 16V, X5R ceramic capacitor from BOOT to PHASE pin. The bootstrap capacitor provides the charge to switch HS FET. The bootstrap diode is integrated.

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Table 4-1. CSD967201-Q1 Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
PWM	32	I	Tri-state input from external controller. Logic low sets control FET gate low and sync FET gate high. Logic high sets control FET gate high and sync FET gate low. Either Body Brake or DCM is enabled if PWM stays in Hi-Z for greater than the tri-state shutdown holdoff time (t_{3HT}).
SW	11 – 18, 23, 38	O	Switch node connecting the HS MOSFET source and LS MOSFET drain - pin connection to the output inductor.
TMON/FLT	34	O	Temperature amplifier output. Reports a voltage proportional to the IC temperature. An ORing function is integrated in the IC. When used in multiphase applications, a single wire can be used to connect the TMON/FLT pins of all the ICs. Only the highest temperature is reported. TMON/FLT is pulled up to 3V if thermal shutdown detection circuit is tripped.
VCC	3	PWR	Supply voltage for internal analog circuitry. This pin is bypassed to AGND. The recommendation is to use one 2.2µF, 10V, X5R capacitor on VCC.
VDRV	4	PWR	Supply voltage for gate drivers. This pin is bypassed to PGND. The recommendation is to use one 1µF, 16V, X7R capacitor on VDRV.
VIN	24 – 29	I	Power input voltage pin. Connect input capacitors close to this pin. The recommendation is to use at least five 10µF, 25V, X7R capacitors on VIN, plus two 0.1uF, 50V, X7R caps close to the VIN pins.

(1) I = input, O = output, GND = ground

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5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{INPUT}	PVIN to PGND	–0.3	24	V
	PVIN to SW (DC)	–0.3	24	V
	PVIN to SW (Transient for 25ns)		26	V
	SW to PGND (DC)	–0.3	24	V
	SW to PGND (Transient for 25ns)		26	V
	BP33	-0.3	3.6	
	VCC to AGND	–0.3	6	V
	VDRV to PGND	–0.3	6	V
	EN, TMON/FLT to AGND(2)	–0.3	VCC + 0.3	V
	IMON, PWM to AGND	–0.3	6	V
	BOOT to PHASE(2)	–0.3	VCC + 0.3	V
	BOOT to PGND	–0.3	V_{SW} + 5	V
	Transient Load	max NegOC threshold	min HSOC value	A
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Must not exceed 6V

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	VCC supply voltage	4.5	5	5.5	V
V_{IN}	PVIN supply voltage (DC nominal for start-up)	3	12	20	V
V_{IN}	PVIN supply voltage (transient after start-up) ($V_{IN\_UVLO\_RISING}$ - $V_{IN\_UVLO\_HYS}$)		2.7		V
V_{OUT}		0.2	0.6	2.0	V
I_{OUT}	Output current (DC)			60	A
I_{OUT_PK}	Output current transient			90	A
f_{SW}	Switching frequency	200	500	2000	kHz
	Minimum PWM on time	12		30	ns
	Minimum PWM off time (steady state)			60	ns

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5.3 Recommended Operating Conditions (continued)

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Junction temperature	–40		150	°C

5.4 Thermal Information

THERMAL METRIC[1]		VDK (WQFN-FCRLF) 38 PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.49	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	3.66	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.12	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	3.66	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.17	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

Over recommended operating conditions and junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN						
$VIN_{SHUTDOWN}$	Voltage at which device tri-states output	VIN rising	21	22	22.3	V
VIN_{SD_HYS}	$VIN_{SHUTDOWN}$ hysteresis			500		mV
$I_{VIN,standby}$	VIN standby supply current	VIN = 12V, PWM = Z		105		µA
VDRV + VCC						
$I_{CC+DRV\_standby}$	Standby supply current	EN = Low, PWM = Z		60		µA
$I_{CC+DRV\_standby}$	Standby supply current	EN = High, PWM = Z		1.6		mA
Power-On Reset and Undervoltage Lockout						
V_{POR}	VDRV voltage for complete power down	VDRV rising		3		V
		VDRV falling		2.8		V
V_{CC_UVLO}	VCC undervoltage lockout voltage	VCC rising		3.8	4	V
V_{HYS_VCC}	VCC undervoltage lockout voltage hysteresis			200		mV
$V_{DRV\_UVLO\_RISING}$	VDRV undervoltage lockout voltage	VDRV rising		4	4.2	V
$V_{DRV\_UVLO\_HYS}$	VDRV undervoltage lockout voltage hysteresis			200		mV
$V_{IN\_UVLO\_RISING}$	PVIN undervoltage lockout voltage	PVIN rising	2.85	3	3.1	V
$V_{IN\_UVLO\_HYS}$	PVIN undervoltage lockout voltage hysteresis		225	300	350	mV
PWM						
C_{PWM_IN}	PWM pin capacitance				200	pF
R_{PWM}	PWM resistance			4		kΩ

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5.5 Electrical Characteristics (continued)

Over recommended operating conditions and junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IHPWM}	PWM input logic level high, rising	VCC = 5V		2.2	2.3	V
	PWM input logic level high, falling		1.9	2.0		V
V_{PWMT}	PWM input tri-state window high	VCC = 5V	1.9			
	PWM input tri-state window low				1.3	V
V_{PWML}	PWM input logic level low, rising	VCC = 5V		1.2	1.3	V
	PWM input logic level low, falling		0.89	1.0		V
SW						
V_{SW_LKG}	SW voltage due to HS leakage	EN = 0V, VDRV = 0, 4V < VIN < 20V		1	146	mV
		EN = 0V, 4.5V < VDRV <6V, 4V < VIN < 20V		46	138	mV
EN						
V_{IH_EN}	Logic level high threshold			2.0	2.5	V
R_{EN}	Enable pin internal pulldown			500		kΩ
V_{IL_EN}	Logic level low threshold		0.8			V
Temperature Sense (TMON/FAULT)						
V_{TMON_OFFS}	TMON offset voltage	$V_{TMON} = V_{TMON\_OFFS} + T_J \times V_{TMON\_GAIN}$		600		mV
V_{TMON_25C}	TMON voltage at TJ = 25°C (Across VCC)		776	800	824	mV
G_{TMON}	TMON voltage temperature coefficient (across VCC)			8		mV/°C
TMON_ACCURACY	Temperature sensing accuracy		–3		3	%
I_{TMON}	TMON sinking current	V_{TMON} = 0.8V (25°C)	TBD	0.24	TBD	mA
I_{TMON}	TMON sourcing current	V_{TMON} = 0.8V (25°C)	TBD	6.6	TBD	mA
$V_{TMON\_\_FAULT}$	TMON voltage at fault		3	3.3		V
Current Sense (IMON)						
	Current sensing range	1K Sense resistor	–40		IOC_{PEAK}	A
	Current sensing accuracy	–30A <= I_L < –10A, LS FET ON	–5		5	%
	Current sensing accuracy up to 10A	-10A <= I_L < 10A, LS FET ON		500		mA
	Current sensing accuracy up to 30A	0A <= I_L < 30A, LS FET ON		900		mA
	Current sensing accuracy	30A <= I_L < 60A, LS FET ON	–3		3	%
	Current sensing accuracy	10A <= I_L < 60A, LS FET ON	–5		5	%
	Current sensing accuracy	60A <= I_L < 90A, LS FET ON	–5		5	%
$I_{IMON\_VOUT\_RANGE}$	Current sense dynamic voltage range		0.8		2.2	V
I_{IMON_GAIN}	Current sense gain	IMONREF = 1.25V		5		µA/A
Protections (IOC, HSS, NOC, Thermal Shutdown)						
I_{HSS}	High side short threshold	PWM = Low		–100		A
I_{NOCL}	Negative cycle-by-cycle current limit falling threshold	PWM = Low		–45		A
I_{NOCH}	Negative cycle-by-cycle current limit rising threshold for hysteresis current limiting	PWM = Low		–25		A
IOC_{PEAK}	Over current peak threshold	PWM = Hi	113	130	140	A

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5.5 Electrical Characteristics (continued)

Over recommended operating conditions and junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IOC_{VALLEY}	Over current valley threshold	PWM = Low	85	95	110	A
V_{CBOOT_FAULT}	Boot cap fault voltage threshold			2.2		V
V_{CBOOT_CHG}	Boot cap recharge voltage threshold (rising)			2.6		V
V_{CBOOT_CHG}	Boot cap recharge voltage threshold (falling)			2.1		V
$T_{SHUTDOWN}$	Thermal shutdown threshold (rising)			155		°C
$T_{SHUTDOWN\_HYS}$	Thermal shutdown hysteresis (falling)			20		°C

5.6 Switching Characteristics (Timing)

Over recommended operating conditions and junction temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-On Reset and Undervoltage Lockout						
$t_{PD\_POR\_PWM}$	POR to PWM Delay	EN and VCC rising, PWM=L. Time between VCC_UVLO to low side gate drive is H. C_{BP33} = 100nF			75	µs
$t_{PD\_EN\_PWM}$	EN to PWM Delay	EN rising, VCC=H, PWM=L. Time between EN=H to low side gate drive is H. C_{BP33} = 100nF			25	µs
PWM						
$t_{PD\_PWM\_SW}$	PWM to SW Delay	V_{IHPWM} to SW 50% rising, 10A		27	40	ns
$t_{3T\text{-}HOLDOFF}$	Tri-state window enter hold-off time	V_{IHPWM} to V_{PWMT} to SW tristate		25		ns
$t_{3RD\text{-}HOLDOFF}$	Tri-state window exit hold-off time	V_{IHPWM} from V_{PWMT} to V_{PWML} to SW rising		27		ns
Current Sense (IMON)						
$t_{PD\_SW\_IMON}$	SW to IMON delay (delay between IMON peak from actual inductor current peak)				35	ns
$I_{IMON\_LATENCY}$	Minimum number of PWM cycles for accurate current sense during transient	Current sense within specified accuracy		10		cycles
	Minimum PWM LS Ton for accurate current sense for DC accuracy	Current sense within specified accuracy		100		ns

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5.7 Typical Device Characteristics: Power Stage

The typical CSD967201-Q1 characteristic curves are based on measurements made on a PCB design with dimensions of 3.5 in (W) × 5in (L) × 0.00958 in (T) and 8 2oz copper layers. See the *Application and Implementation* for a detailed explanation. The operating conditions for all graphs are V_{IN} = 12V, V_{DRV} = 5V, V_{CC} = 5V, V_{OUT} = 0.8V, f_{SW} = 650kHz, L_{OUT} = 85nH, I_{OUT} = 30A, T_J = 25°C with no heat sink and no airflow. For device efficiency and power, no controller loss or DC inductor loss is included unless otherwise stated (inductor AC loss is not excluded). For board efficiency and power, all losses from the power stage, inductor AC and DC losses, as well as board and connector losses are included unless otherwise stated.

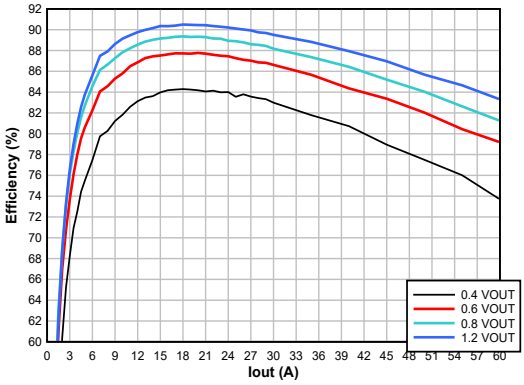

Figure 5-1. 12VIN Device Efficiency

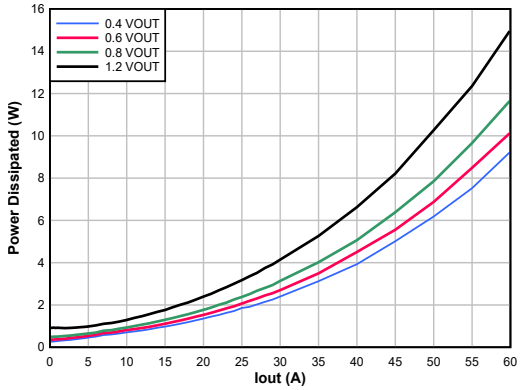

Figure 5-2. 12VIN Device Power Loss

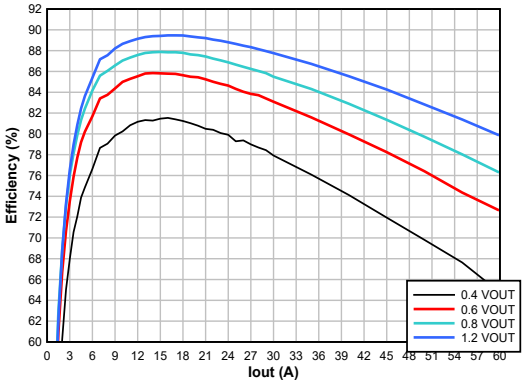

Figure 5-3. 12VIN Board Efficiency

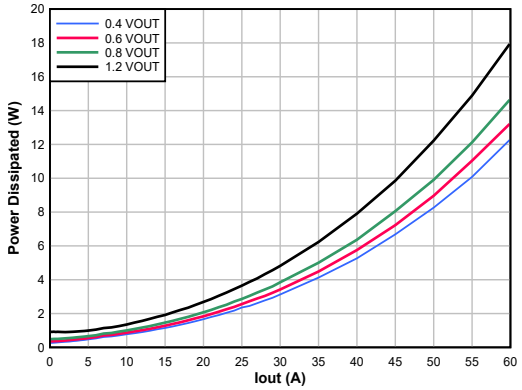

Figure 5-4. 12VIN Board Power Loss

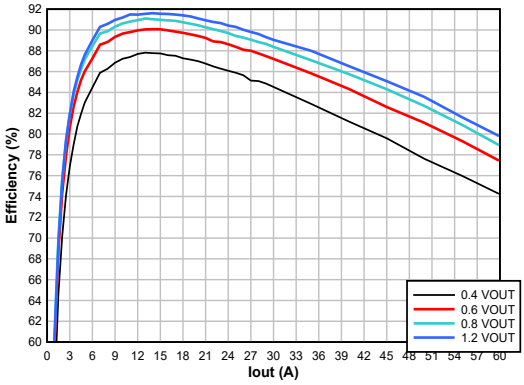

Figure 5-5. 6VIN Device Efficiency

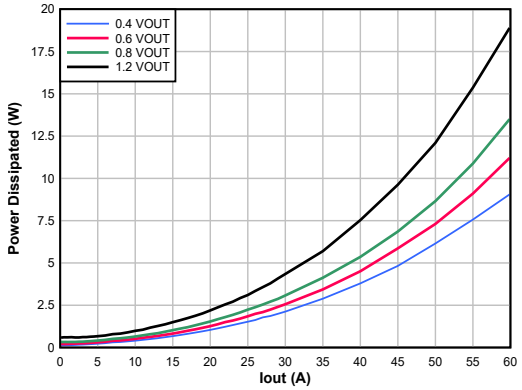

Figure 5-6. 6VIN Device Power Loss

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5.7 Typical Device Characteristics: Power Stage (continued)

The typical CSD967201-Q1 characteristic curves are based on measurements made on a PCB design with dimensions of 3.5 in (W) × 5in (L) × 0.00958 in (T) and 8 2oz copper layers. See the *Application and Implementation* for a detailed explanation. The operating conditions for all graphs are V_{IN} = 12V, V_{DRV} = 5V, V_{CC} = 5V, V_{OUT} = 0.8V, f_{SW} = 650kHz, L_{OUT} = 85nH, I_{OUT} = 30A, T_J = 25°C with no heat sink and no airflow. For device efficiency and power, no controller loss or DC inductor loss is included unless otherwise stated (inductor AC loss is not excluded). For board efficiency and power, all losses from the power stage, inductor AC and DC losses, as well as board and connector losses are included unless otherwise stated.

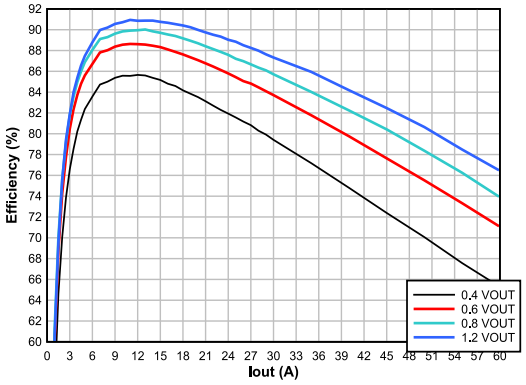

Figure 5-7. 6VIN Board Efficiency

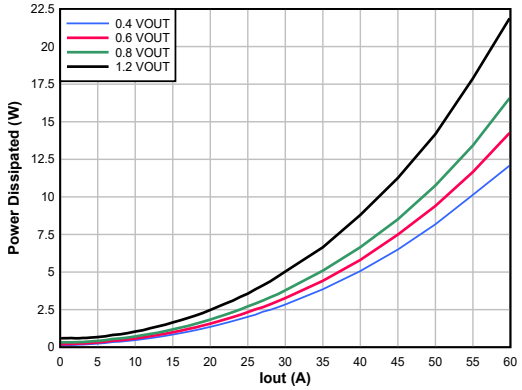

Figure 5-8. 6VIN Board Power Loss

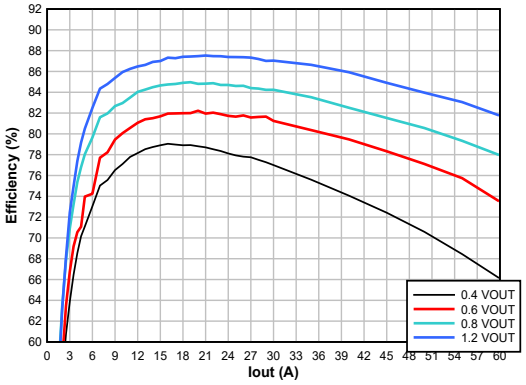

Figure 5-9. 19VIN Device Efficiency

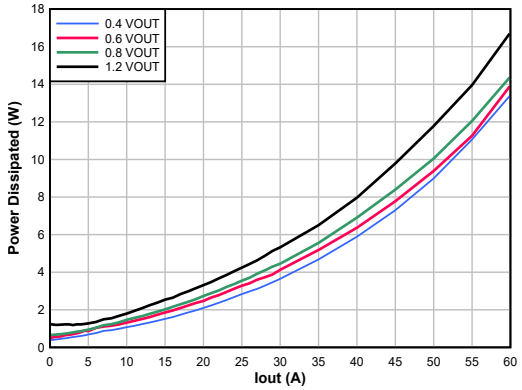

Figure 5-10. 19VIN Device Power Loss

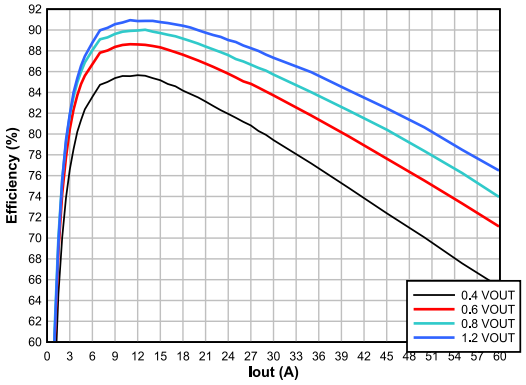

Figure 5-11. 19VIN Board Efficiency

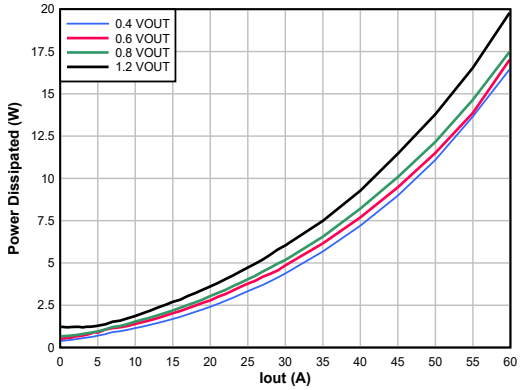

Figure 5-12. 19VIN Board Power Loss

5.7 Typical Device Characteristics: Power Stage (continued)

The typical CSD967201-Q1 characteristic curves are based on measurements made on a PCB design with dimensions of 3.5 in (W) × 5in (L) × 0.00958 in (T) and 8 2oz copper layers. See the *Application and Implementation* for a detailed explanation. The operating conditions for all graphs are V_{IN} = 12V, V_{DRV} = 5V, V_{CC} = 5V, V_{OUT} = 0.8V, f_{SW} = 650kHz, L_{OUT} = 85nH, I_{OUT} = 30A, T_J = 25°C with no heat sink and no airflow. For device efficiency and power, no controller loss or DC inductor loss is included unless otherwise stated (inductor AC loss is not excluded). For board efficiency and power, all losses from the power stage, inductor AC and DC losses, as well as board and connector losses are included unless otherwise stated.

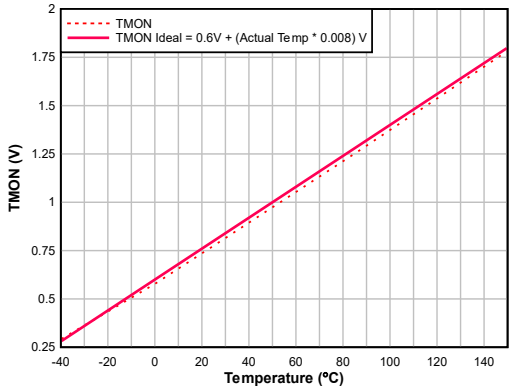

Figure 5-13. TMON Voltage vs Actual Temp

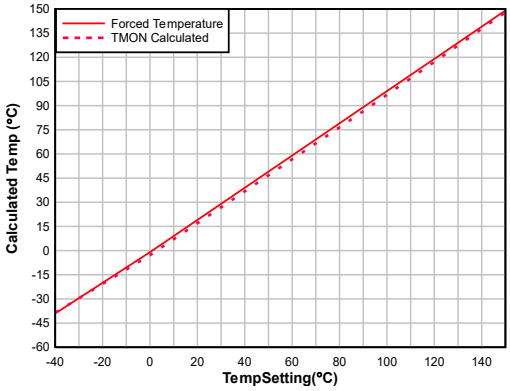

Figure 5-14. TMON Calculated Temp vs Actual Temp

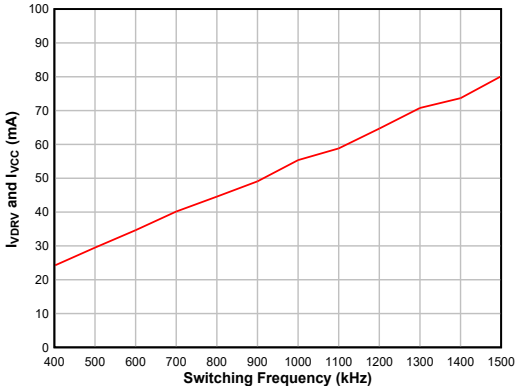

Figure 5-15. VCC + VDRV Current vs Switching Frequency

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5.8 Typical Characteristics: Current Sense

The typical CSD967201-Q1 characteristic curves are based on measurements made on a PCB design with dimensions of 3.5 in (W) × 5in (L) × 0.00958 in (T) and 8 2oz copper layers. Of these 12 copper layers, 8 are signal layers of 1oz copper thickness and 4 are power layers of 2oz copper thickness. See the *Application and Implementation* section for a detailed explanation. The conditions for all graphs is V_{IN} = 12V, V_{DRV} = 5V, V_{CC} = 5V, V_{OUT} = 0.8V, L_{OUT} = 85nH, I_{LOAD} = 30A, T_J = 25°C with no heat sink and no airflow. No controller loss or DC inductor loss unless otherwise stated (inductor AC loss is not excluded).

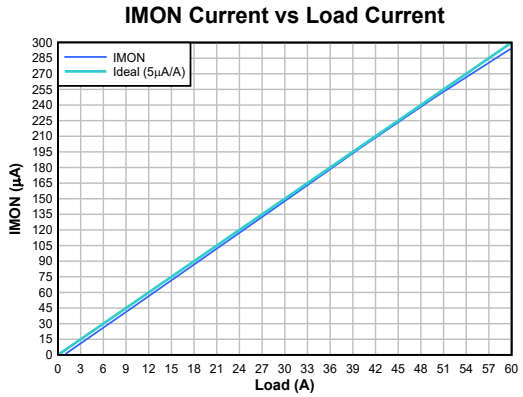


Figure 5-16. IMON Current vs Current

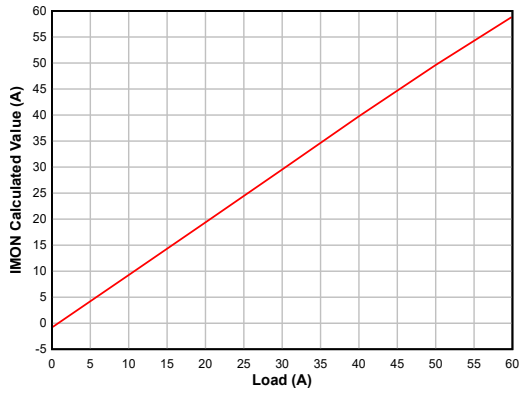


Figure 5-17. IMON Calculated Load Current vs Actual Load Current

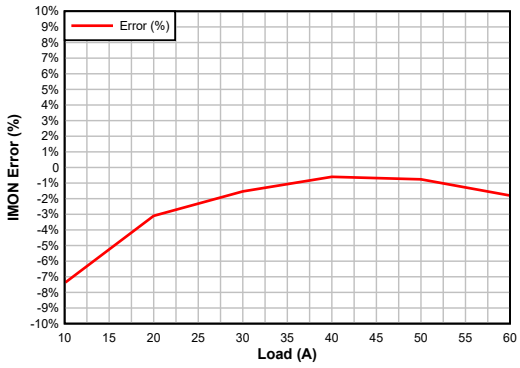


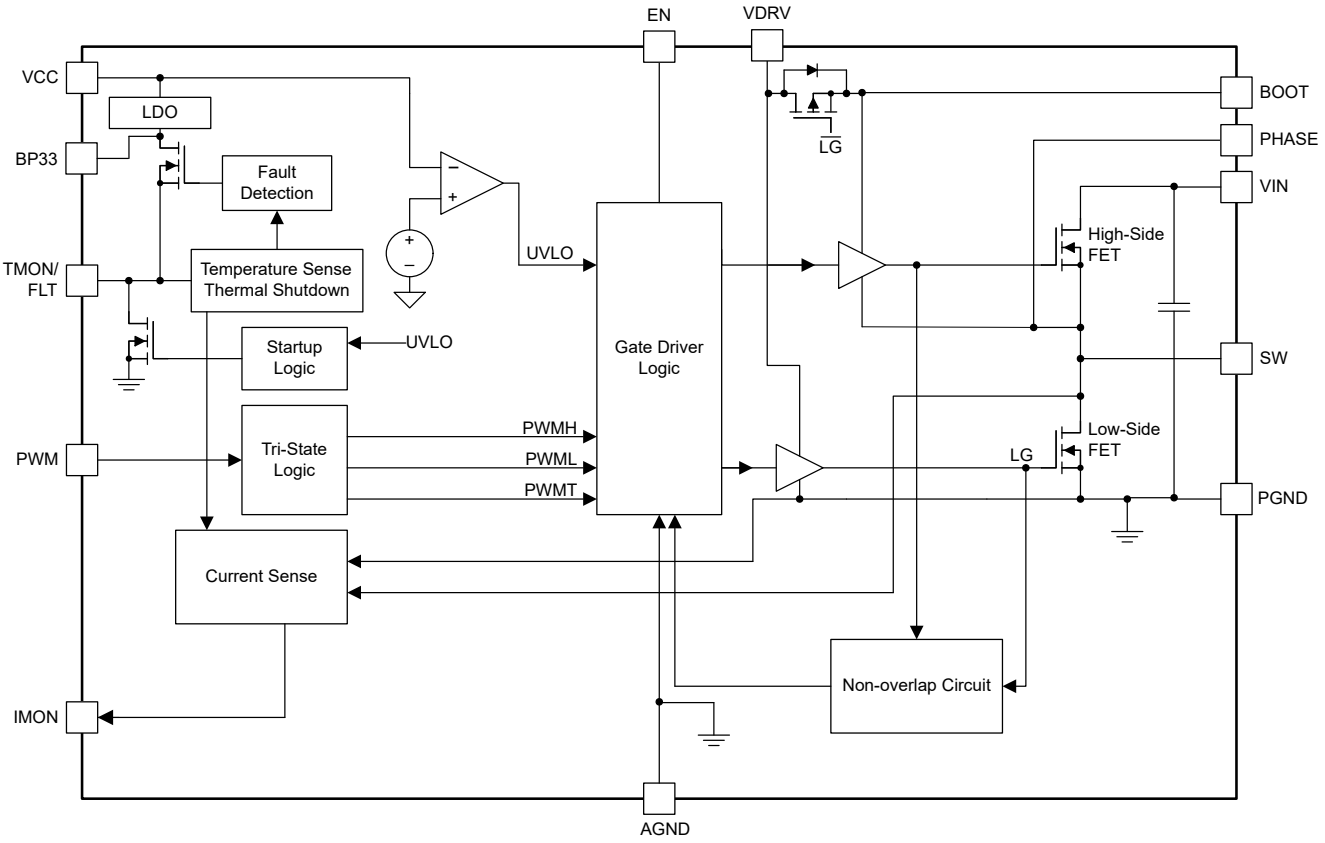
Figure 5-18. Current Sense Accuracy for Load Current from 10A to 60A (Error % vs Load Current)

6 Detailed Description

6.1 Overview

The CSD967201-Q1 monolithic power stage is a highly optimized design for use in a high-power, high-density synchronous buck converter.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Powering the CSD967201-Q1 and Gate Drivers

CSD967201-Q1 requires an external voltage to supply the integrated driver IC and provide the necessary gate drive power for the MOSFETs. The V_{CC} pin supplies the driver IC logic and sense circuitry. The V_{DRV} pin supplies the gate drive power. TI recommends a 1µF, 10V, X5R or higher ceramic capacitor to bypass V_{CC} to A_{GND}. Connect this ceramic capacitor directly between V_{CC} and A_{GND} on the top side of the PCB. Bypass the V_{DRV} pin to P_{GND} using a 1µF, 10V, X5R ceramic capacitor. Place this ceramic capacitor as close as possible to V_{DRV}. TI recommends to have at least five 10µF, 25V, X7R or higher ceramic capacitors from V_{IN} to P_{GND}.

The device also includes a bootstrap circuit to provide gate drive power for the control FET. Connect a ceramic capacitor (with a value of minimum 100nF, 16V, X5R) between BOOT and PHASE pins to generate the bootstrap supply to drive the control FET . TI recommends to maintain a placeholder for an R_{BOOT} resistor in series with the bootstrap capacitor to slow down the turn on speed of the control FET and reduce voltage spikes on the SW node, if necessary. Evaluate the voltage stress during first prototype development. Adjust the value of R_{BOOT} accordingly. For applications that use 12V or less as the typical input supply voltage, a boot resistor can not be necessary.

6.3.1.1 Undervoltage Lockout (UVLO) Protection

The V_{CC} and V_{DRV} supplies are monitored for UVLO conditions and both control FET and sync FET gates are held low until adequate supply is available. An internal comparator evaluates the V_{CC} and V_{DRV} voltage level,

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and if both are above the UVLO threshold, the device logic becomes active. If V_{CC} or V_{DRV} is less than the UVLO threshold, the gate driver is disabled and the internal MOSFET gates are actively driven low.

At the rising edge of the V_{DRV} voltage, both control FET and sync FET gates are actively held low during V_{DRV} transitions between V_{POR} to $V_{DRV\_UVLO\_RISING}$. This region is referred to as the gate drive latch zone, seen in Figure 6-1. In addition, at the falling edge of the V_{DRV} voltage, both control FET and sync FET gates are actively held low during the $V_{DRV\_UVLO\_RISING}$-V_{DRV_HYS} to V_{POR} transition.

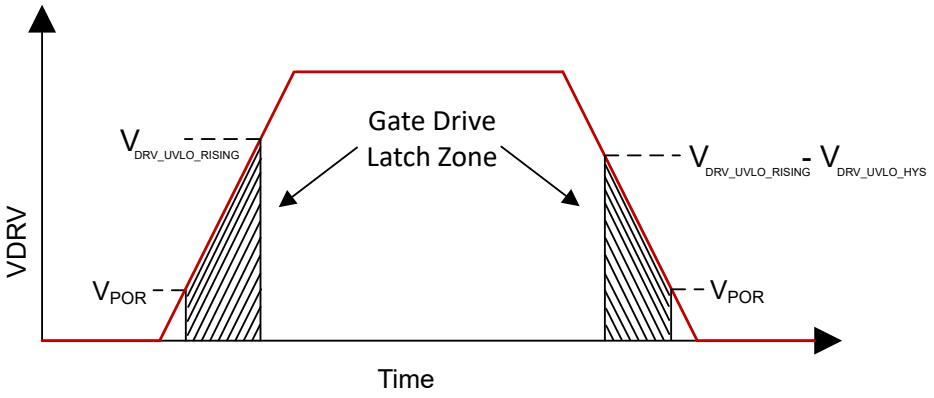

Figure 6-1. UVLO Operation

The CSD967201-Q1 power stage device must be powered up and enabled before the PWM signal is applied. TMON/FLT and PWM are actively held low until Vin is above V_{IH_VIN}, and V_{DRV} exceeds $V_{DRV\_UVLO\_RISING}$ and $t_{Startup\text{-}Delay}$ time has passed. This process enables handshaking between the controller and the power stage to make sure that PWM is not fired until the power stage is ready.

6.3.1.2 Power Up and Down Sequence

V_{IN} and V_{DRV} can be powered up in any sequence. V_{DRV} is connected to V_{CC} with a 2.2Ω resistor.

When V_{DRV} exceeds $V_{DRV\_UVLO\_RISING}$, TMON/FLT and IMON start rising after $t_{Startup\text{-}Delay}$ time has passed. If no faults as described in Section 6.3.7 are detected, TMON goes on to report accurate die temperature and IMON corresponds to the load current.

6.3.2 Power Stage and Gate Drivers

The main power blocks for CSD967201-Q1 are High Side (HS) and Low Side (LS) LDNMOS FETs, and high performance gate drivers. These drivers feature fixed dead-time control to minimize switching losses and switch-node ringing.

6.3.2.1 Integrated Clamp Circuit

CSD967201-Q1 has an integrated clamp circuit that prevents the voltages across the HS and LS FETs from reaching a voltage beyond the safe operating conditions. This triggering of the clamp achieves avalanche free operation and minimizes stress to the FETs.

6.3.2.2 Gate Drivers Power and Control

CSD967201-Q1 has an internal high-performance gate driver IC that features fixed dead-time control for lowest possible switching loss and switch-node ringing reduction.

6.3.2.2.1 Power and Bootstrap Circuit

The gate drivers are powered from the VDRV pin, while the logic controlling them is powered from VCC. The device also includes a bootstrap circuit to provide gate drive power for the control FET. The bootstrap circuitry is able to work with at least a 100nF capacitor (C_{BOOT}) between the BOOT and PHASE pins to generate the bootstrap supply to drive the control FET.

An optional resistor, R_{BOOT}, is used in series with the bootstrap capacitor to slow down the turn on speed of the control FET and reduce voltage spikes on SW, if necessary.

Note that the integrated clamp prevents the voltage across the FETs from exceeding safe operating ratings and serves as the first line of defense.

6.3.3 Enable (EN)

The EN pin is TTL compatible. The device sustains logic level thresholds during all V_{CC} operating conditions between V_{VCC_UVLO} and V_{CC}. In addition, if this pin is left floating, a weak internal pulldown resistor pulls the EN pin below the logic level low threshold. The operational functions of this pin follow the timing diagram outlined in Figure 6-2. A logic level low actively holds both control FET and sync FET gates low. See Section 6.3.5 for details on the operation of the current sensing circuit.

TI recommends to connect the EN pin to controller DRON to allow the controller to reset the fault. Refer to Section 6.3.7 for details on fault behavior.

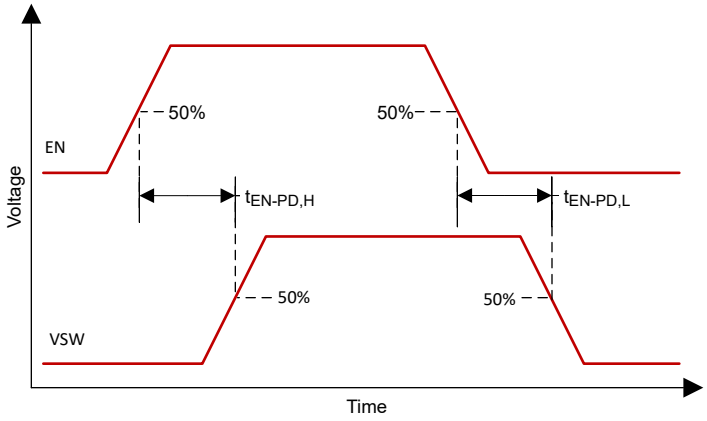

Figure 6-2. CSD967201-Q1 EN Timing Diagram

6.3.4 Pulse Width Modulation (PWM) Control

The input PWM pin controls the switching logic when EN is at logic level high. For normal forced continuous conduction mode operation, PWM is toggled between logic level low and logic level high, and the SW node follows with some propagation delay. A third PWM state is also defined between logic level high and low, the tri-state window. PWM must dwell inside the tri-state window for more than the tri-state hold-off time (t_{3HT}) for this logic level to be registered. The tri-state shutdown propagation delay (t_{3SD}) is inclusive of the tri-state hold-off time. The tri-state mode can be entered by actively driving the PWM input into the tri-state window or the PWM input can be made high impedance and internal current sources can drive the pin voltage to the tri-state voltage, V_{PWMT}.

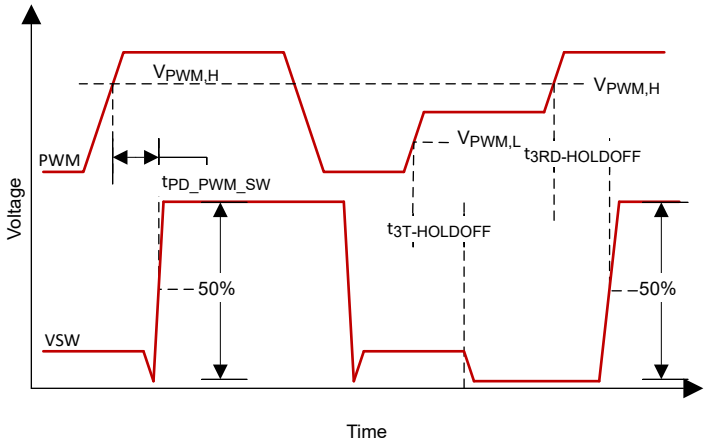

Figure 6-3. PWM Timing Diagram

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6.3.4.1 DCM Operation: Phase Off, Body Braking and Diode Emulation Modes

To support Discontinuous Conduction Mode (DCM) operation, the tri-state logic level enables several related functions depending on the sequence of PWM:

- **Body Braking Mode:** When tri-state mode is first detected both gates are immediately turned off. Assuming the device is switching beforehand, this results in body diode conduction until the main inductor current is driven to 0A. This body diode conduction mode is referred to as body-braking mode and can be used to increase the speed of discharge of the inductor current (for example, to limit the overshoot during a load release transient). Multiple body-braking cycles can occur consecutively as long as PWM goes from tri-state level to low prior to going high.

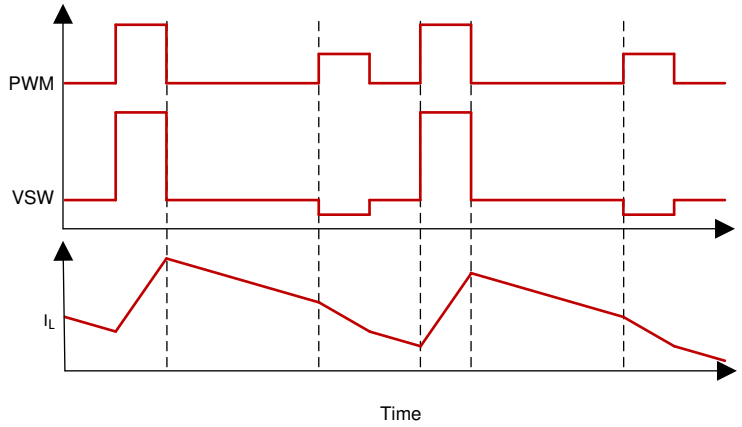

Figure 6-4. Body-Braking Mode

- **Phase Off Mode** If the tri-state level is maintained beyond the complete discharge of the inductor current, this effectively turns off the power stage. This mode is used in multiphase applications to allow dynamic phase shedding to increase the efficiency at light load.

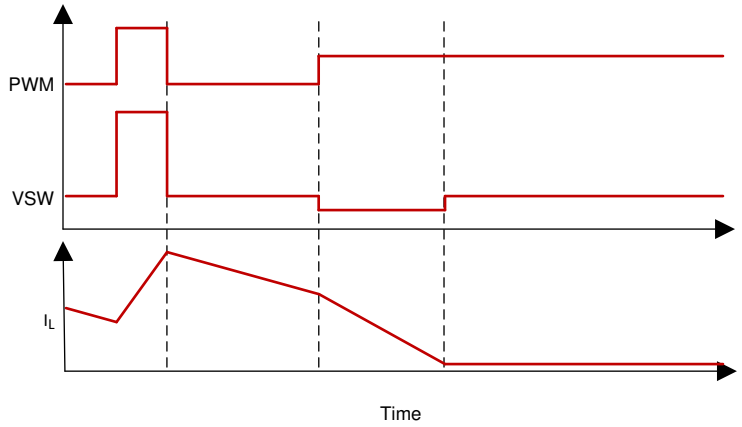

Figure 6-5. Phase Off Mode:

6.3.4.2 PWM State Diagram

Figure 6-6 demonstrates how the various operating states are connected and which transitions are allowed along with a couple of examples of common scenarios.

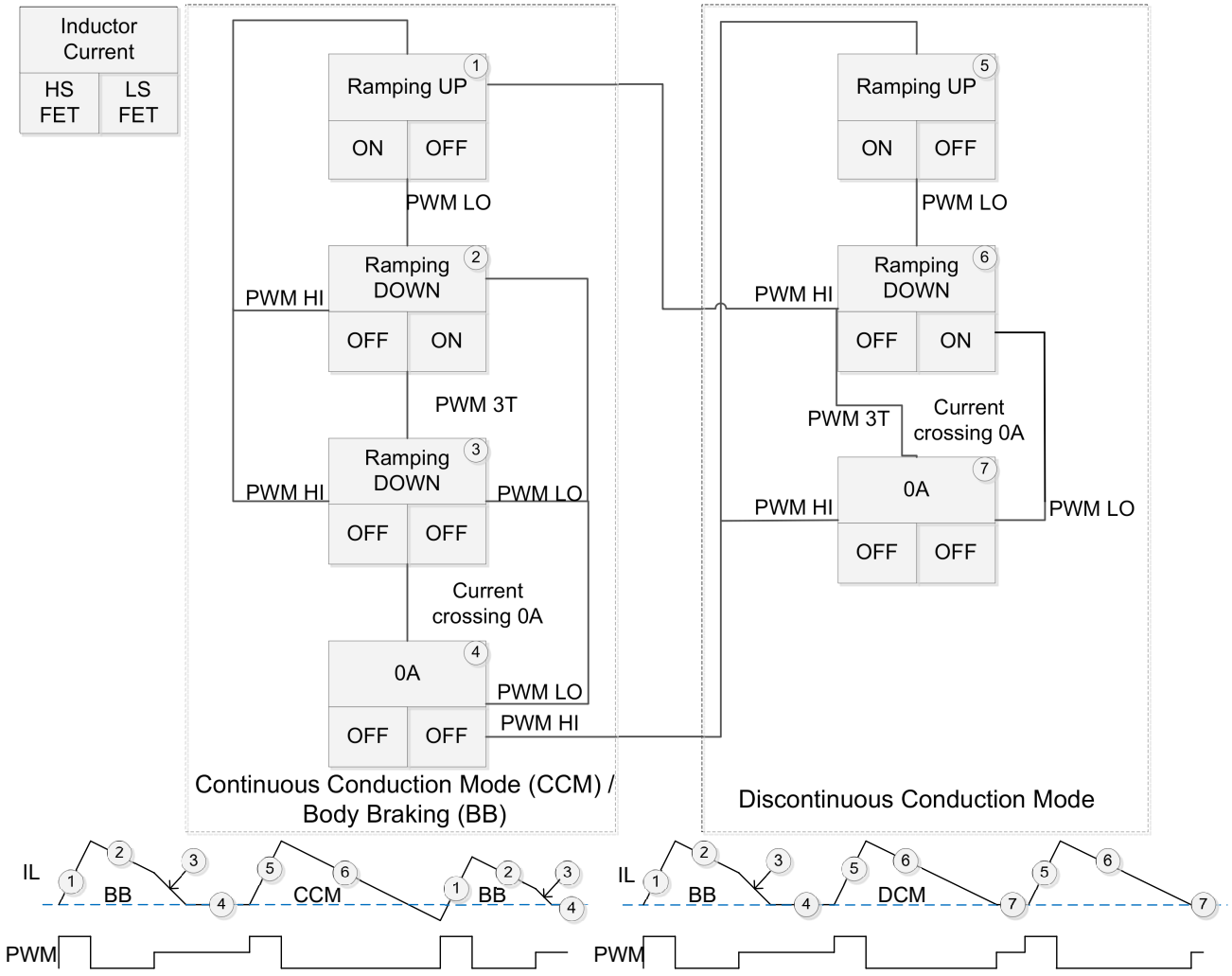

Figure 6-6. PWM State Diagram

Both V_{PWML} and V_{PWMH} threshold levels are designed to accommodate both 3.3V and 5V logic controllers.

6.3.5 Current Sense Output (IMON)

CSD967201-Q1 features integrated inductor current sensing. The device outputs a current that is proportional to the current flowing through the output inductor.

When a fault occurs, the power stage first flags the controller by raising the voltage of the TMON/FLT pin to 3V. The expected behavior of the controller to a power stage fault is to shut down the system by driving PWM into the tri-state window for all phases.

6.3.6 Temperature Monitoring - TMON (Thermal Monitor)

During normal operation the output TMON/FLT pin is a highly accurate analog temperature measurement of the power stage die temperature. The TMON/FLT pin has no local bypass capacitor requirements, but can drive up to 470pF of capacitance to accommodate controller side filtering of the TMON/FLT pin for enhanced accuracy and noise immunity.

The TMON/FLT pin also includes a built in ORing function. When connecting TMON/FLT pins of more than one device together, the TMON/FLT bus automatically reads the highest TMON/FLT voltage among all devices. This connection simplifies the temperature sense and fault reporting design for multi-phase applications, where a single line TMON/FLT bus can be used to tie the TMON/FLT pins of all phases together and the system can monitor temperature of the hottest device.

The TMON/FLT output also serves as a fault output and is driven to 3V. See Section 6.3.7 for details.

6.3.7 Faults and Protection Mechanisms

CSD967201-Q1 incorporates multiple fault detection and protection mechanisms for conditions that cause detriment to the system or the IC such as overtemperature.

CSD967201-Q1 has built-in overtemperature protection (described in Section 6.3.7.7), over current protection (described in Section 6.3.7.5), and high-side short detection (described in Section 6.3.7.8). Only catastrophic faults such as overtemperature fault and high side short are flagged to the controller by driving TMON/FLT to 3V.

Table 6-1. CSD967201-Q1 TMON/FLT and IMON Fault Response Summary

CSD967201-Q1			
FAULT	**FAULT RESPONSE**	**POWER STAGE IMMEDIATE RESPONSE ON TMON/FLT AND IMON**	
		TMON/FLT	**IMON**
V_{DRV}, V_{CC}, below UVLO	Ignore PWM, HS and LS FET Off, PWM pulled low with weak pulldown	HiZ (allow good phases to drive TMON)	Hi-Z
V_{BOOT_UVLO}	Do not turn on HS, turn on LS if PWM low from controller	Normal operation	Normal operation
$V_{IN\ UVLO}$	Ignore PWM, HS and LS FET Off	HiZ (allow good phases to drive TMON)	Hi-Z
IOC_{VALLEY} over current valley	Keep LS FET on (or tri-state mode) until inductor current falls below valley current limit and PWM is not high	Normal operation	Normal operation
IOC_{PEAK} over current peak	Truncate HS pulse, turn on LS for min-off-time, respond to PWM if PWM=LOW/TRISTATE	Normal operation	Normal operation
Negative over current	LS and HS are turned off at NOC limit until the NOC hysteretic limit, cycle is repeated if NOC persists	Normal operation	Normal operation
Over temp	Ignore PWM, HS and LS FET Off until $T_{SHUTDOWN}$ falling threshold, then respond to PWM	Set to 3V (Fault)	Normal operation
High Side Short (HSS)	Keep LS FET on	Latch to 3V (Fault)	Normal operation
Fault recovery mechanism	• Over temp is cleared after the temperature falls below the threshold because the fault is not latched • Fault recovery is automatic for the power stage for all states except HSS • Power cycle to recover from HSS fault, because the fault is latched		

6.3.7.1 VDRV Fault Detection

At startup, PWM is low with a weak pulldown and nothing is active on the device. During normal operation, if the V_{DRV} voltage sags below $V_{DRV\_UVLO\_RISING}$-$V_{DRV\_UVLO\_HYS}$, CSD967201-Q1 turns off the LS and HS FET and ignores the PWM input signal, while IMON and TMON are in tri-state mode. However, if V_{DRV} does drop below V_{POR}, CSD967201-Q1 does a full power down. In multiphase operation, TMON is driven by other phases that are in normal operation as TMON/FLT continues to report the temperature allowing the the voltage rail to still be powered by phases not in fault.

6.3.7.2 VCC Fault Detection

During normal operation, if the V_{CC} voltage sags below V_{CC_UVLO}, CSD967201-Q1 turns off the LS and HS FET and ignores the PWM input signal, while IMON and TMON are in tri-state mode. In multiphase operation, TMON is driven by other phases that are in normal operation as TMON/FLT continues to report the temperature allowing the voltage rail to still be powered by phases not in fault.

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6.3.7.3 BOOT_FAULT Undervoltage

CSD967201-Q1 detects a fault whenever V_{BOOT} falls under V_{BOOT_FAULT}. This fault detection is only active after the first PWM high is detected, to avoid the part getting stuck in a fault condition during initial power up.

Upon detection of this fault, CSD967201-Q1 does not turn on the HS, and turns on the LS if PWM is low from the controller. IMON and TMON are normal operation. This fault is V_{BOOT} rises above V_{BOOT_FAULT}.

6.3.7.4 VIN Undervoltage

CSD967201-Q1 detects a fault whenever V_{IN} falls under V_{INUVLO}. This fault detection is only active after the first PWM high is detected, to avoid the part getting stuck in a fault condition during initial power up.

Upon detection of this fault, CSD967201-Q1 TMON/FLT is put into tri-state mode. The power stage then turns off the HS and LS FET by ignoring PWM. IMON is Hi-Z and TMON output is normal operation. This fault is cleared when V_{IN} is above V_{INUVLO}.

6.3.7.5 High Side Overcurrent (IOC) Protection

This power stage is equipped with two layers of over current protection, IOC_{VALLEY} and IOC_{PEAK}.

When the current through the control FET exceeds the current limiting over current valley threshold (IOC_{VALLEY}), but does not return to the IOC_{VALLEY} current limit during the LS FET on time, the LS FET on time is extended until the inductor current is below the IOC_{VALLEY} limit. If the PWM level is high when the IOC_{VALLEY} limit is crossed, the HS FET is turned on for the remaining duration of the PWM high signal, with SW duration of a minimum of TON_{MIN}. It is possible that the LS will be kept on until the next PWM high, effectively skipping a PWM high pulse. IMON and TMON are normal operation.

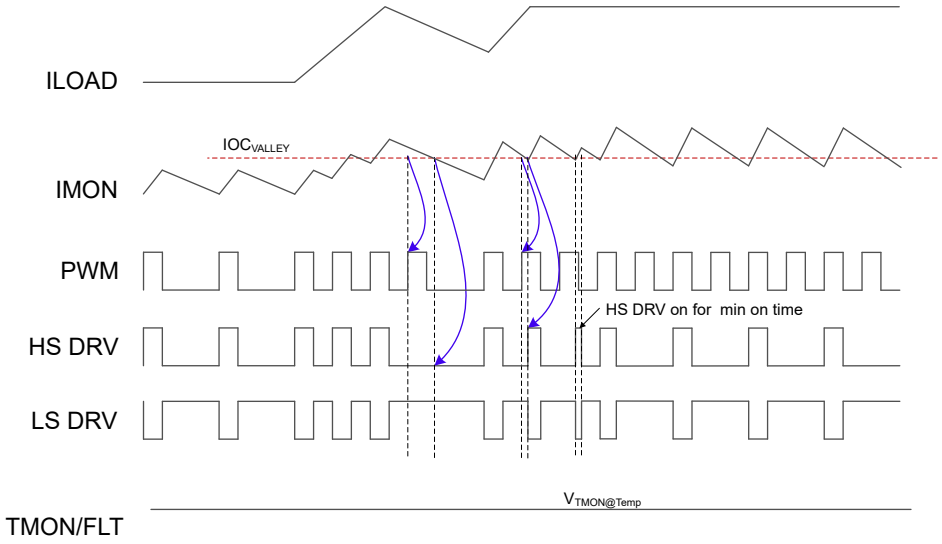

Figure 6-7. IOC_{VALLEY} Protection

In cases of large transients, or when the inductor ripple increases due to inductor saturation and lower inductance, a second current limit is implemented (IOC_{PEAK}). When the current through the control FET exceeds the current limiting over current peak threshold (IOC_{PEAK}) the power stage automatically truncates the SW pulse that cycle by turning off the control FET and turning on the sync FET (as if a PWM low is detected). IMON and TMON are normal operation.

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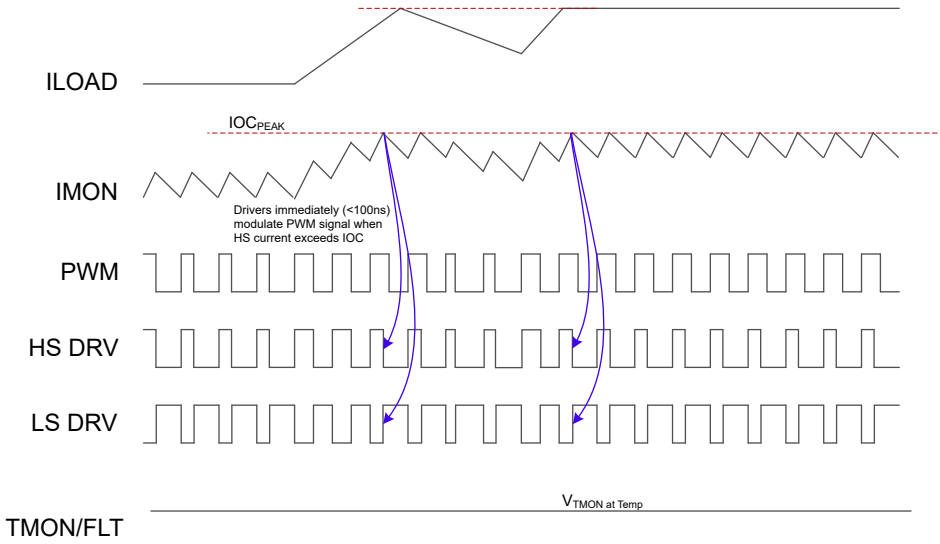

Figure 6-8. IOC_{PEAK} Protection

6.3.7.6 Negative Over Current (NOC) Protection

This power stage is equipped with negative over current (NOC) protection. when the current through the LS FET exceeds the NOC threshold, the power stage automatically turns off the LS and HS FET until the NOCH threshold is reached. This cycle repeats until the NOC threshold is no longer reached, or until the controller detects a fault (most likely overvoltage on the output). IMON and TMON are normal operation.

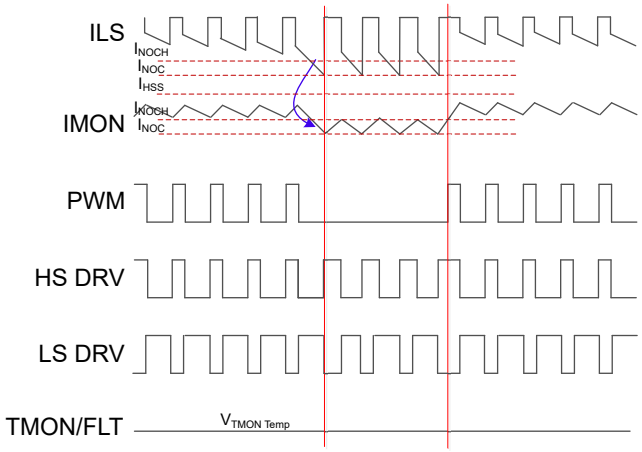

Figure 6-9. NOC Protection

6.3.7.7 Overtemperature (OT) Protection

An over temperature fault occurs when the die temperature reaches the thermal shutdown temperature (see the *Electrical Characteristics* table). The power stage automatically reacts to an over temperature fault to avoid damage.

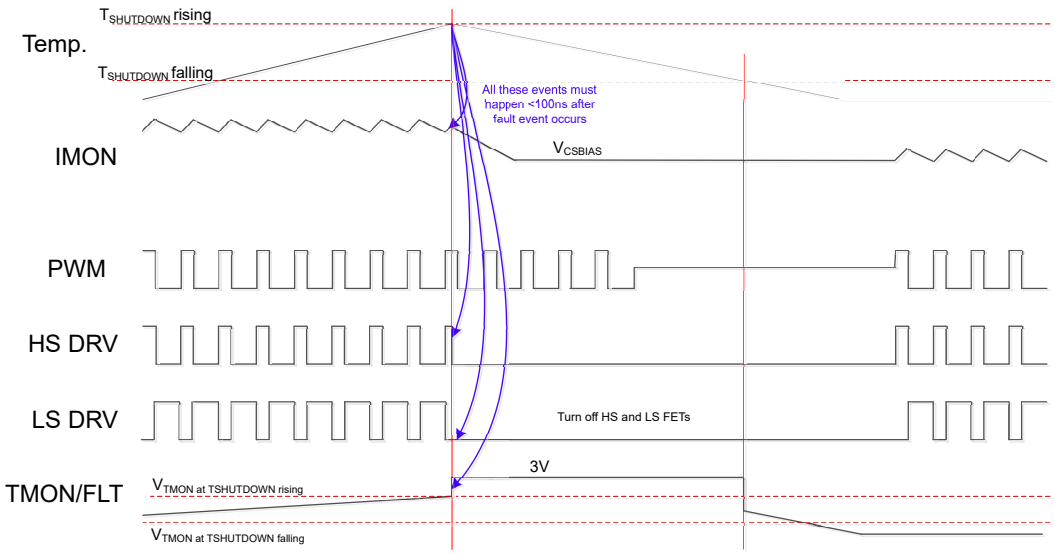

Figure 6-10. OT Protection

When the power stage detects the overtemperature event, the power stage automatically turns off both the control FET and the sync FET and sets TMON/FLT to 3V. If the temperature falls below the overtemperature threshold hysteresis band, the driver again responds to PWM commands and the TMON/FLT pin returns to normal operation. A weak pulldown resistance allows TMON/FLT to return to normal operation from a fault so there is a significant delay before the TMON/FLT output reports the correct temperature. As with any event that interrupts the normal PWM behavior (see Section 6.3.3 and Section 6.3.1.1), design the application to disable the controller when the controller detects an OT event and to engage the soft-start sequence to prevent potential damage to the power stage or the system.

6.3.7.8 High-Side Short (HSS) Detection

This power stage is equipped with high-side short detection circuitry. A high-side short is detected by monitoring the negative current (drain to source current) flowing through the sync FET when PWM is low. If a high side short occurs, the current in the sync FET builds rapidly due to the shoot-through current when PWM is low.

When the negative current exceeds the HSS threshold specified in the *Electrical Characteristics* table, the TMON/FLT flag is latched to 3V, the HS FET is turned off and the LS FET is turned on.

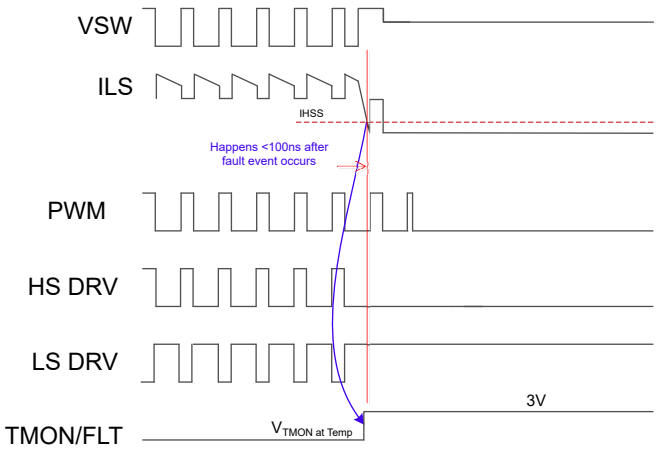

Figure 6-11. HSS Protection

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6.4 Device Functional Modes

Undervoltage Lockout (UVLO)

When VCC is lower than the specified UVLO threshold. Both the high side and low side FETs are off.

Active Switching (Tri-state Mode)

In this mode of operation, PWM is in tri-state mode. Both the high side and low side FETs are off.

Active Switching (Low)

In this mode of operation, PWM is at logic level low. The high side FET is off, and the low side FET is on.

Active Switching (High)

In this mode of operation, PWM is at logic level high. The high side FET is on, and the low side FET is off.

Fault

The power stage device is in a fault state. TMON/FLT is pulled high based on the kind of fault. Both the high side FET and low side FET are off.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The CSD967201-Q1 power stage is a highly optimized design for synchronous buck applications using monolithic enabled circuit IP with a 5V gate drive. The control FET and sync FET silicon are parametrically tuned to yield the lowest power loss and highest system efficiency. As a result, a rating method is used that is tailored towards a more systems-centric environment. The advanced gate driver techniques make sure of avalanche free operation and maintain very fast switching of the power MOSFETs for improved efficiency. System-level performance curves such as power loss, safe operating area, and normalized graphs allow engineers to predict the product performance in the application.

In addition, this power stage incorporates integrated temperature and inductor sensing. This technology allows extremely accurate sensing of both temperature and current for high-end applications without the need for additional board components that add design complexity, cost, and space requirements to the design.

7.1.1 Current Rating

CSD967201-Q1 operates with a wide range of applications including highly dynamic load scenarios. For this reason, both a peak continuous current rating and a recommended DC current rating are specified. The peak continuous rating defines the peak transient load currents at which the device can operate. Operation above this level initiates the over-current protection and results in current-limiting behavior or shutdown of the device as described in Section 6.3.7. The recommended DC current rating defines the maximum continuous load current at which the device can safely operate.

7.1.2 Integrated Current Sensing

The CSD967201-Q1 power stage incorporates state-of-the-art inductor current sensing. This technology uses temperature compensated on-resistance based sensing of the sync FET current during the on-state (PWM logic level low) and emulates the inductor current during the HS FET conduction.

As a result, the instantaneous inductor current can be calculated based on Equation 1.

$$I_L = \frac{(I_{IOUT})}{5} \quad (1)$$

where

- I_L is the instantaneous inductor current in A
- I_{IOUT} is the current measured at the IOUT pin in uA
- 5 is the conversion factor coefficient of the IOUT pin signal

The smart sensing technology automatically adjusts to changes in the input voltage, output voltage, temperature, bias voltage, output inductance, and switching frequency to produce a very low error in the emulated signal during steady-state operation. During a tri-state condition, the current sense ramps down to 0A and remains at 0A until the device receives a PWM signal. In the tri-state condition, the device turns off the synchronization FET so that the ramp-down rate of the IOUT pin signal increases slightly to accurately represent the additional voltage drop due to the body diode conduction. This current sensing scheme enables the following features:

- Highly accurate current sensing over a wide operating range
- Temperature compensated sensing eliminates the need for complex thermistor based temperature compensation

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- Temperature compensation intrinsic to each part enabling multiphase designs to more accurately share current
- Simplified PCB design
- Enables the use of low DCR inductors for improved system-level efficiency

7.1.3 VDS Ratings

DC rating is the VDS that can be applied to the device in operation over extended period of time. Transient rating is the maximum VDS that can be applied to the device in operation over a short period of time, as specified below.

Derating from absolute max specifications is accounted for. Additional de-rating is not required if the device is operated within the shown safe operating area.

Probe VDS at the power stage pins using a high bandwidth differential probe. Because this measurement is prone to board parasitics, layout, routing, and so on, probing the device at the power stage pins between PVIN and SW for the HS FET and between SW and PGND for the LS FET is essential to get an accurate reading.

7.1.4 Power Loss Curves

In an effort to simplify the design process for engineers, Texas Instruments has provided measured efficiency and power loss performance curves. The power loss curves plot power loss as a function of load current. This curve is measured by configuring and running the power stage as the curve is in the final application. The measured power loss is the power stage power loss which consists of both input conversion loss and gate drive loss.

$$\text{Power loss} = (V_{IN} \times I_{IN}) + (V_{DRV} \times I_{DRV}) - (V_{SW\_AVG} \times I_{LOAD}) \quad (2)$$

In this case, V_{DRV} and I_{DRV} refer to the voltage and current of both the V_{CC} and V_{DRV} combined. The power loss curve is measured under isothermal test conditions at a junction temperature of T_J = 25°C.

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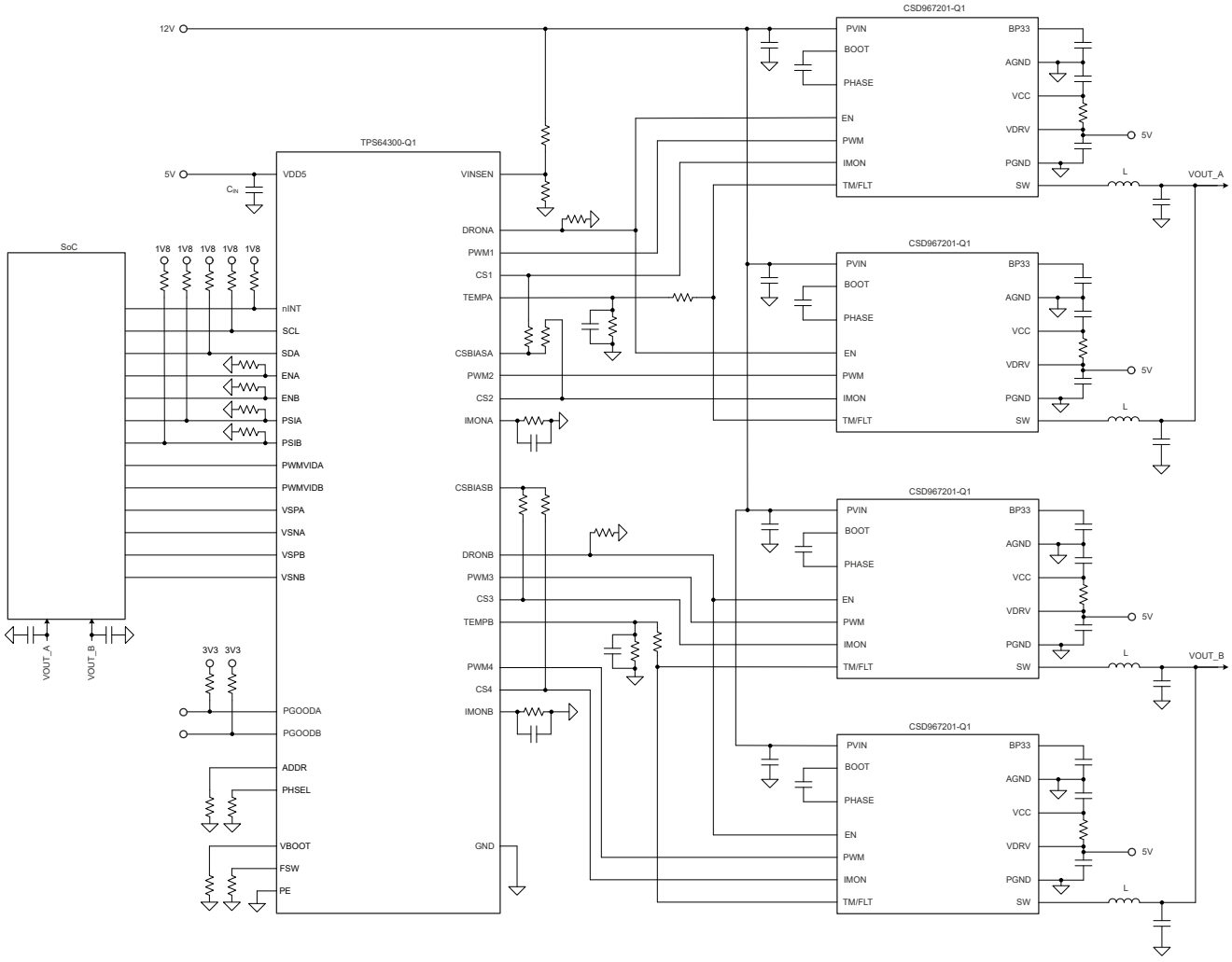
7.2 Typical Application



Note: this is a conceptual drawing only. Actual designs can require additional components not shown.

Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

The following table summarizes the key design requirements for this application.

Table 7-1. Design Parameters

PARAMETER	VALUE
Input voltage (V_{IN})	6V – 19V
Bias supply (V_{DRV} and V_{CC})	5V
Power loss	< 5W at 30A over full VIN operating range
Power stage switching frequency (F_{SW})	650kHz
Output inductor (L_{OUT})	85nH
Junction temperature (T_J)	25°C
Output current (I_{OUT})	60A for 10ms
	90A for 10µs
Output voltage (V_{OUT})	0.6V – 1.3V

ADVANCE INFORMATION

Table 7-2. Recommended Passive Components and Board Level Parasitic Tolerance

		MIN	NOM	MAX	UNIT
C_{IN}	IN Bypass capacitance	10			µF
C_{BOOT}	BOOT capacitance	0.1	0.22	0.47	µF
C_{VCC}	VCC input bypass capacitance	0.3	1		µF
C_{BP33}	BP33 input bypass capacitance	47	100	150	nF
C_{VDRV}	VDRV input bypass capacitance	0.3	1		µF
C_{IMON}	External parasitic capacitance seen by IMON	10		100	pF
L	Switch Node coil inductance	20		220	nH
R_{BOOT}	BOOT resistance	0	0	5	Ω
$R_{IMON-CSBIAS}$	Resistance value that can be placed between pins		1000		Ω
C_{PWM}	Parasitic capacitance on PWM line			200	pF
$R_{TMON/FAULT}$	Resistance value that is placed from the pin to GND		20		kΩ
$C_{TMON/FAULT}$	Parasitic capacitance on TMON line			470	pF

7.2.2 Detailed Design Procedure

Output Inductor Selection

A smaller inductance yields better transient performance, but leads to higher ripple current and lower efficiency. Higher inductance has the opposite effect. 85nH is chosen for the output inductor in the typical example as the value achieves a good balance between transient performance and output ripple.

Input Capacitor Selection

Having input capacitance helps minimize the input voltage ripple. TI recommends to use five 10µF, 0805, 10V, ceramic capacitors to reduce the input continuous current stress seen by each capacitor.

Switching Frequency Selection

Select switching frequency depending on intended use case, in this case 650kHz.

Duty Cycle Selection

Select duty cycle using the equation of a buck converter as follows.

$$D = V_{OUT}/V_{IN} \quad (3)$$

7.2.3 Application Curves

The application curves are shown in the *Typical Characteristics* for efficiency and power loss. The operating conditions for the figures are V_{IN} = 12V, $V_{DRV, VCC}$ = 5V, V_{OUT} = 0.8V, f_{SW} = 650kHz, L_{OUT} = 85nH, I_{OUT} = 0A to 60A, T_J = 25°C, unless specified otherwise.

7.3 Power Supply Recommendations

CSD967201-Q1 is designed to operate with a well-regulated 6V to 19V input supply on the VIN pin. A well-regulated 5V input supply is required on the VDRV pin.

CSD967201-Q1 provides CSD967201-Q1 BOOT-SW supply. Connect a boot capacitor, and optionally boot resistor, to control the turn-on slew rate.

Powering on the controller or power stage first in sequence is safe. PWM is an input pin. IMON and TMON/FLT are output pins.

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7.4 Layout

7.4.1 Layout Guidelines

7.4.1.1 Recommended Schematic Overview

Several critical components must be used in conjunction with this power stage device. Figure 7-2 shows a CSD967201-Q1 schematic example with the critical components needed for proper operation.

- C_{BOOT}: Bootstrap capacitor
- R_{BOOT}: Bootstrap resistor (optional, most likely not needed)
- C_{BP33}: Filter capacitor for BP33
- C_{VCC}: Bypass capacitor for V_{CC}
- C_{VDRV}: Bypass capacitor for V_{DRV}
- R_{VCC}: Filter resistor between V_{DRV} and V_{CC}
- C_{IN1}: Bypass capacitor (critical to be close to V_{IN} pins) to help with ringing reduction
- C_{IN2}, C_{IN3}, and C_{IN4}: Bulk bypass capacitors for V_{IN}
- C_{SNUB}: Snubber capacitor (optional, most likely not needed)
- R_{SNUB}: Snubber resistor (optional, most likely not needed)

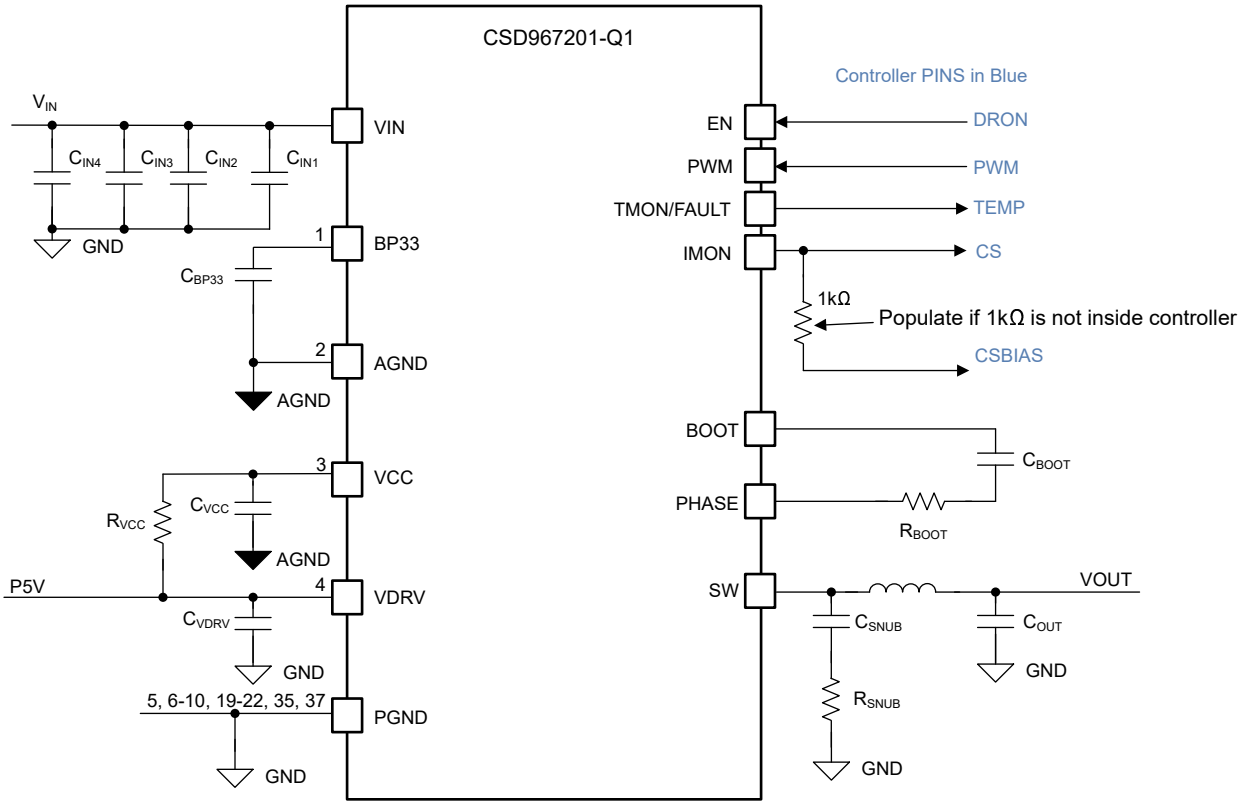

Figure 7-2. Recommended Design Schematic

CSD967201-Q1 has been optimized for 12V input applications. For 12V input voltage, good layout practices typically eliminate the need for external components to help control the voltage stress due to switch-node ringing. However, Texas Instruments always recommends including placeholders for the components R_{BOOT}, C_{SNUB} and R_{SNUB} for new designs to give the designer options to control ringing without re-designing the PCB in case the layout cannot be optimized. For applications that are intended for greater than 12V input, these components can be necessary to make sure of proper voltage margin in the design. Make sure to verify the voltage margin during the validation phase of any new development.

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7.4.1.2 Recommended PCB Design Overview

There are two key system-level parameters that can be addressed with a proper PCB design: electrical and thermal performance. Properly optimizing the PCB layout yields maximum performance in both areas. A brief description on how to address each parameter is added in the following sections.

7.4.1.3 Electrical Performance

CSD967201-Q1 has the ability to switch at voltage rates greater than 10 kV/µs. The PCB layout design, placement of the input capacitors, inductor, and output capacitors are key factors that must be optimized in layout for optimum performance.

- The placement of the input capacitors relative to V_{IN} and P_{GND} pins of CSD967201-Q1 device hold the highest priority during the component placement routine. Make sure to minimize these node lengths. Because of this, placing ceramic input capacitors as close as possible to the V_{IN} and P_{GND} pins (see *Recommended PCB Layout* section) is advisable. In multi-phase designs, the available area close to the power stage on the top side is typically limited. TI recommends that one 1µF, 0402, 50V, ceramic capacitor be placed on the top side of the board as close as possible to V_{IN} and P_{GND} pins. In addition, placing a minimum of 40µF of bulk ceramic capacitance as close as possible to each CSD967201-Q1 in a design is advisable. In high-density multiphase designs, TI recommends to use three 22µF, 0805, 16V, ceramic capacitors placed on the bottom layer directly beneath the power stage.
- For the bootstrap capacitor, C_{BOOT}, the recommendation is to place a ceramic capacitor with a minimum value of 0.1µF, 0402, 16V, as close as possible to the BOOT and BOOTR pins.
- TI recommends to place the switch node of the output inductor relatively close to the power stage CSD967201-Q1 V_{SW} pins. Maintaining the V_{SW} connection area as short and wide as feasible to reduce PCB conduction loss and reduce the switching noise level is key.[1]

7.4.1.4 Thermal Performance

Because CSD967201-Q1 has the ability to use the GND planes as the primary thermal path, TI recommends to use thermal vias to draw heat from the device into the system board. The following three design strategies help minimize the amount of solder that often wicks down the via barrel:

- Intentionally separate the vias to avoid a cluster of holes in a given area.
- Use the smallest drill size allowed. The example in Section 7.4.2 includes vias with a 0.25mm diameter drill hole and a 0.5mm diameter capture pad.
- Tent the opposite side of the via with solder-mask.

The number and drill size of the thermal vias align with the end user's PCB design rules and manufacturing capabilities. The thermal vias also act as the main GND return path for the device. A typical via has a DC current handling capability range between approximately 2A and 3A. Use this estimate to calculate the number of GND vias to place beneath and near the power stage. For example, for a 40A design, place 20 GND vias beneath and beside the power stage.

[1] Keong W. Kam, David Pommerenke, "EMI Analysis Methods for Synchronous Buck Converter EMI Root Cause Analysis", University of Missouri – Rolla

7.4.2 Layout Example

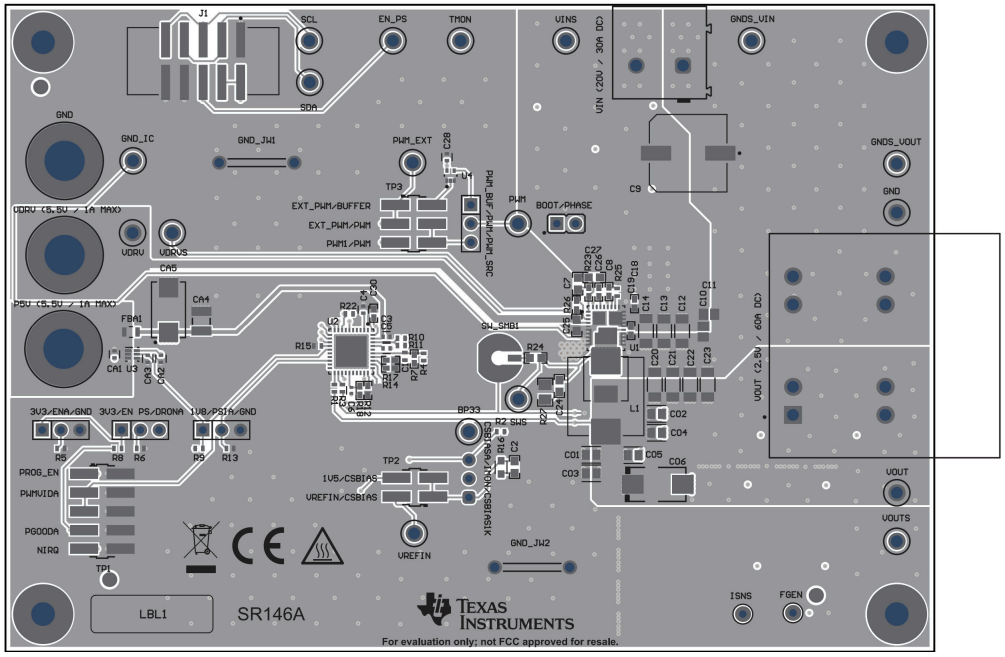

Figure 7-3. Recommended PCB Layout Top Layer (Top Down View)

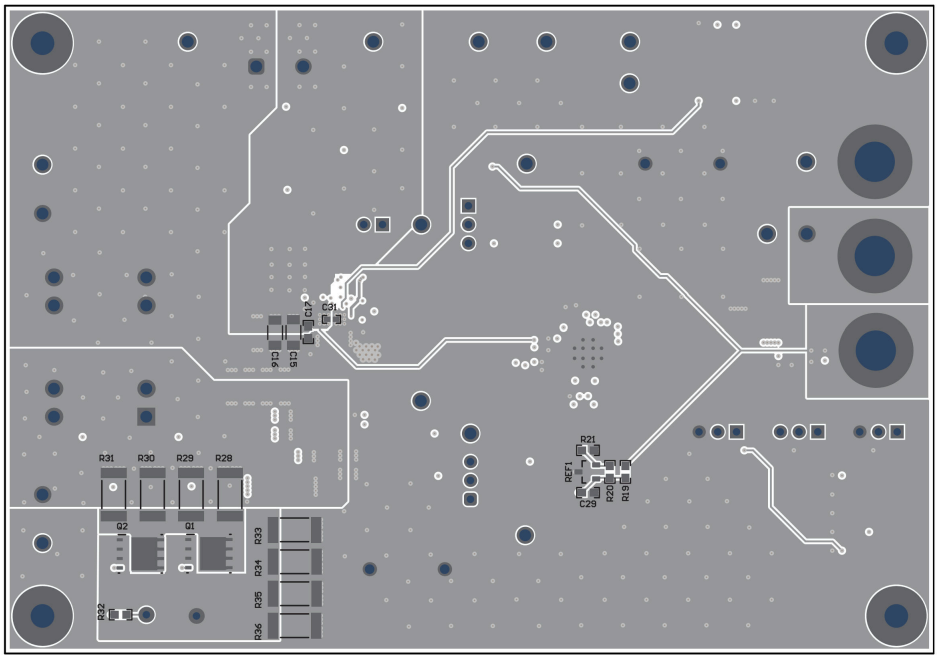

Figure 7-4. Recommended PCB Layout Bottom Layer (Bottom View)

7.4.3 Multiphase Layout Considerations

For applications that require multiple power stages driven in parallel for a single rail, follow these additional layout guidelines.

- All power stages and the associated controllers must share a common ground.
  - Make sure that Layer 2 of the board is a solid ground plane.
- Route the IMON and IMONREF return traces to the controller CS# and CSBIAS pins on a quiet inner layer.

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- The recommended distance from the controller to the closest power stage is no smaller than 800 mils.
- Phase-to-phase noise coupling can often be reduced by adjusting settings in the controller rather than board level layout changes. Verify the existence of phase-to-phase noise coupling prior to completion of board design.

7.4.4 Footprint Compatibility

CSD967201QVDKRQ1 is designed to be footprint-compatible with other similar automotive standard 5mm × 6mm × 0.75mm power stages. See Section 10 for mechanical dimensions for footprint compatibility.

8 Device and Documentation Support

8.1 Device Support

8.1.1 Third-Party Products Disclaimer

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8.2 Documentation Support

8.3 Receiving Notification of Documentation Updates

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8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

DATE	REVISION	NOTES
November 2025	*	Initial release

ADVANCE INFORMATION

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/Ball material (4)	MSL rating/Peak reflow (5)	Op temp (°C)	Part marking (6)

(1) **Status:** For more details on status, see our product life cycle.
(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.
(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.
(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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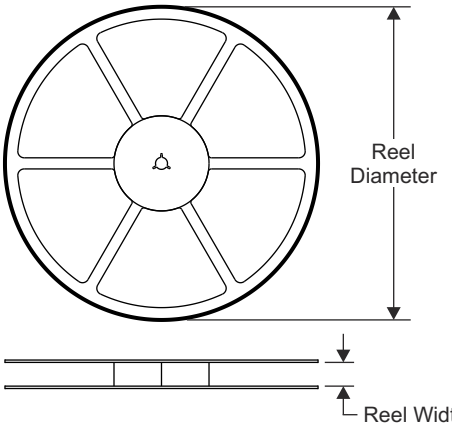
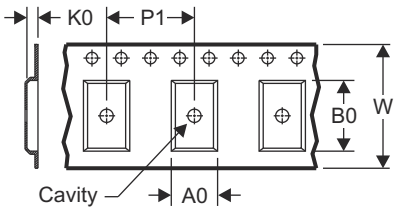
ADVANCE INFORMATION

10.1 Tape and Reel Information

REEL DIMENSIONS

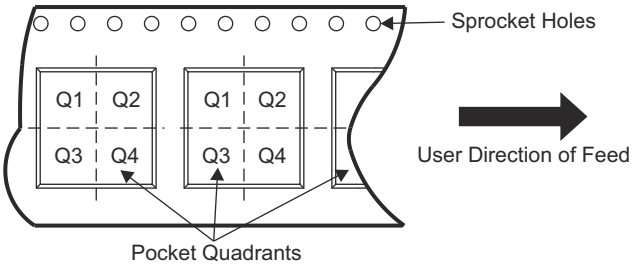


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

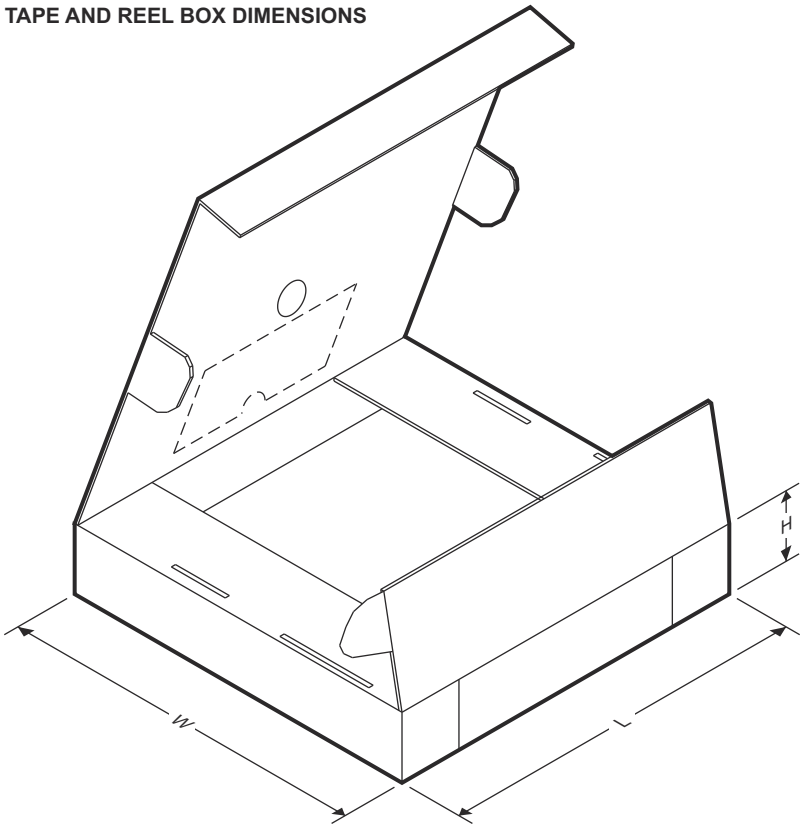
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD967201QVDKRQ1	WQFN-FCRLF	VDA	38	3000	330	12.4	5.30	6.30	1.20	8.00	12.00	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



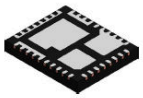
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD967201QVDKRQ1	WQFN-FCRLF	VDA	38	3000	367	367	38

ADVANCE INFORMATION

ADVANCE INFORMATION

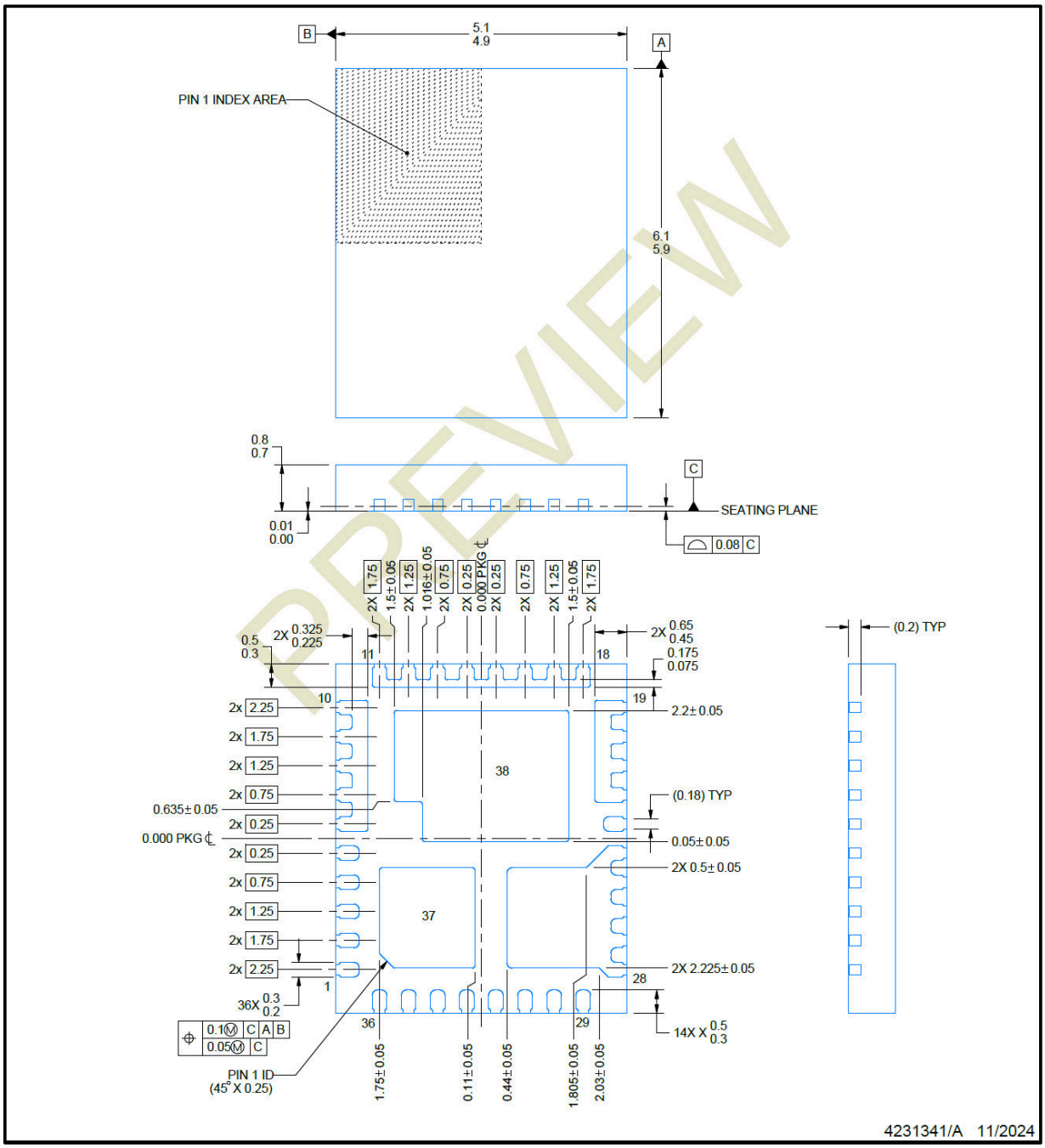
PACKAGE OUTLINE

VDK0038A



WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

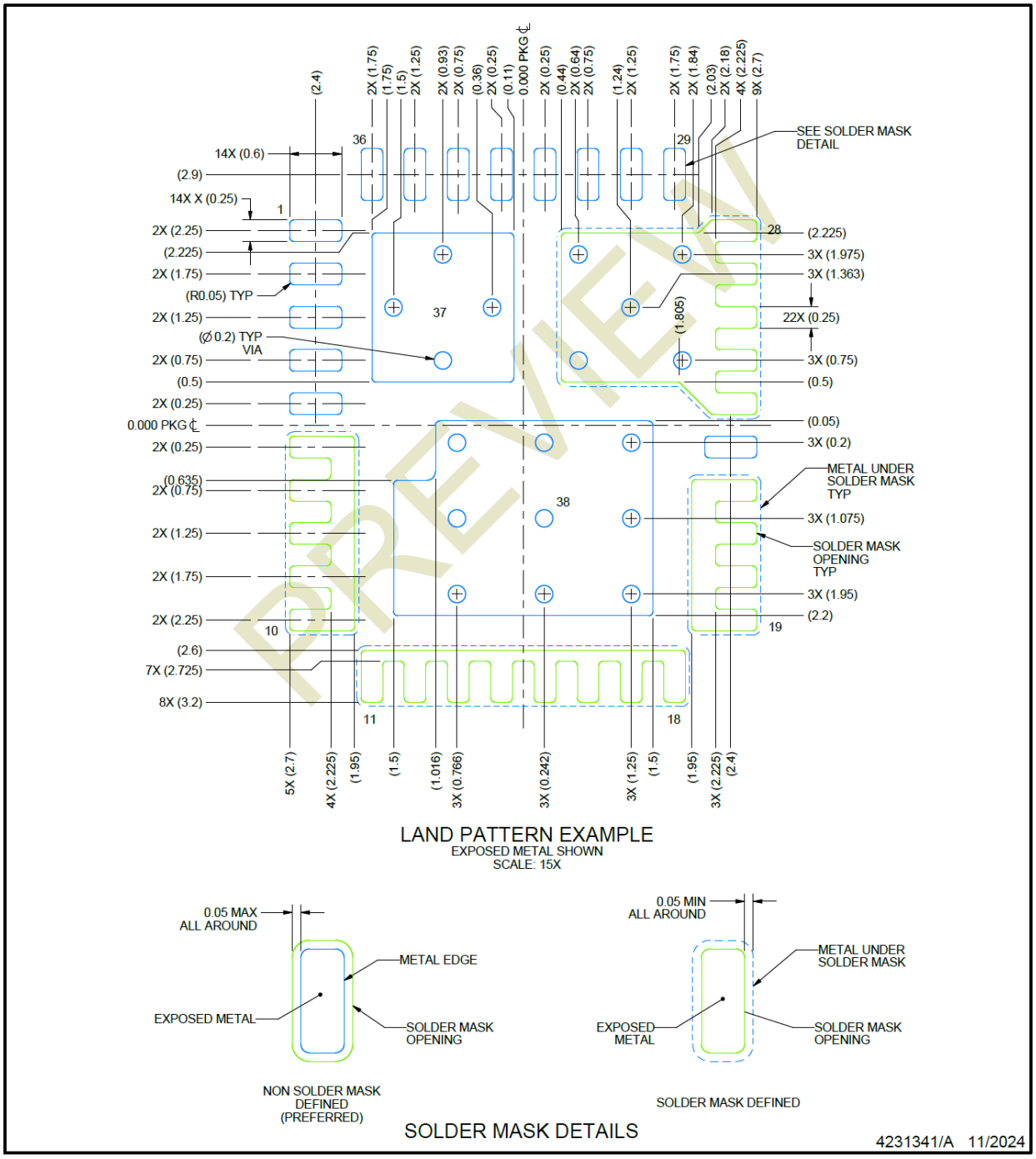
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

VDK0038A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

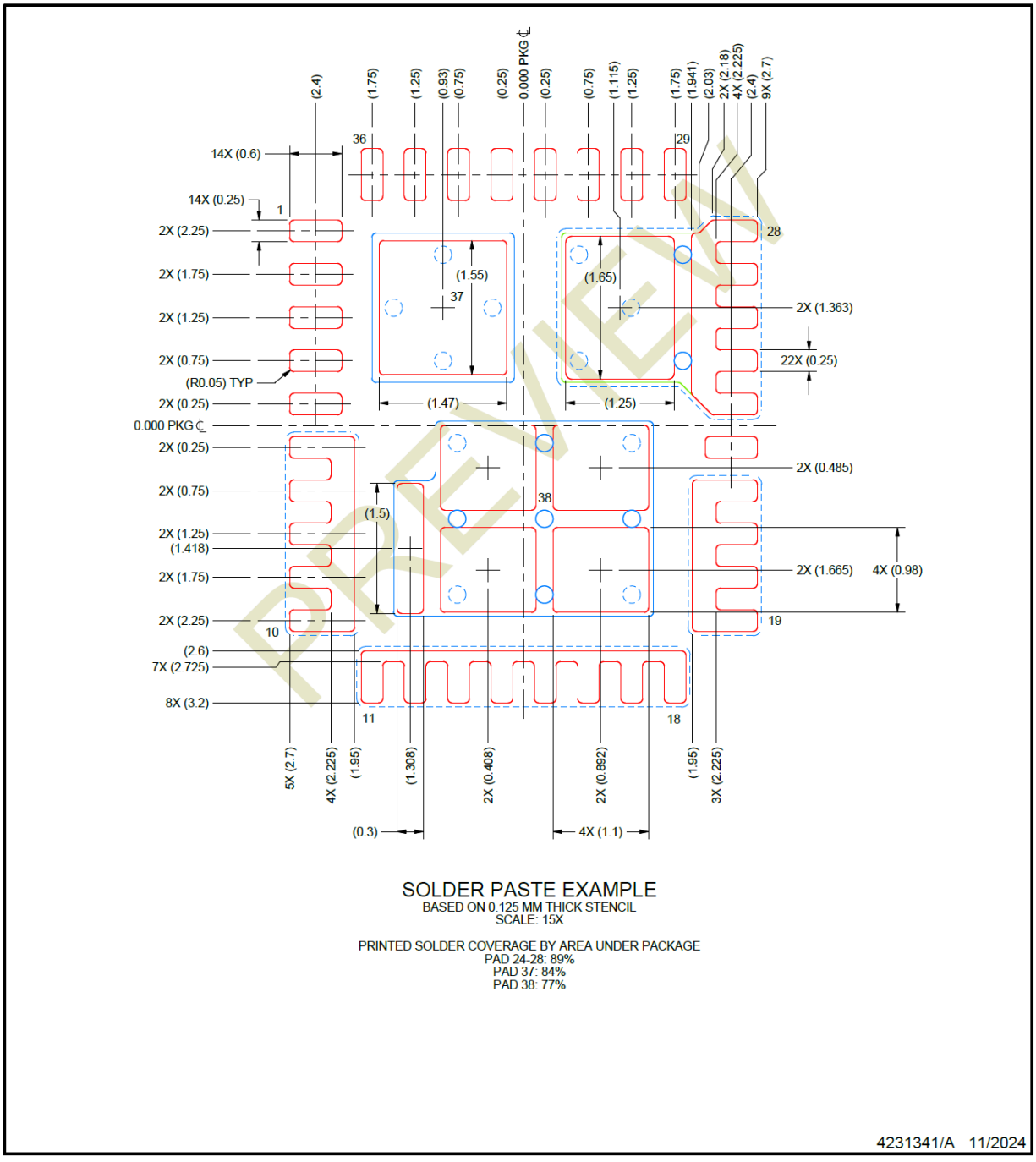
ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

VDK0038A

WQFN-FCRLF - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Last updated 10/2025