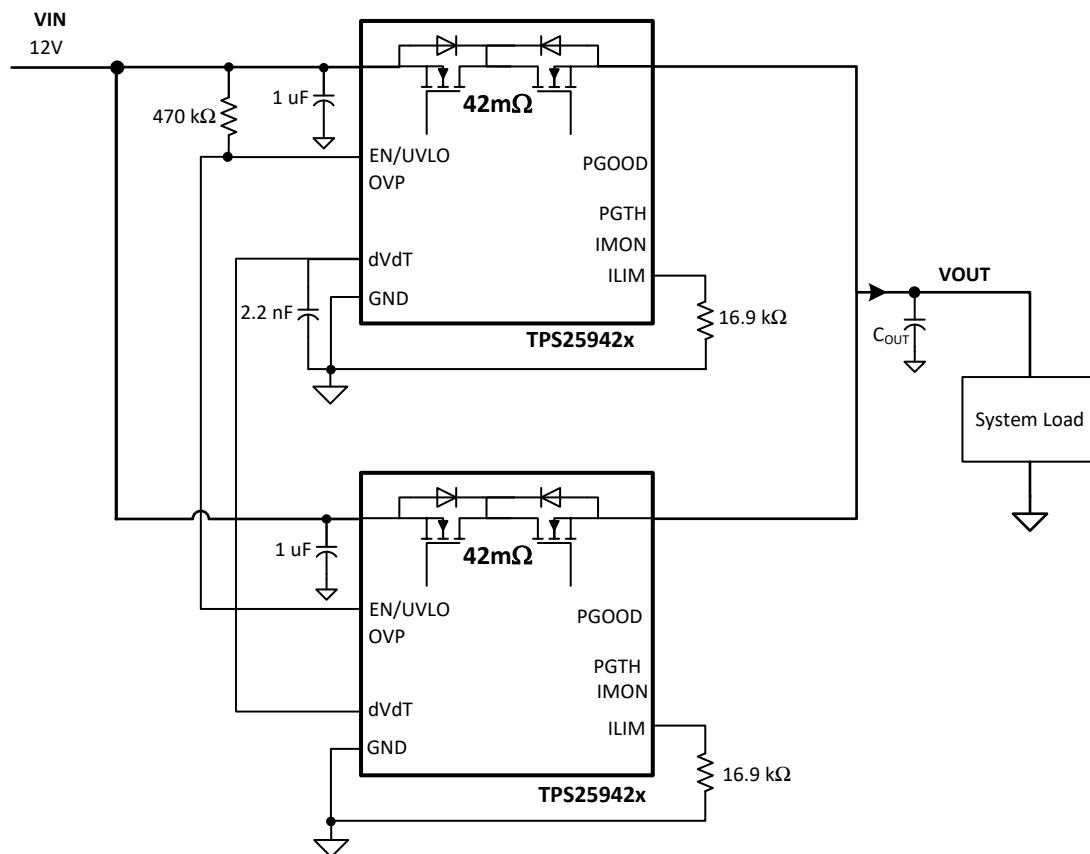




Circuit Configuration for Parallel Operation of two eFuses