CoolGaN™ Integrated Power Stage IGI60F0014A1L

140 mΩ / 600 V GaN power switch with robust, fast and accurate isolated gate driver

Features

- 600 V GaN switch (140 mΩ typ. / 190 mΩ max. R_{dson}) with dedicated functional isolated gate driver
  - source / sink peak driving current 1 A / 2 A
  - gate resistors for flexible turn-on / -off speed (EMI reduction)
  - coupling capacitor C_C enables programmable negative gate drive voltage for safe “off” state
  - gate resistor R_{SS} for programmable on-state gate current (typ. 5 mA)
- Standard logic input levels compatible with digital controllers
- Wide range for both input and output driver supply voltage
- Fast input-to-output propagation (47 ns typ.) with low variation
- Galvanic input-to-output isolation based on robust coreless transformer technology
- Gate driver with very high common mode transient immunity (CMTI) > 150 V/ns
- 1200 V input-to-output isolation
- Thermally enhanced 8 x 8 mm QFN-21 package with large exposed pad

Description

IGI60F0014A1L combines a single channel 140 mΩ (typ.) / 600 V enhancement-mode CoolGaN™ switch with a dedicated gate driver in a thermally enhanced 8 x 8 mm QFN-21 package. Due to the galvanic functional isolation between input and output the power stage is able to cover a broad spectrum of applications and topologies.
Infineon’s CoolGaN™ and related power switches provide a very robust gate structure that requires a small continuous gate current of a few mA in the steady “on”-state. However, this guarantees optimized driving under any operating conditions and always results in a minimized R_{dson}, regardless of temperature and process parameter variations or switch current level. Because of the GaN-specific low threshold voltage and extremely fast switching, a negative gate drive voltage is required during hard-switching transients to avoid spurious turn-on effects. The external passive SMD components (RRC) in the gate loop fulfil this task without the need for a permanent negative supply voltage and besides enable easy adaptation to different applications (low/medium power, hard/soft switching).

The driver utilizes on-chip coreless transformer EiceDriver™ technology (CT) to achieve isolation and level-shifting of the PWM signal to the high side. CT achieves excellent robustness with fast switching transients up to 150 V/ns.

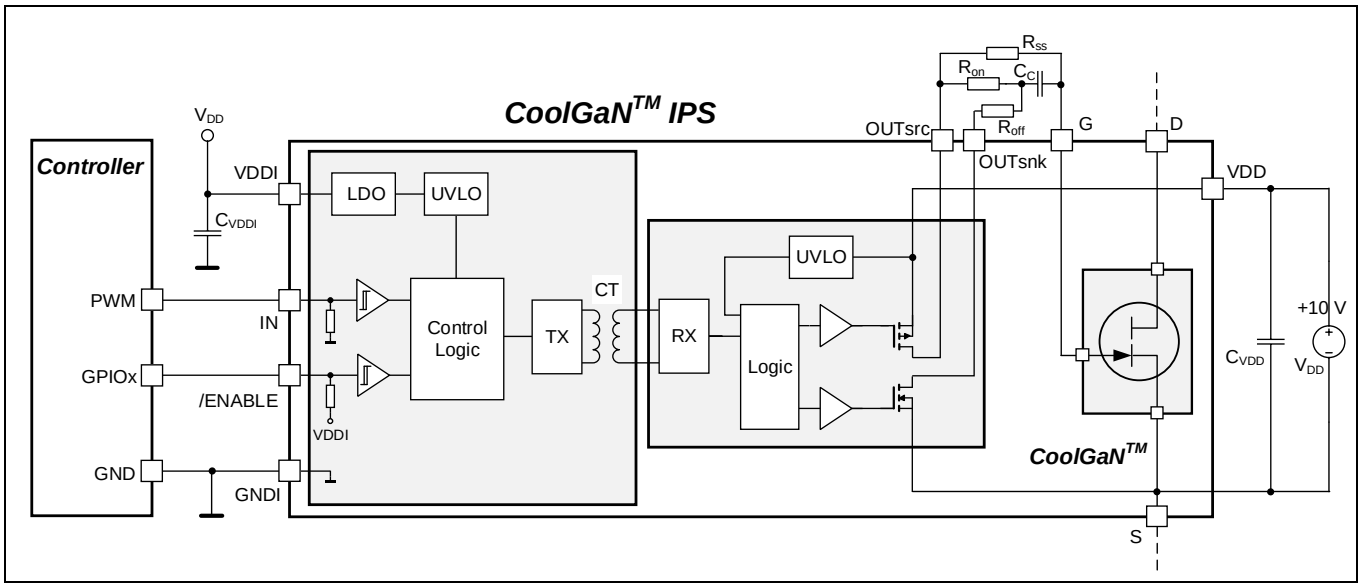

Figure 1 Typical Application

Potential Application Segments

- Consumer and server SMPS power supplies
- Uninterruptable power supplies
- Power adapters and fast chargers

Potential Power Topologies

- Digital controller based AC/DC, DC/DC and DC/AC topologies
- LLC or LCC resonant converters
- Single or interleaved synchronous buck or boost converter
- Low-to-medium power bridgeless boost PFC
- Single-phase or interleaved Totem Pole PFC
- High-frequency bidirectional dual active bridge

Product Versions

Table 1 CoolGaN™ power stage product overview

Part Number	OPN	Package	$R_{dson,typ.}$ / $R_{dson,max.}$ @ 25 °C	Isolation class	Working voltage
IGI60F0014A1L		QFN-21 8 x 8 mm	140 mΩ / 190 mΩ	functional	600 V

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1 Pin configuration and description

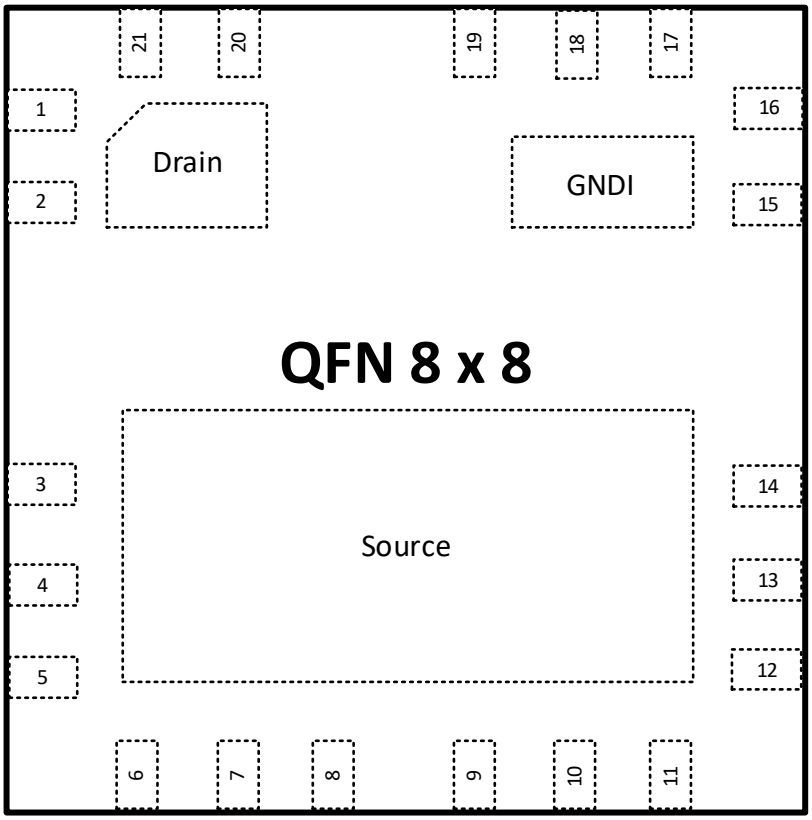


Figure 2 Pin configuration and exposed for QFN-21 8 x 8 mm package, top view (not to scale)

Table 2 Pin description

Pin No.	Symbol	Description
1, 2, 20, 21	D	Drain connection GaN switch
3 – 8, 14	S	Source connection GaN switch
9	SK	Kelvin source connection GaN switch
10	G	Gate connection GaN switch
11	OUTSNK	Driver output sink (connects to S)
12	OUTSRC	Driver output source (connects to VDD)
13	VDD	Driver supply voltage (typ. 8 V)
15, 19	GNDI	Ground connection of driver input stage
16	VDDI	Supply voltage driver input stage
17	IN	Input signal (default state Low); controls GaN switch
18	/ENABLE	Input signal (default state High – driver output set to Low state); logic Low required to activate driver output

2 Functional description

2.1 Block Diagram

A simplified functional block diagram of the GaN Power Stage is given in Fig. 5. For level-shifting of the input signal to a high-side switch an on-chip coreless transformer (CT) is utilized, resulting in a galvanic input-to-output isolation.

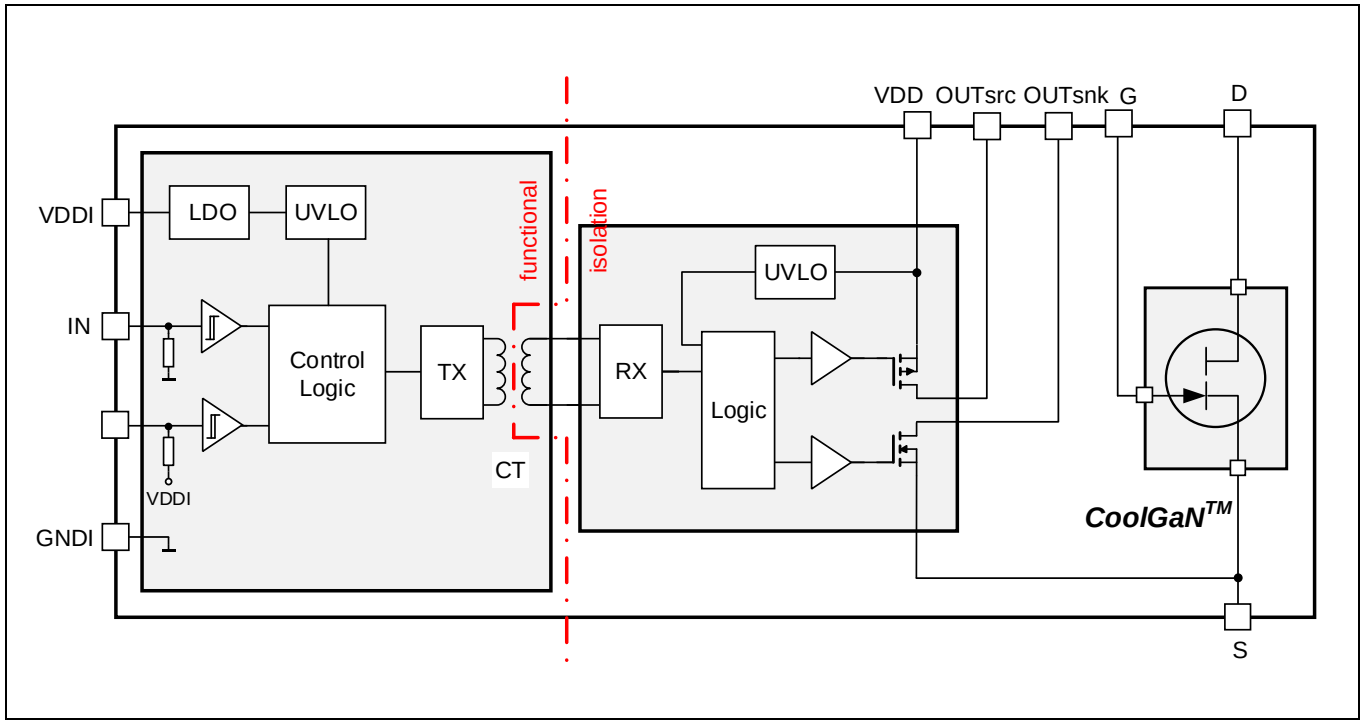


Figure 3 Block Diagram IGI60F0014A1L

2.2 Power supply

Basically the Power Stage requires two supply voltages: a µController ground-related V_{DDI} (3 to 15 V) for the driver input circuitry and a source-related V_{DD} (8 to 12 V) as the gate drive supply. In low-side applications usually a single 8 V supply voltage can be used for both V_{DDI} and V_{DD}. Operation as a high-side switch, however, requires a floating gate driver supply. In applications with moderate duty cycle variations (e. g. LLC), this high-side supply voltage can be generated from the ground-related one via bootstrapping.

Independent Undervoltage Lockout (UVLO) functions for both supply voltages ensure a defined start-up and robust functionality under all operating conditions.

2.2.1 Driver input supply voltage

The driver input die is supplied via V_{DDI}. Any applied voltage up to 15 V is regulated by an internal LDO to 3.3V. A ceramic bypass capacitance C_{VDDI} of typ. 100 nF has to be placed close to pin VDDI. The Undervoltage Lockout threshold, defining the minimum V_{DDI}, is set to typically 2.85 V.

Power consumption to some extent depends on switching frequency, as the input signal is converted into a train of repetitive current pulses to drive the CT. Due to the chosen robust encoding scheme the average pulse repetition rate and thus the average supply current depends on the switching frequency f_{sw}. However, for f_{sw} < 500 kHz this effect is very small.

2.2.2 Driver output supply voltage

The output stage has to be supplied by a voltage V_{DD} of typically 8 V related to the source of the GaN switch. In low-side applications V_{DD} can be ground-related. A ceramic bypass capacitance C_{VDD} of typ. 100 nF has to be placed close to pin VDD. The minimum operating supply voltage is defined by the implemented undervoltage lockout function (see chapter 2.4).

2.3 Driver output

The rail-to-rail driver output stage realized with complementary MOS transistors is able to provide a typical 1 A sourcing and 2 A sinking current. This is by far sufficient when driving a GaN HEMT due to the low gate charge of only 3 nC. In addition, the relatively low driver output resistance is beneficial, too. With an R_{on} of 3.1 Ω for the sourcig pMOS and 1.2 Ω for the sinking nMOS transistor the driver can be considered as nearly ideal. The gate drive parameters can thus be determined easily and accurately by the external components as described in chapter 4. The p-channel sourcing transistor allows real rail-to-rail behavior without suffering from a source follower's voltage drop.

2.4 Undervoltage Lockout (UVLO)

The Undervoltage Lockout function ensures that the gate drive outputs can be switched to their high level only, if both input and output supply voltages exceed the corresponding UVLO threshold voltages. Thus it can be guaranteed that the GaN switches are in “off” state, if the driving voltage is too low for complete and fast switching-on, thereby avoiding excessive power dissipation and keeping the switch transistors within their safe operating area (SOA).

The UVLO level for the output supply voltage V_{DD} is set to a typical “on”-value of 4.2 V (with 0.3 V hysteresis), whereas $UVLO_{in}$ for V_{DDI} is set to 2.85 V with 0.15 V hysteresis.

2.5 Start-up and active clamping

Special attention has been paid to cover all possible operating conditions, like start-up or arbitrary supply voltage situations:

- if V_{DDI} drops below $UVLO_{in}$, a “switch-to-low” command is sent to the gate driver output
- for V_{DD} lower than the respective output UVLO level, a new fast active clamping circuit provides a low-impedance path from the gate driver output to the source of the GaN switch. As soon as the output voltage exceeds a low threshold level (typ. below 1 V), the clamp is activated within approximately 20 ns.

As the result, safe operation of the GaN Power Stage can be guaranteed under any circumstances.

2.6 CT Communication and Data Transmission

A Coreless Transformer (CT) based communication module is used for PWM signal transfer between input and output. A proven high-resolution pulse repetition scheme in the transmitter combined with a watchdog time-out at the receiver side enables recovery from communication fails and ensures safe system shut-down in failure cases.

2.7 CoolGaN output stage

The 600 V CoolGaN™ switch of type IGx60R190 is characterized by a typical R_{dson} of 140 mΩ @ 25 °C. And thanks to the current driving concept, this value increases by a comparably moderate 85 % @ 150 °C. As typical for GaN, gate and output charges are very small (3 and 16 nC, resp.) and there is no reverse recovery charge due to the lack of a physical body diode.

3 Characteristics

3.1 Absolute maximum ratings

The absolute maximum ratings are listed in Table 3. Stresses beyond these values may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note or Test Conditions
		Min.	Max.		
Drain-to-source voltage continuous	V_{DS}		600	V	V_{GS} = 0 V
Drain-to-source voltage pulsed	$V_{DS,pulse}$		750	V	T_J = 25°C, V_{GS} <= 0 V, cumulated stress time < 1h
			650	V	T_J = 125°C, V_{GS} <= 0 V, cumulated stress time < 1h
Continuous drain current	I_D		12.5	A	T_{Case} = 25°C
			5.5	A	T_{Case} = 125°C (see Fig. 8)
Pulsed drain current	$I_{D,pulse}$		23	A	T_{Case} = 25°C
			13	A	T_{Case} = 125°C (see Fig. 8)
Supply voltage input chip	V_{DDI}	-0.3	17	V	
Supply voltage output chips	V_{DD}	-0.3	22	V	
Voltage at pins IN and ENABLE	V_{IN}	-0.3	17	V	
Voltage at pin OUT	V_{OUT}	-0.3	V_{DD} + 0.3	V	
Junction temperature	T_J	- 40	150	°C	
Storage temperature	T_S	-65	150	°C	
Soldering temperature		-	260	°C	reflow/wave soldering[1]
ESD capability	V_{ESD_HBM}	-	2	kV	Human Body Model[2]
	V_{ESD_CDM}	-	0.5	kV	Charged Device Model[3]

[1]acc. to JESD22A111

[2]acc. to EIA/JESD22-A114-B (discharging 100 pF capacitor through 1.5 kΩ resistor)

[3]acc. to JESD22-oo2

3.2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Thermal resistance junction-case	R_{thJC}		t.b.d.		K/W	

3.3 Operating range

Table 5 Operating range

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input supply voltage	V_{DDI}	3		15	V	
Driver output supply voltage	V_{DD}	5.5	8	20[1]	V	min. defined by $UVLO_{out}$
Logic input voltage at pins IN and /ENABLE	V_{IN}	-0.3		15	V	
Ambient temperature	T_A	-40		125	°C	
Junction temperature	T_J	-40		150[2]	°C	

[1] VDD < 12 V recommended

[2] continuous operation above 125 °C may reduce lifetime

3.4 Electrical characteristics

Unless otherwise noted, min/max values of characteristics are the lower and upper limits, resp. They are valid within the full operating range. Typical values are given at T_J = 25 °C with V_{DDI} = V_{DD} = 8 V.

Table 6 Power supply

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
V_{DDI} quiescent current	I_{VDDIqu}		1.4		mA	no switching
V_{DD} quiescent current	I_{VDDqu}		0.7		mA	no switching
Undervoltage Lockout input ($UVLO_{in}$) turn-on threshold	$UVLO_{in}$	2.75	2.85	2.95	V	
$UVLO_{in}$ turn-off threshold	$UVLO_{in-}$	-	2.7	-	V	
$UVLO_{in}$ threshold hysteresis	$\Delta UVLO_{in}$	0.1	0.15	0.2	V	
Undervoltage Lockout outputs ($UVLO_{out}$) turn-on threshold	$UVLO_{out}$	4.0	4.2	4.4	V V	
$UVLO_{out}$ turn-off threshold	$UVLO_{out-}$	-	3.9	-	V	
$UVLO_{out}$ threshold hysteresis	$\Delta UVLO_{out}$	0.2	0.3	0.4	V	

Table 7 Logic inputs IN and /ENABLE

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input voltage threshold for transition LH	V_{INH}	1.7	2.0	2.3	V	independent of V_{DDI}
Input voltage threshold for transition HL	V_{INL}	-	1.2	-	V	independent of V_{DDI}
Input voltage threshold hysteresis	V_{IN_hys}	0.4	0.8	1.2	V	
Input pull down resistor (IN)	R_{IN}		75		kΩ	
Input pull up resistor (/ENABLE)	R_{ENA}		75		kΩ	

Table 8 Static gate driver output characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
High-level (sourcing) output resistance	R_{on}	1.4	3.1		Ω	T_J = 25 °C
				5.8	Ω	T_J = 150 °C
Peak sourcing output current	$I_{src,pk}$		1		A	actively limited to 1.3 A
Low-level (sinking) output resistance	R_{off}	0.6	1.2		Ω	T_J = 25 °C
				2.5	Ω	T_J = 150 °C
Peak sinking output current	$I_{snk,pk}$		-2		A	actively limited to -2.6 A
Active clamp threshold voltage	V_{clmp}		1		V	

Table 9 Output characteristics GaN switch

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Drain-source on-resistance	R_{dson}		140	190	mΩ	T_J = 25 °C
			260		mΩ	T_J = 150 °C
Drain-source leakage current	I_{leak}		0.4		µA	V_{DS} = 600 V, T_J = 25 °C
			8		µA	V_{DS} = 600 V, T_J = 150 °C
Gate charge	Q_g		3.2		nC	I_G = 0 to 3.8 mA, V_D = 400 V, I_D = 5 A
Output charge	Q_{oss}		16		nC	
Reverse recovery charge	Q_{rr}		0		nC	

Table 10 Dynamic Characteristics[1] (see Fig. 4, 5)

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input (IN, /ENABLE) to switching node D propagation delay “on”	t_{PDon}		47		ns	R_{tr} = 50 Ω
Input (IN, /ENABLE) to switching node D propagation delay “off”	t_{PDoff}		47		ns	I_{load} = 2 A
Rise time at node D	t_{rise}		6		ns	10 % to 90 %
Fall time at node D	t_{fall}		5		ns	90 % to 10 %
Minimum input pulse width that changes output state	t_{PW}		18		ns	

Table 11 Functional isolation input-to-output

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Input-to-output isolation voltage	V_{ISO}	1200	-	-	V_{DC}	production test > 10 ms
Package clearance	CLR	-	1.9	-	mm	shortest distance over air, from any input pin to any output pin
Package creepage	CPG	-	1.9	-	mm	shortest distance over surface, from any input pin to any output pin
Common Mode Transient Immunity	CMTI	150	-	-	V/ns	acc. to DIN V VDE V0884-10, static and dynamic test

Table 12 Package characteristics

Parameter	Symbol	Values			Unit	Note or Test Conditions
		Min.	Typ.	Max.		
Comparative Tracking Index of package mold	CTI	400	-	600	V	according to DIN EN 60112 (VDE 0303-11)
Material group	-	-	2	-	-	according to IEC 60112

[1] Verified by design / characterization, not tested in production

3.5 Timing diagram and test circuit

Figure 4 depicts rise, fall and delay times measured at the drain node of the GaN switch.

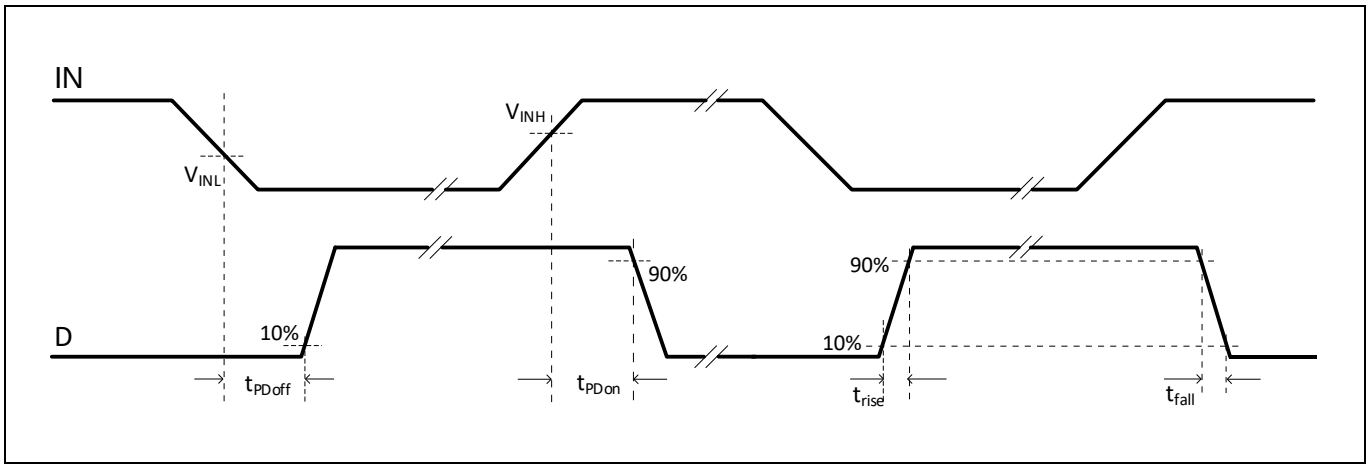


Figure 4 Propagation delay, rise and fall time

Figure 5 shows the associated test circuit. The power stage is operated in a boost configuration at a constant current I_{load}. In this so-called double-pulse arrangement I_{load} is determined by the high-voltage supply (400 V), the output inductance and the length of the first “on”-phase of the IN-signal. The specified delay and transient times are related to an I_{load} value of 2 A (particularly the “off” transient strongly depends on this current).

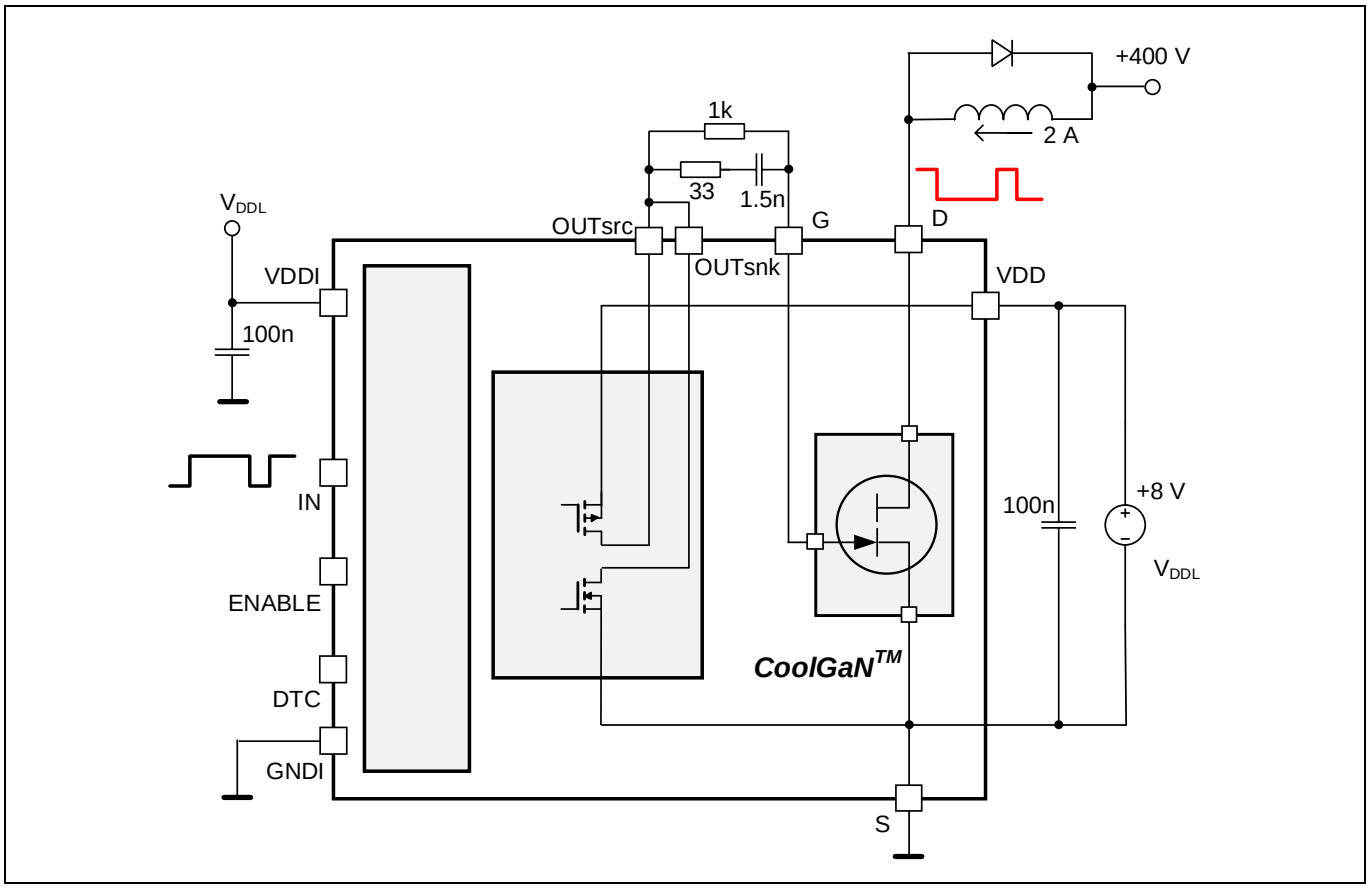


Figure 5 Test circuit

4 Driving CoolGaN™ HEMTs

Although gallium nitride high electron mobility transistors (GaN HEMTs) with ohmic connection to a pGaN gate are robust enhancement-mode (“normally-on”) devices, they differ significantly from MOSFETs. The gate module is not isolated from the channel, but behaves like a diode with a forward voltage V_F of 3 to 4 V. Equivalent circuit and typical gate input characteristic are given in Fig. 6. In the steady “on” state a continuous gate current is required to achieve stable operating conditions. The switch is “normally-off”, but the threshold voltage V_{th} is rather low (~ +1 V). This is why in many applications a negative gate voltage -V_N, typically in the range of several Volts, is required to safely keep the switch “off” (Fig. 3b).

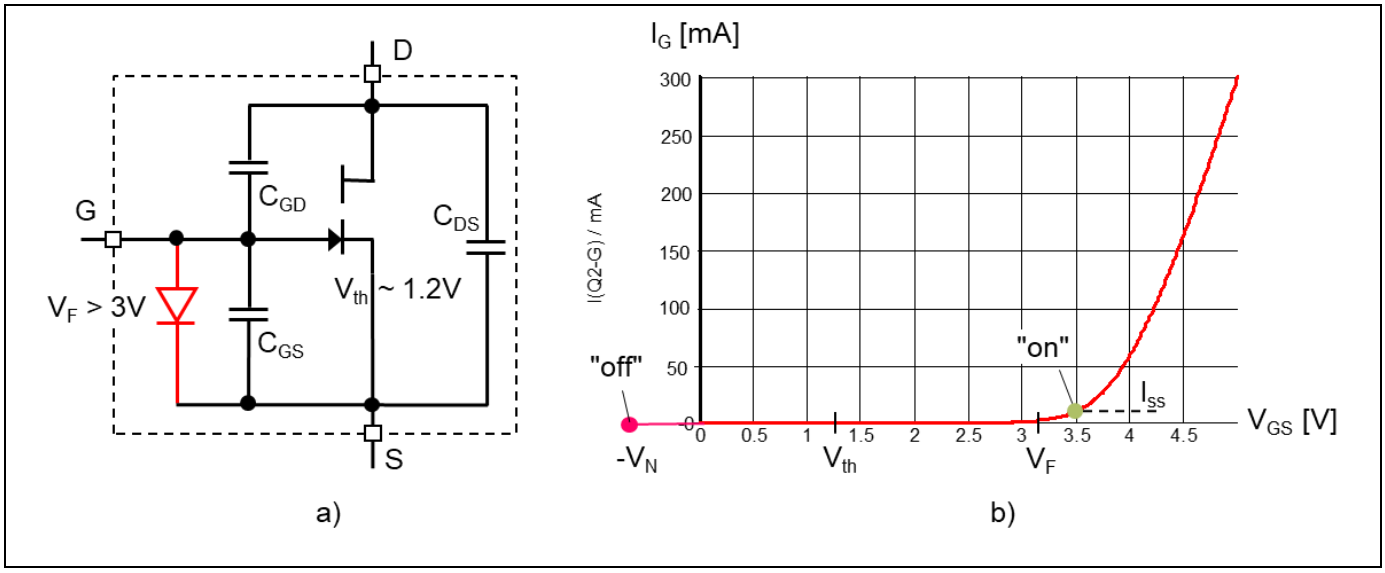


Figure 6 Equivalent circuit (a) and gate input characteristics (b) of typical normally-off GaN HEMT

Obviously the transistor in Fig. 6 cannot be driven like a conventional MOSFET due to the need for a steady-state “on” current I_{ss} and a negative “off” voltage –V_N. While an I_{ss} of a few mA is sufficient, fast switching transients require gate charging currents I_{on} and I_{off} in the 1 A range. To avoid a dedicated driver with 2 separate “on” paths and bipolar supply voltage, the solution depicted in Fig. 7 is usually chosen, combining a standard gate driver with a passive RC circuit to achieve the intended behavior. The high-current paths containing the small gate resistors R_{on} and R_{off}, respectively, are connected to the gate via a coupling capacitance C_C. C_C is chosen to have no significant effect on the dynamic gate currents I_{on} and I_{off}. In parallel to the high-current charging path the much larger resistor R_{ss} forms a direct gate connection to continuously deliver the small steady-state gate current I_{ss}. In addition, C_C can be used to generate a negative gate voltage. Obviously, in the “on” state C_C is charged to the difference of driver supply V_{DD} and diode voltage V_F. When switching off, this charge is redistributed between C_C and C_{GS} and causes an initial negative V_{GS} of value

$$-V_N = -\frac{C_C \cdot (V_{DD} - V_F) - Q_{Geq}}{C_C + C_{GS}}$$

with Q_{Geq} denoting an equivalent switching gate charge (Q_{Geq} = Q_{GS} ~ 0.5 nC for a hard-switching and Q_{Geq} ~ Q_{GS} + Q_{GD} = 3 nC for a soft-switching system). V_N can thus be controlled by proper choice of V_{DD} and C_C. During the „off“ state the negative V_{GS} decreases, as C_C is discharged via R_{SS}. The associated time constant cannot be chosen independently, but is related to the steady-state current and is typically in the 1 µs range. The negative gate voltage at the end of the “off” phase (V_{Nf} in Fig. 7b) thus depends on the “off” duration. It lowers the effective driver voltage for the following switching-on event, resulting in a slight dependence of switching dynamics on frequency and duty cycle. However, in most applications the impact of this effect is negligible.

Another situation requires attention, too. If there is by any reason a longer period with both switches of a half-bridge in “off”-state (e.g. during system start-up, burst mode operation etc.), both capacitors C_C will be discharged. That means, for the first switching pulse after such an extended non-switching period no negative voltage is available. To avoid instabilities due to spurious turn-on effects in such a situation, C_C should not be chosen lower than 1.5 nF.

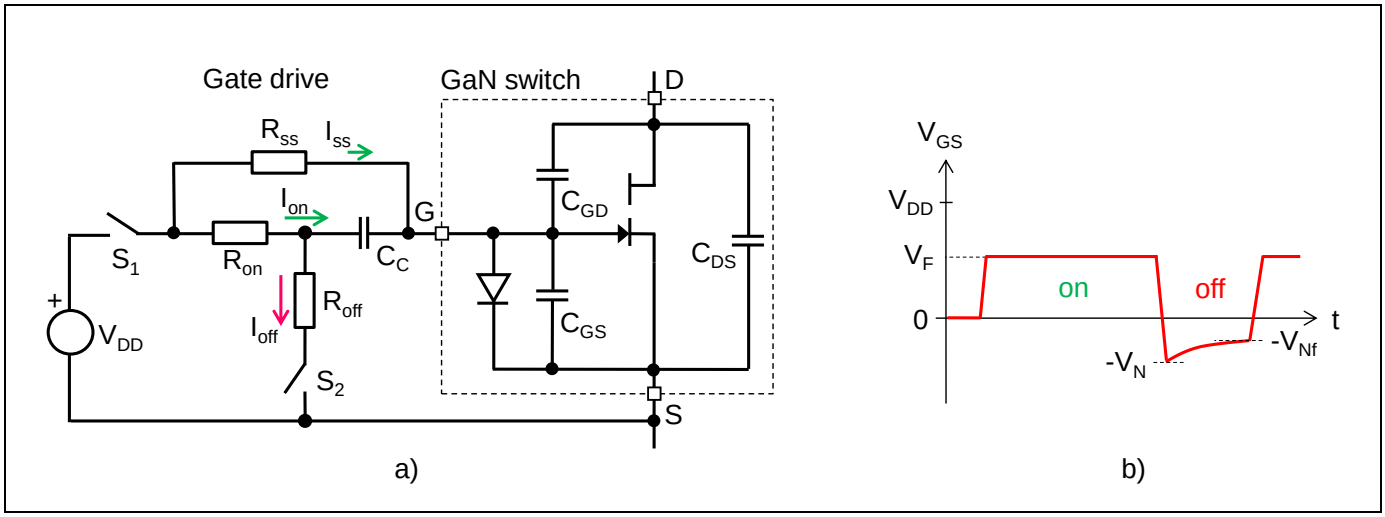


Figure 7 Equivalent circuit of GaN switch with RC gate drive (a) and gate-to-source voltage V_{GS} (b)

In the topology of Fig. 7 a single resistor R_{tr} is responsible for setting the maximum transient charging and discharging current. This is often acceptable. If it is not, an additional resistor R_{off} with series diode in parallel with R_{tr} can be used to realize different impedances for “on” and “off” transients, respectively.
All relevant driving parameters are thus easily programmable by choosing V_{DD}, R_{ss}, R_{tr}, R_{off} and C_C according to the relations

$$-V_N = -\frac{C_C \cdot (V_{DD} - V_F) - Q_{Geq}}{C_C + C_{GS}} \qquad (1)$$

$$I_{ss} = \frac{V_{DD} - V_F}{R_{ss}}, \qquad I_{on,max} = \frac{V_{DD} \cdot (R_{off} + R_{tr})}{R_{off} \cdot R_{tr}}, \qquad I_{off,max} = \frac{V_{th} + V_N}{R_{off}}$$

Typical recommended values are

V_{DD} = 8 V

C_C = 1.5 nF

R_{ss} = 1 kΩ

R_{tr} = 20 … 50 Ω

R_{off} = 4.7 Ω

5 Typical characteristics

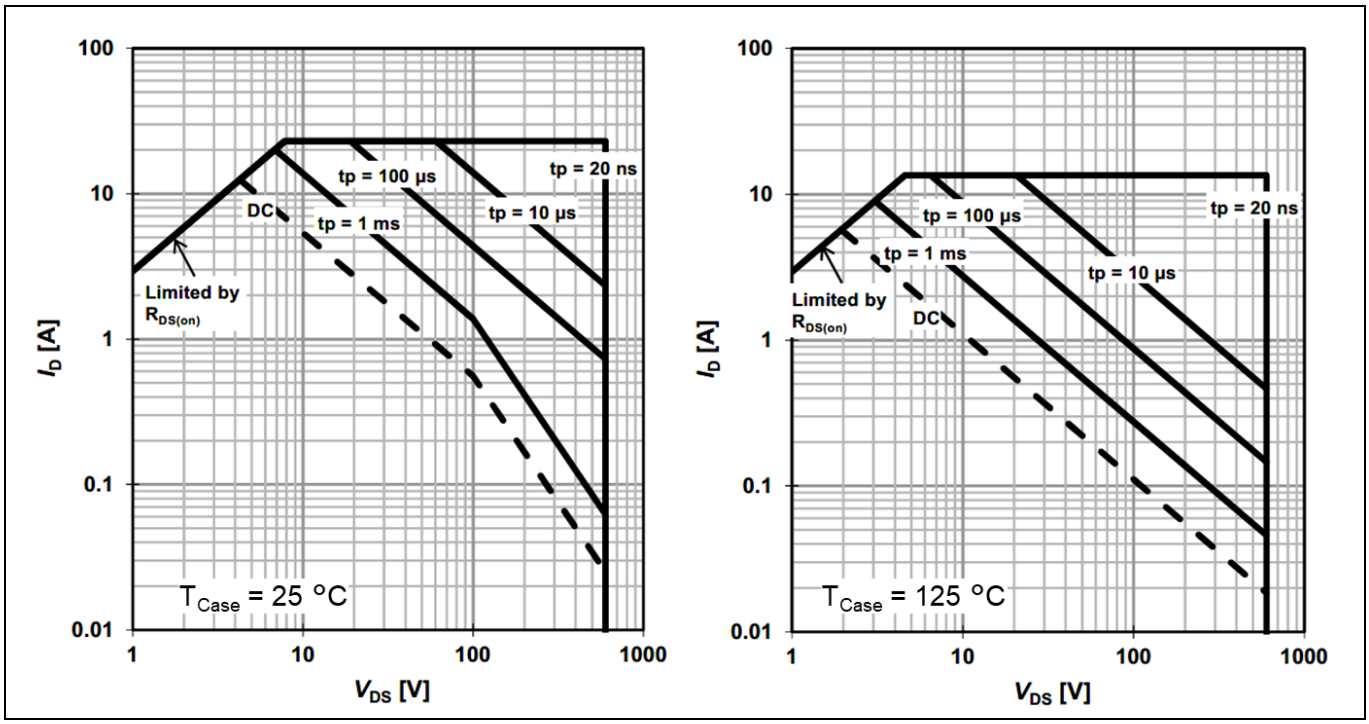


Figure 8 Safe Operating Area (SOA)

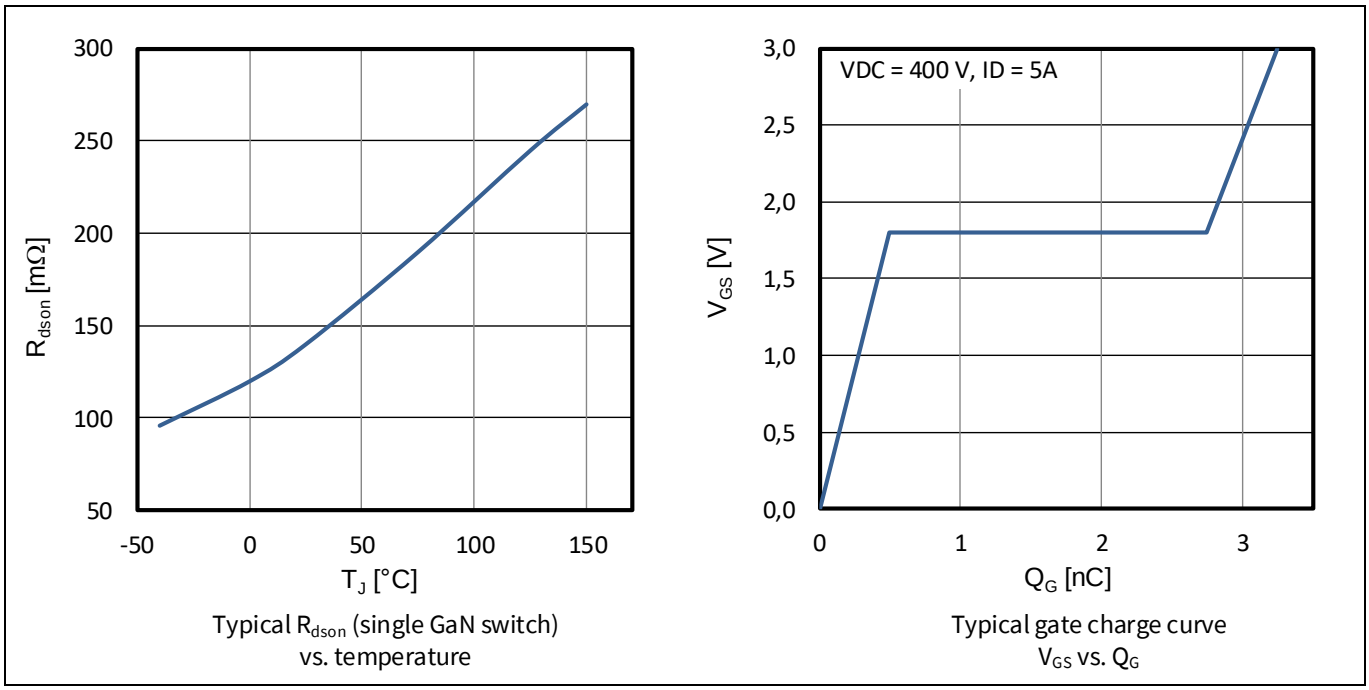


Figure 9 R_{dson} (T) and gate charge curve V_{gs} (Q_G)

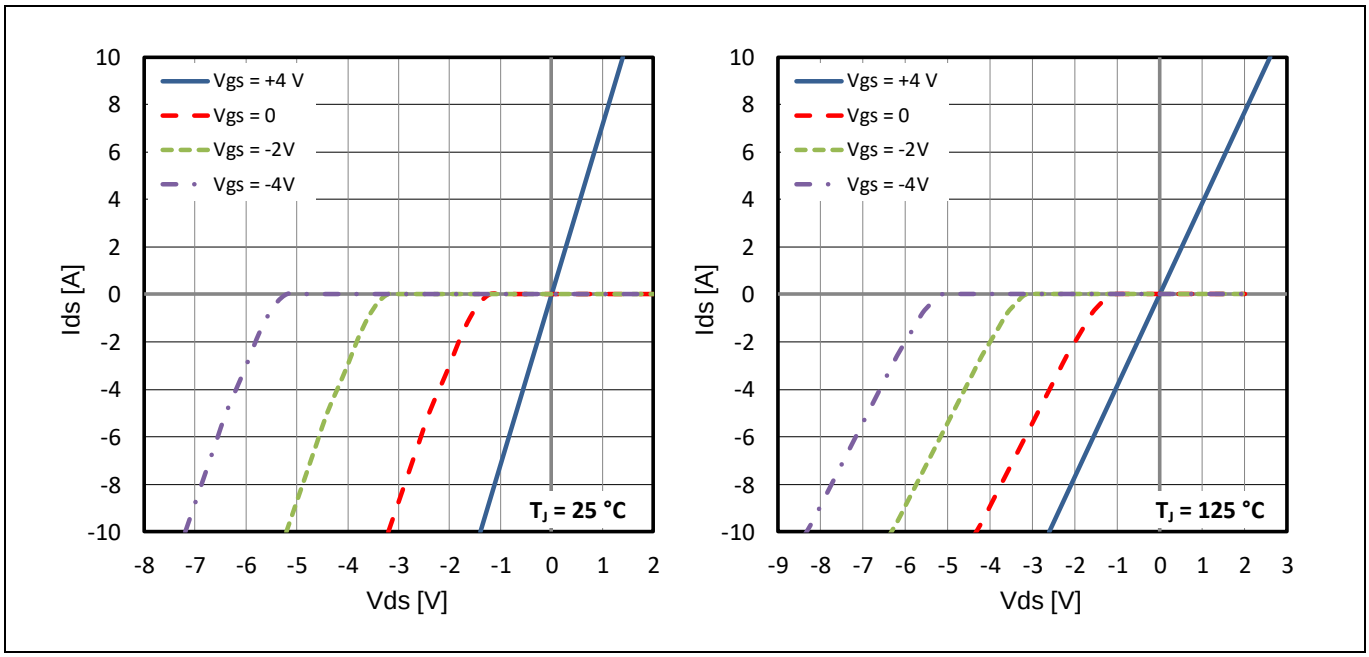


Figure 10 Output characteristic I_{ds} (V_{ds}) in normal and reverse operation (parameter V_{gs})

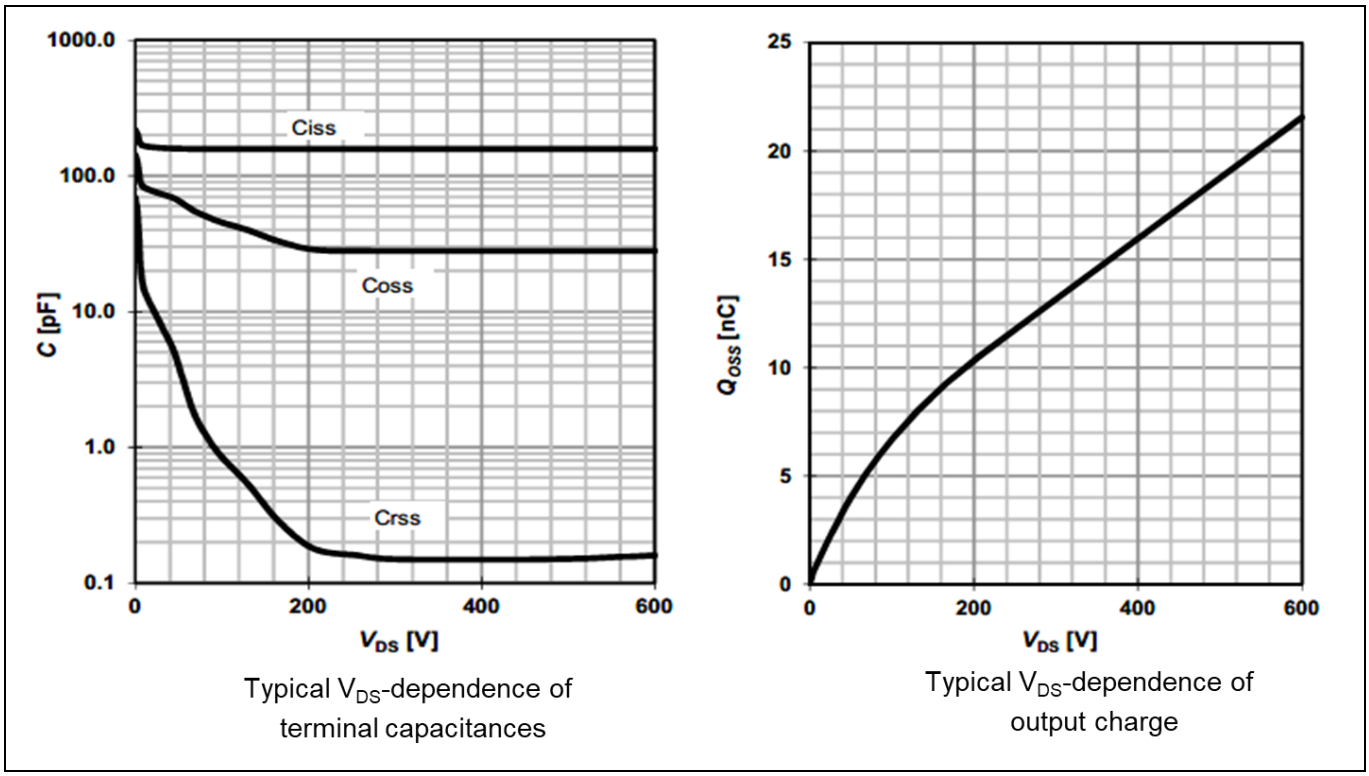
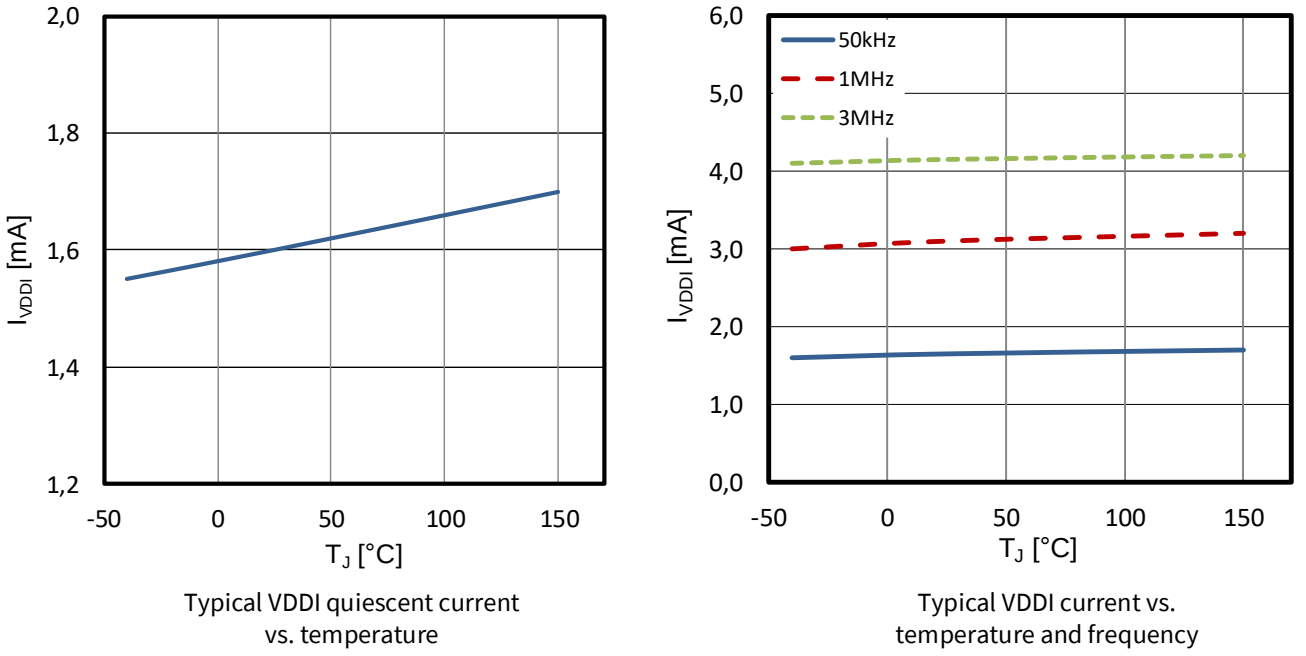


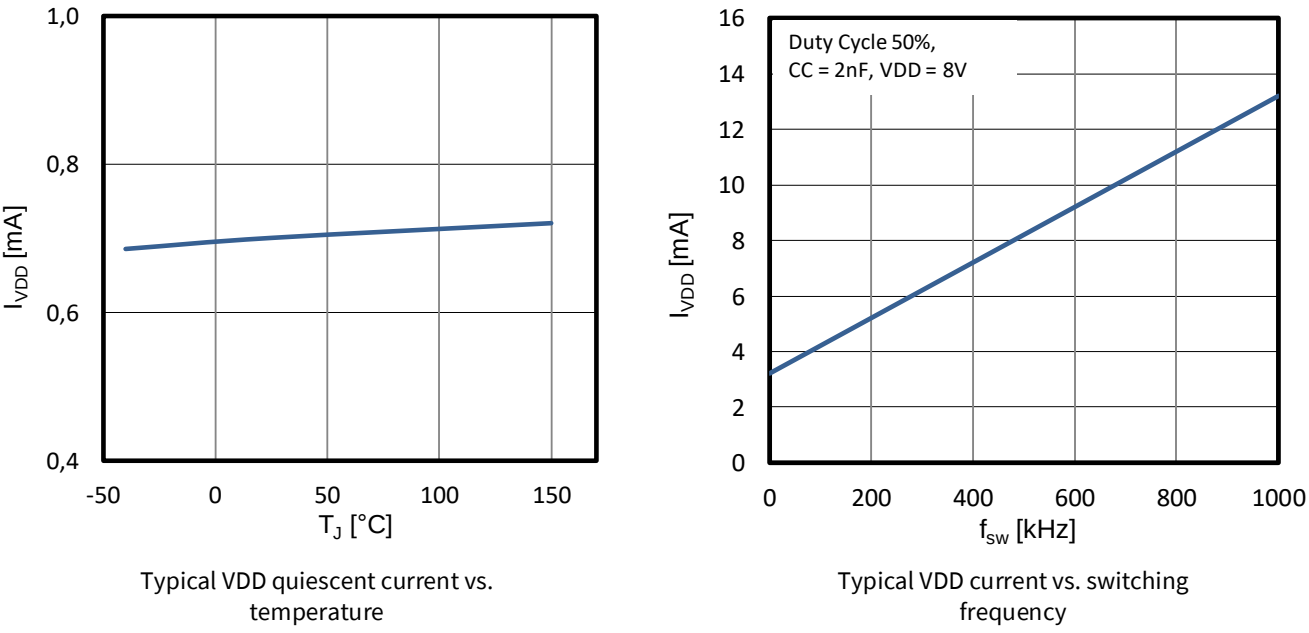
Figure 11 Switch capacitances and output charge



Typical VDDI quiescent current vs. temperature

Typical VDDI current vs. temperature and frequency

Figure 12 Supply current V_{DDI}



Typical VDD quiescent current vs. temperature

Typical VDD current vs. switching frequency

Figure 13 Supply current V_{DD}

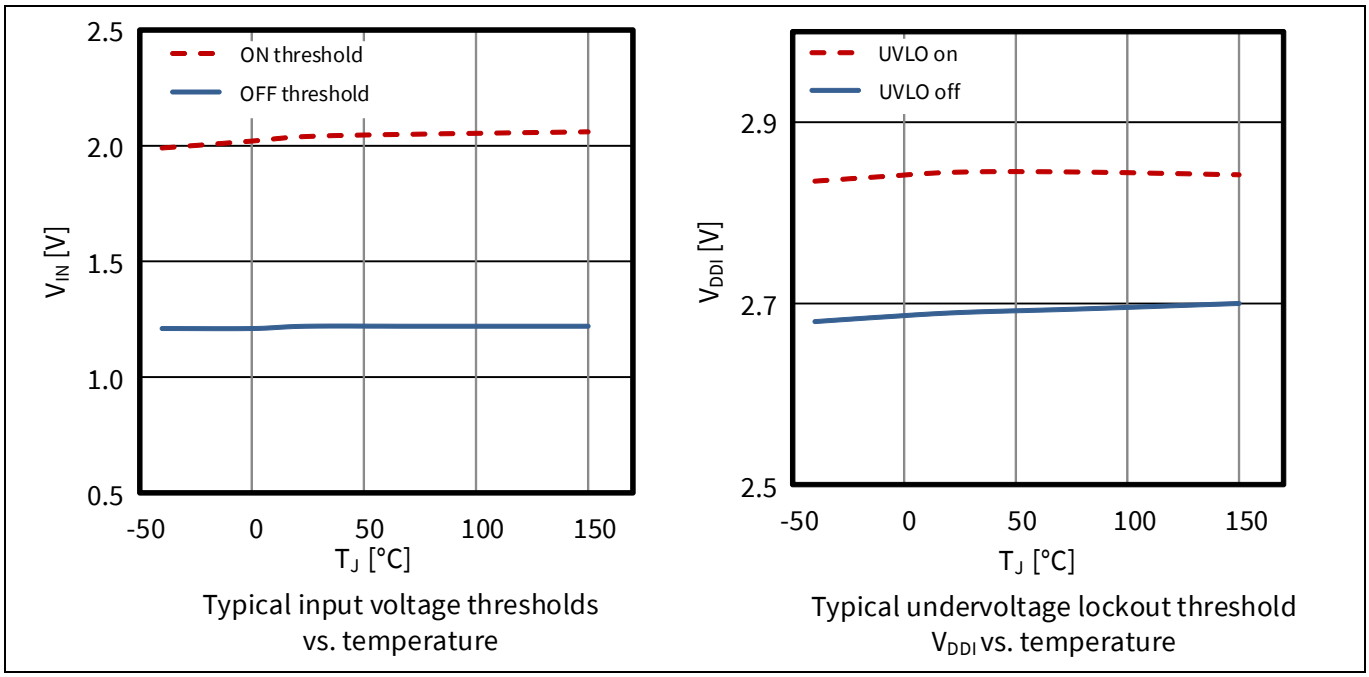


Figure 14 Logic input thresholds and V_{DDI} UVLO

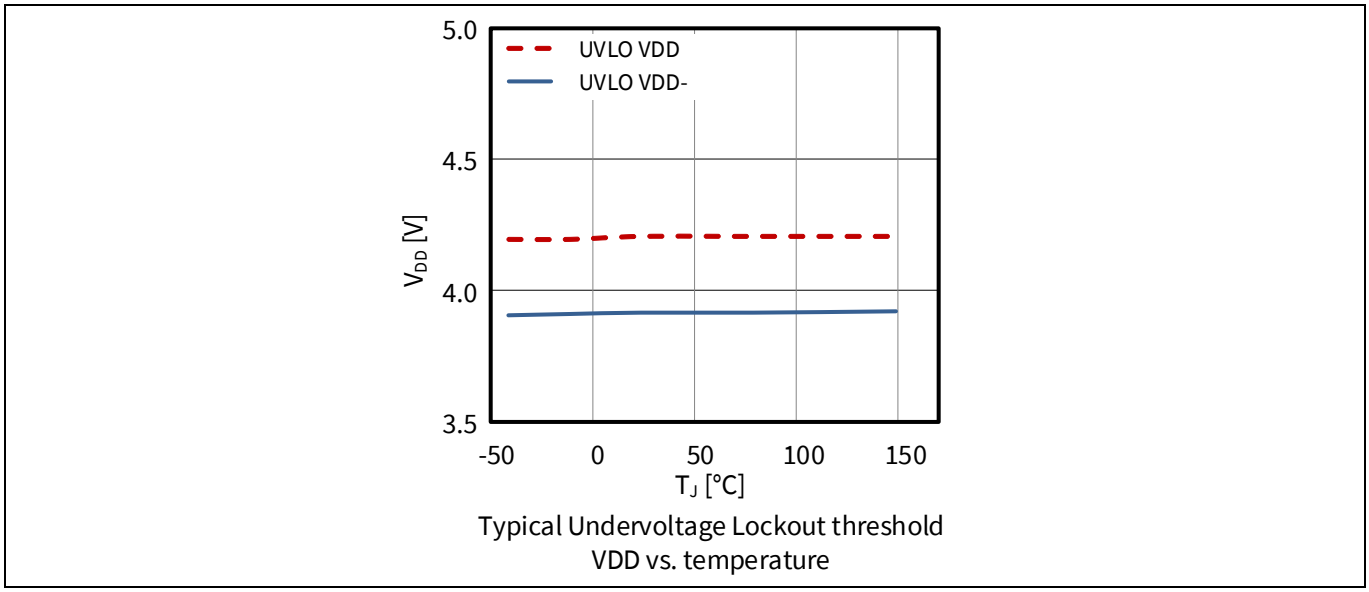
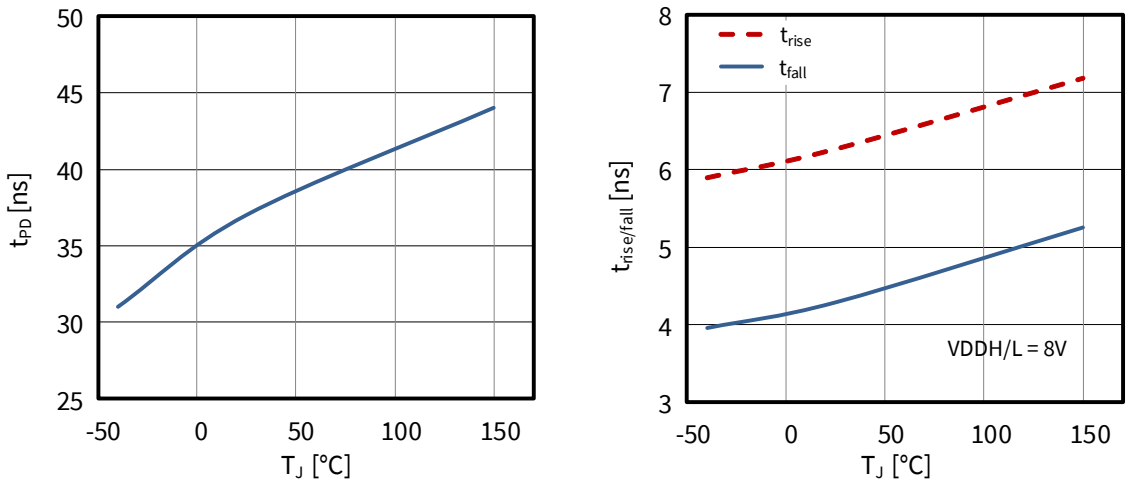


Figure 15 V_{DD} UVLO



Typical propagation delays vs. temperature

Typical rise and fall time vs. temperature

Figure 16 Propagation delay and rise / fall times

6 Application circuit

Fig. 14 shows a typical application of IGI60F0014A1L as the primary side switches in an LLC converter. Two integrated power stages are operated from a single 8 V supply, with the high-side supply generated by bootstrapping (diode D_{boot}, capacitance C_{boot} and resistor R_{boot}).

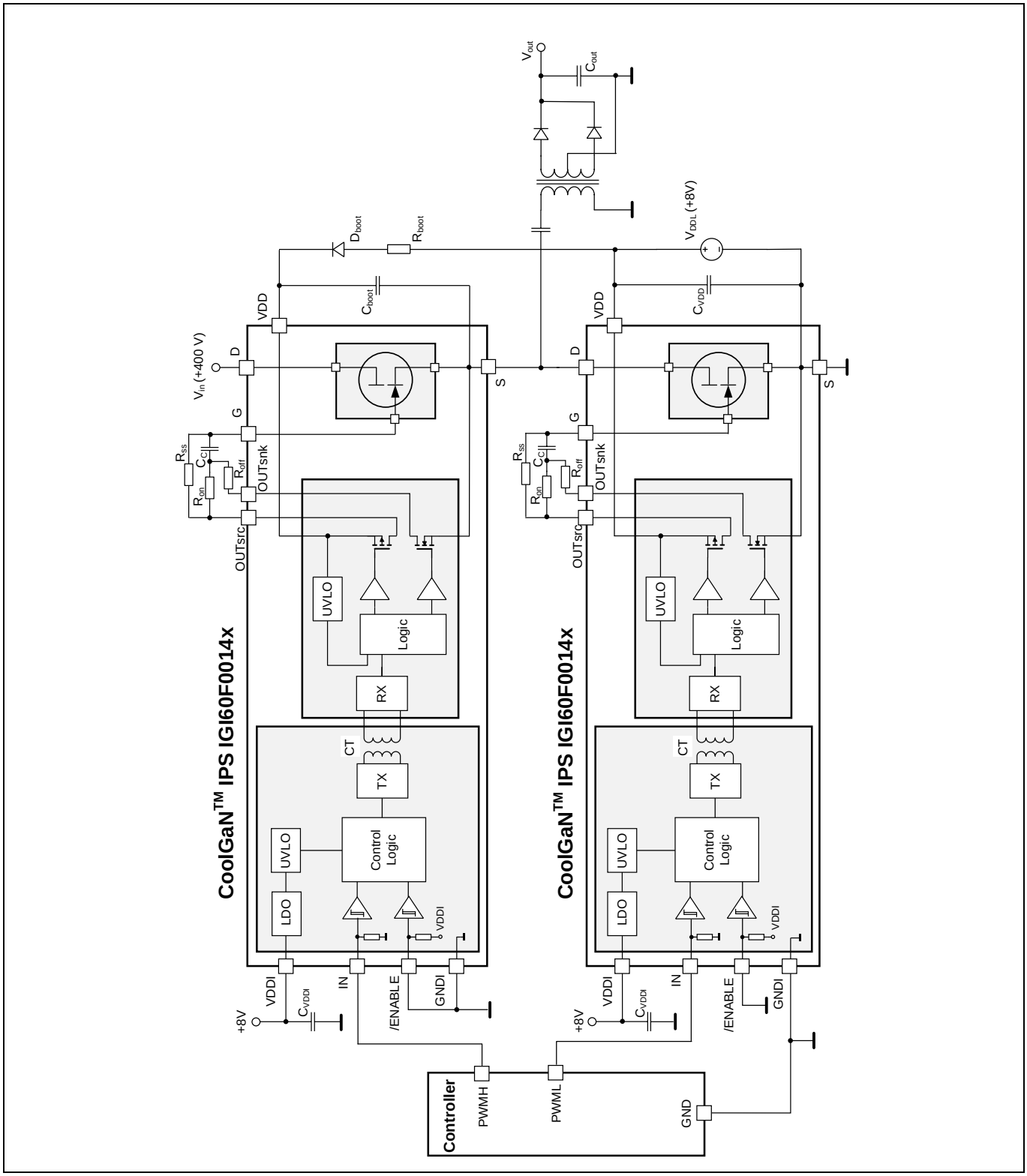


Figure 17 Application of IGI65F0014 in LLC primary stage

7 Layout guidelines

Note: Space intentionally left blank in preliminary Datasheet, ask our Application Engineers for guidance.

8 Package information

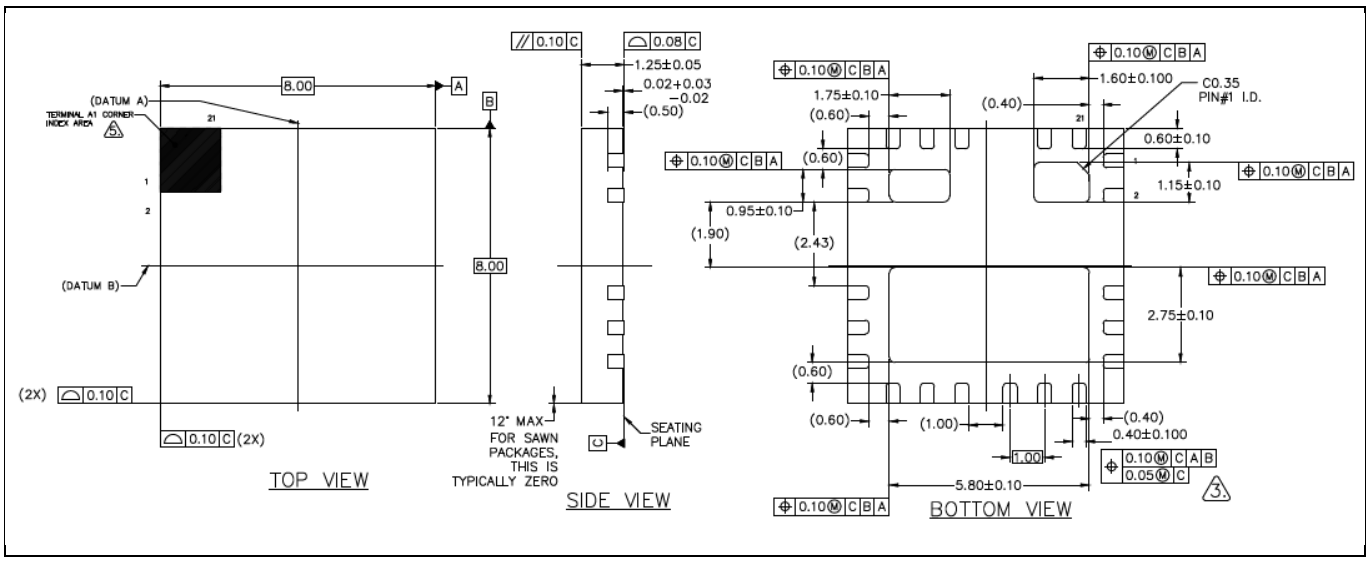


Figure 18 QFN-21 8 x 8mm package outline

Revision history

Document version	Date of release	Description of changes
V0.1b	2019-10-17	1st initial version
V0.2	2020-03-23	New pin configuration, characteristic graphs added, several updates

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Edition 2019-07-18

Published by

Infineon Technologies AG

81726 Munich, Germany

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