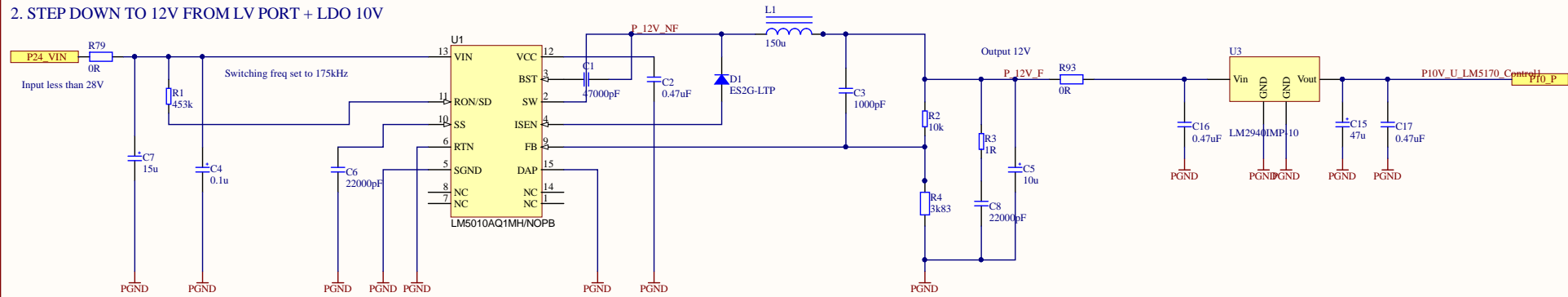
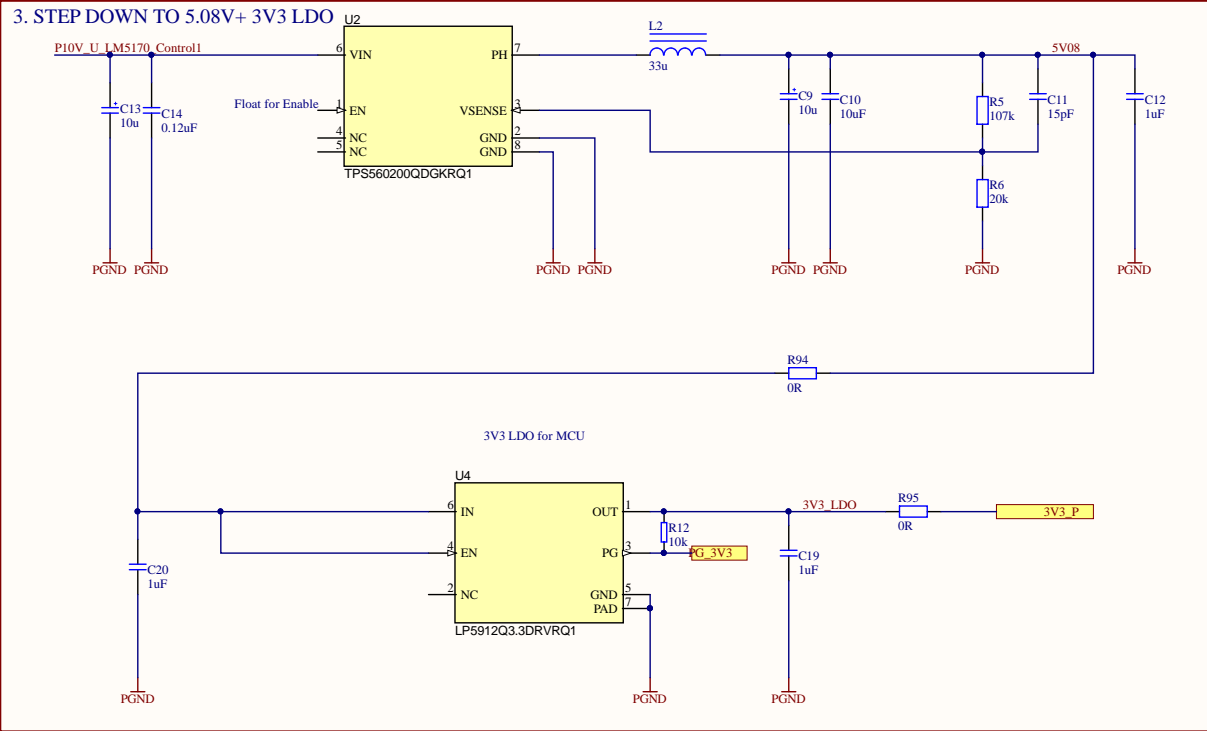


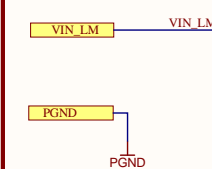
## 2. STEP DOWN TO 12V FROM LV PORT + LDO 10V



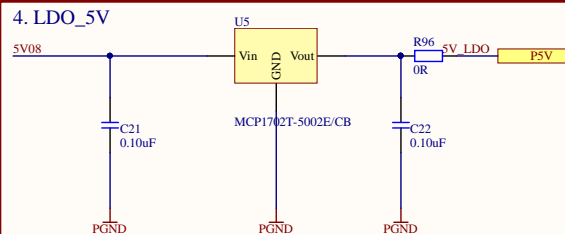
## 3. STEP DOWN TO 5.08V+ 3V3 LDO



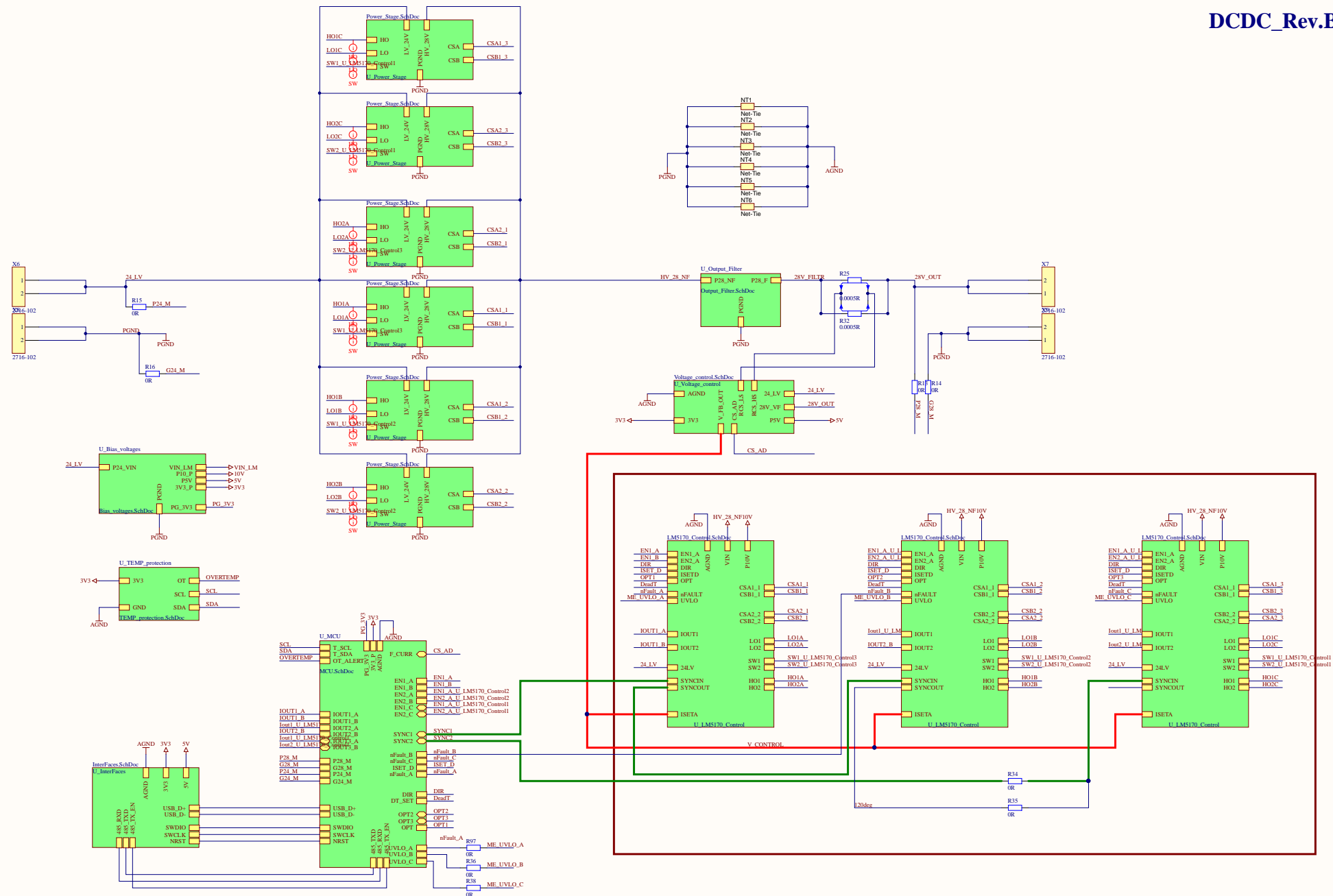
## 1. VIN MANAGEMENT



## 4. LDO\_5V

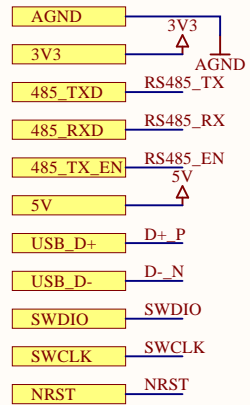


Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...Bias_voltages.SchDoc	Drawn By:

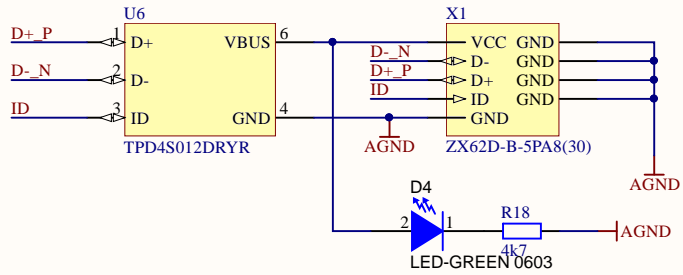


Title		
Size	Number	Revision
A2		
Date:	18/07/2018	Sheet of
File:	C:\Users\DCDC_Hierarchy_SchDoc	Drawn By:

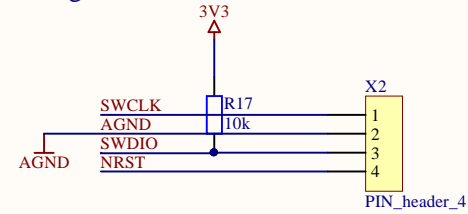
### PORTS



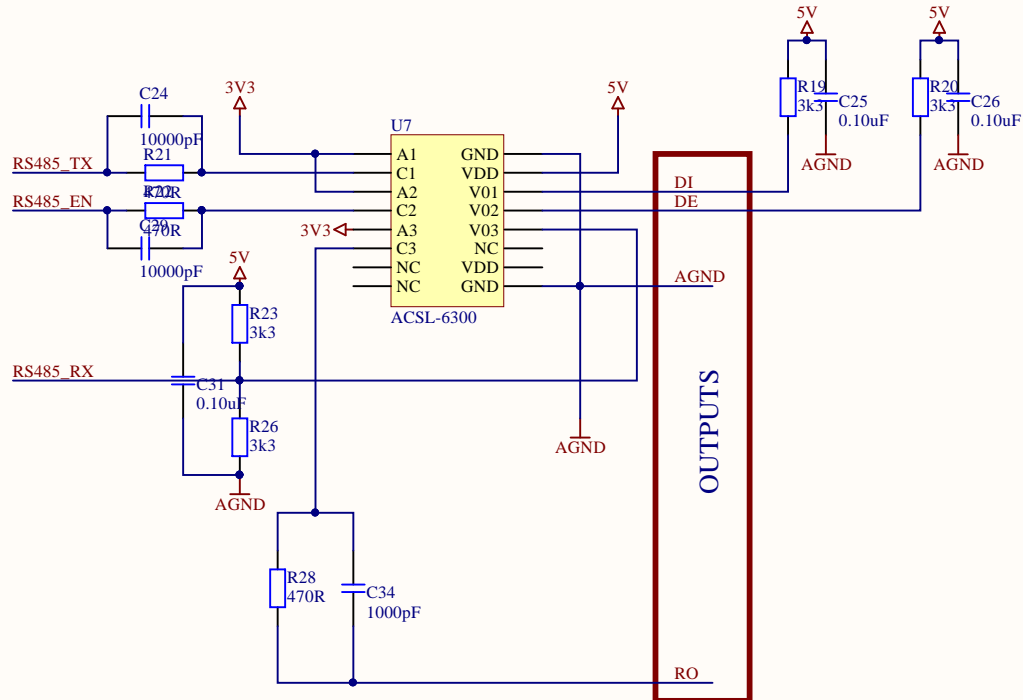
### MICRO\_USB\_ESD



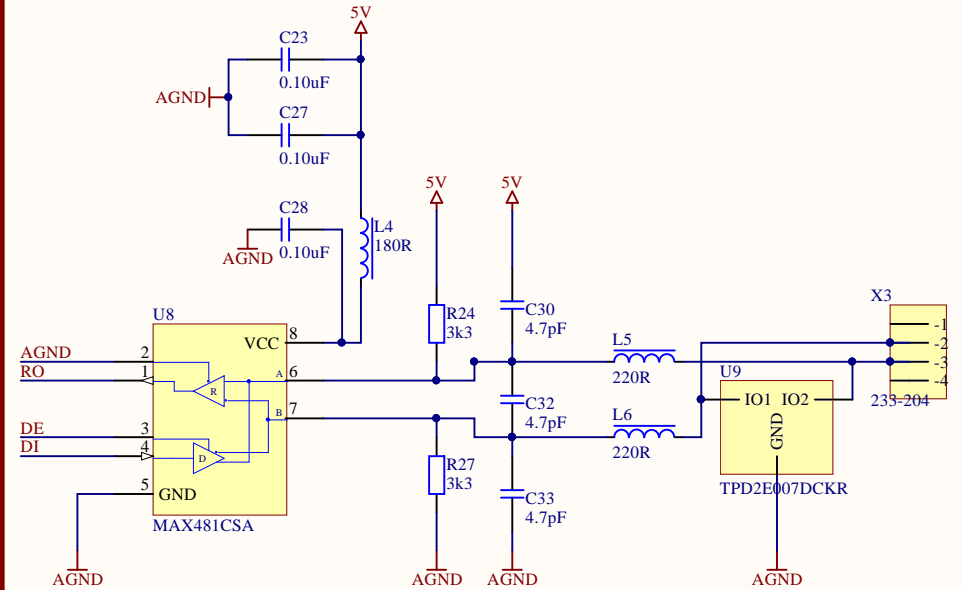
### Programming Pins



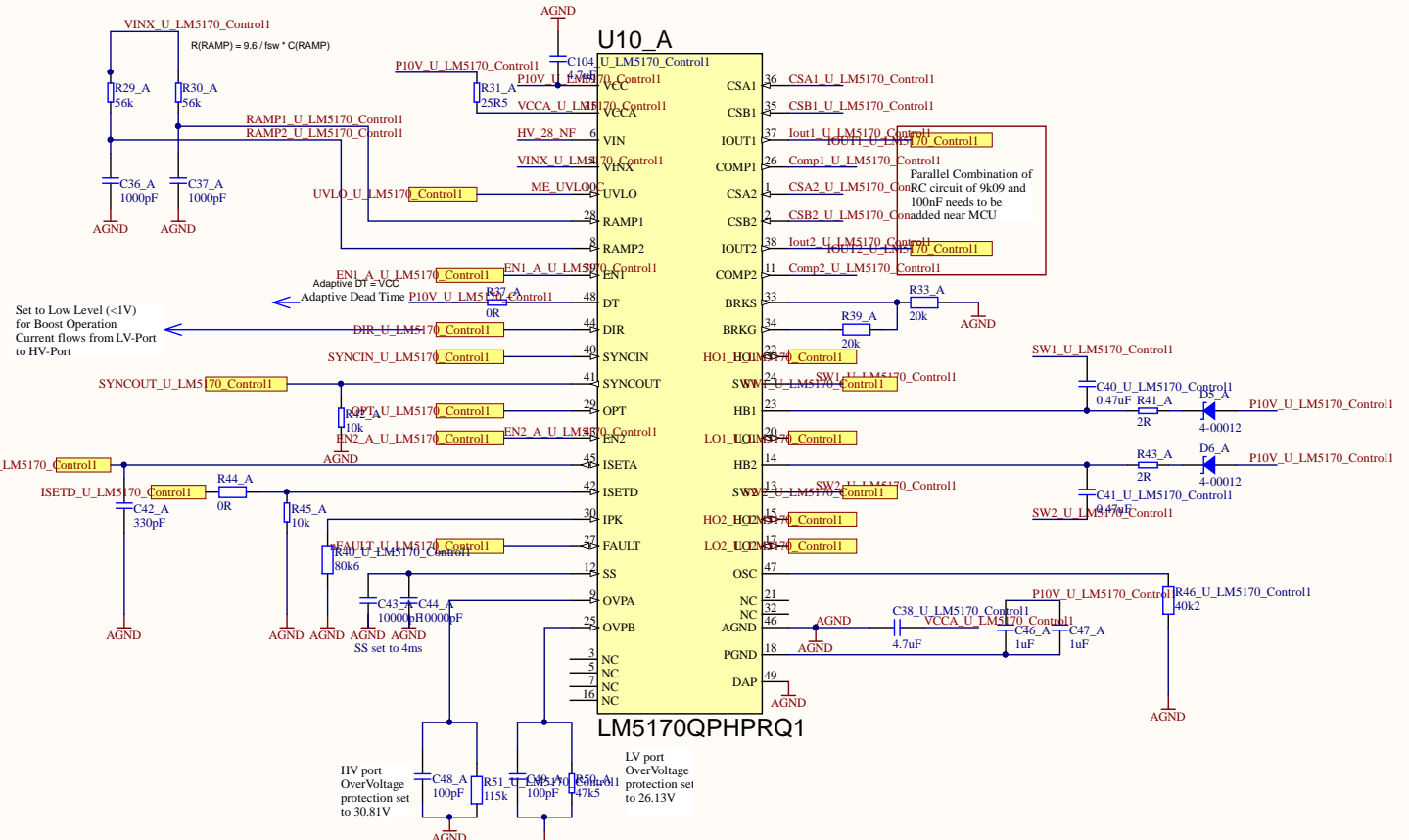
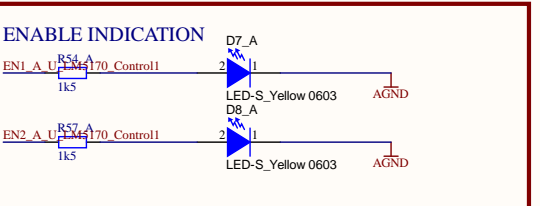
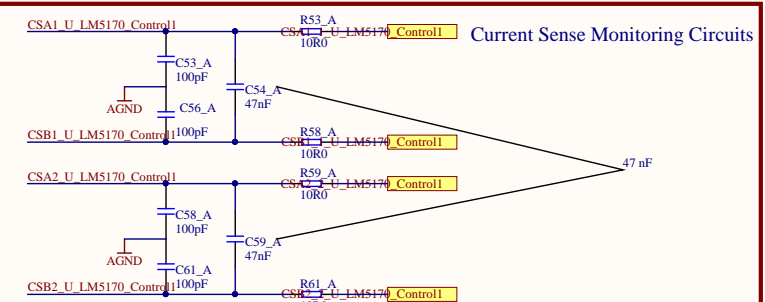
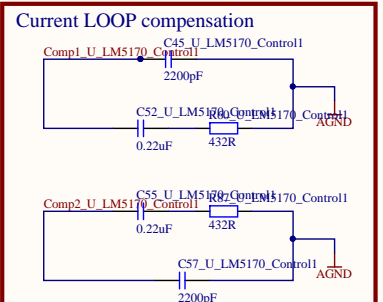
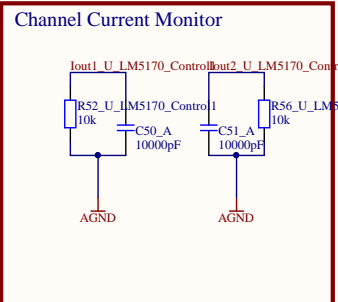
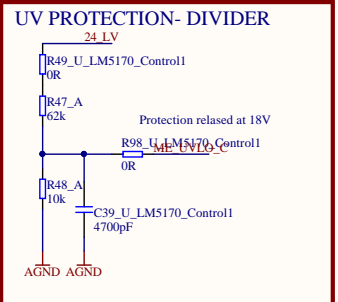
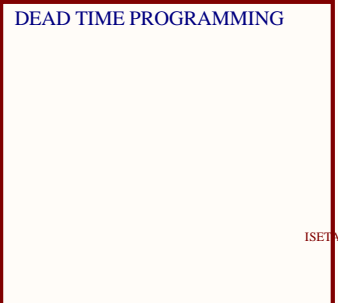
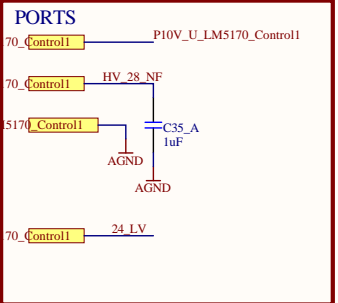
### OPTOCOUPLEDERS



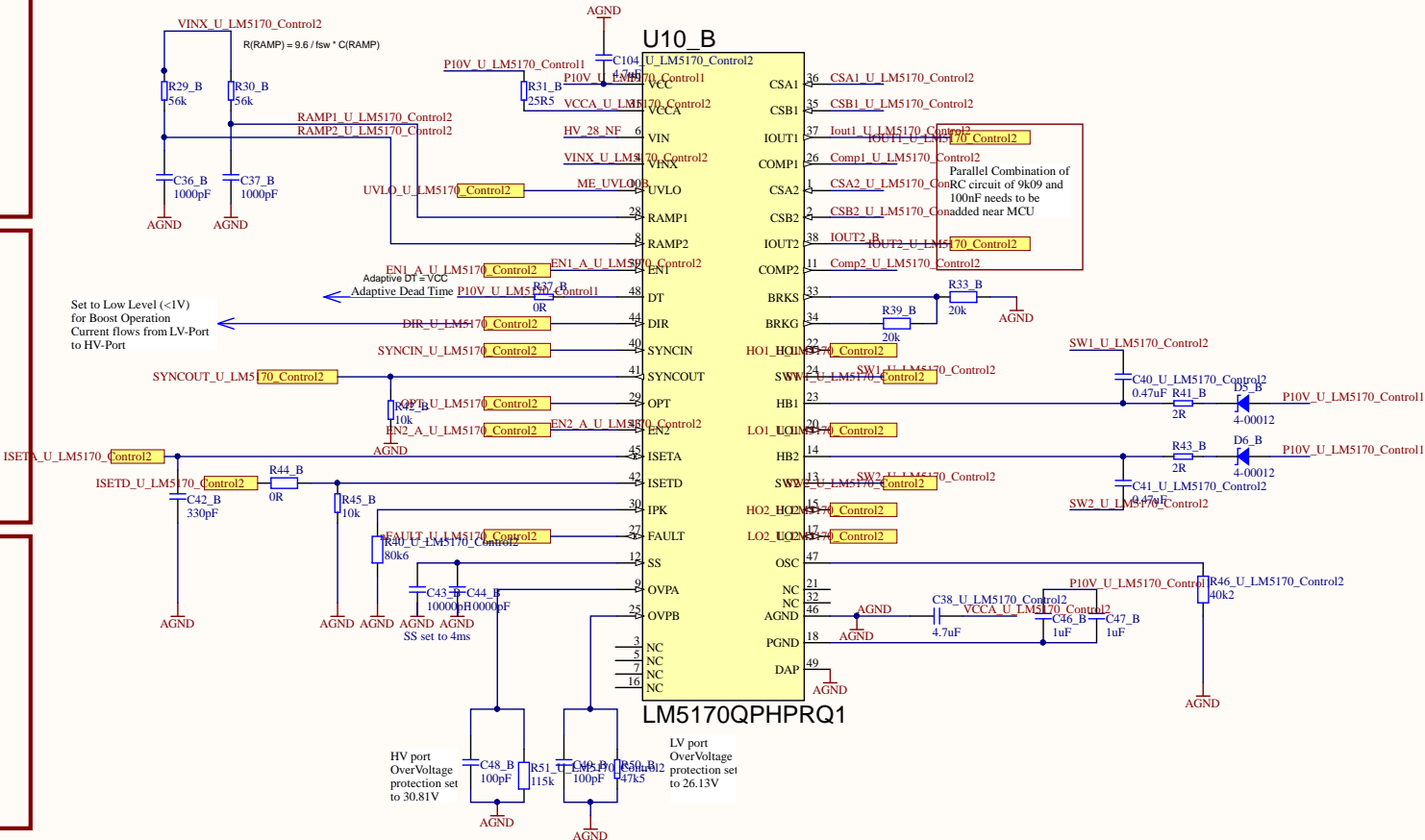
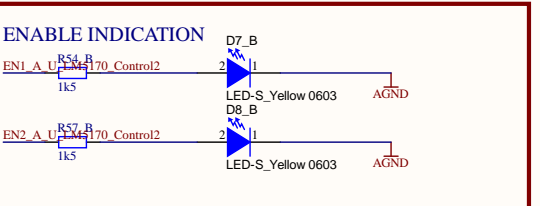
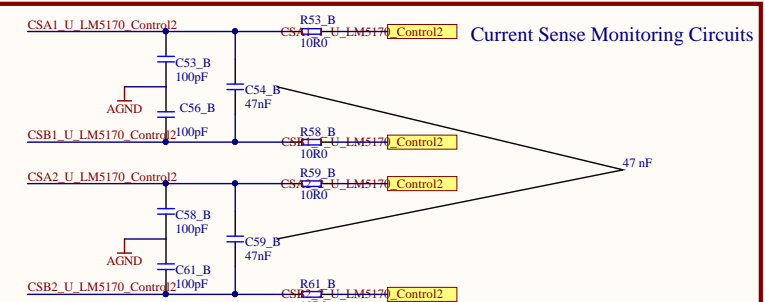
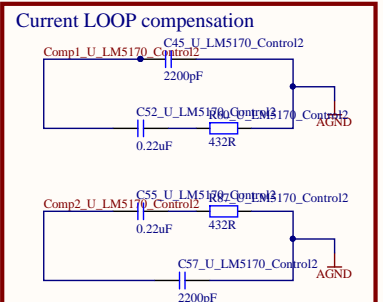
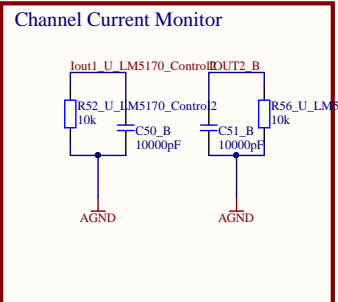
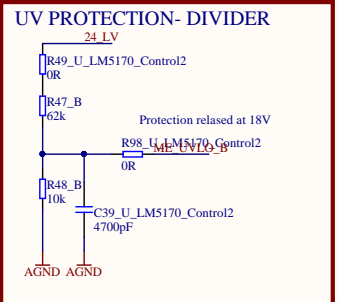
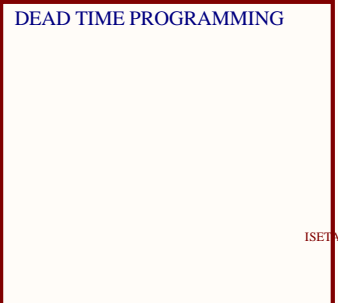
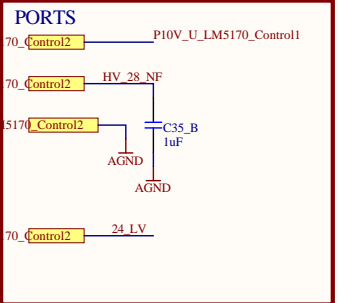
### RS422/485 TRS WITH ESD PROTECTION



Title		Revision	
Size	Number		
A4			
Date:	18.07.2018	Sheet	of
File:	C:\Users\...\InterFaces.SchDoc	Drawn By:	

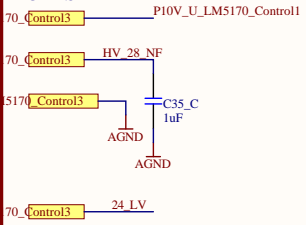


Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...LM5170_Control.SchDoc	Drawn By:



Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...LM5170_Control.SchDoc	Drawn By:

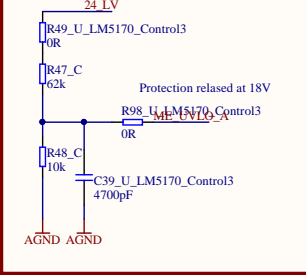
### PORTS



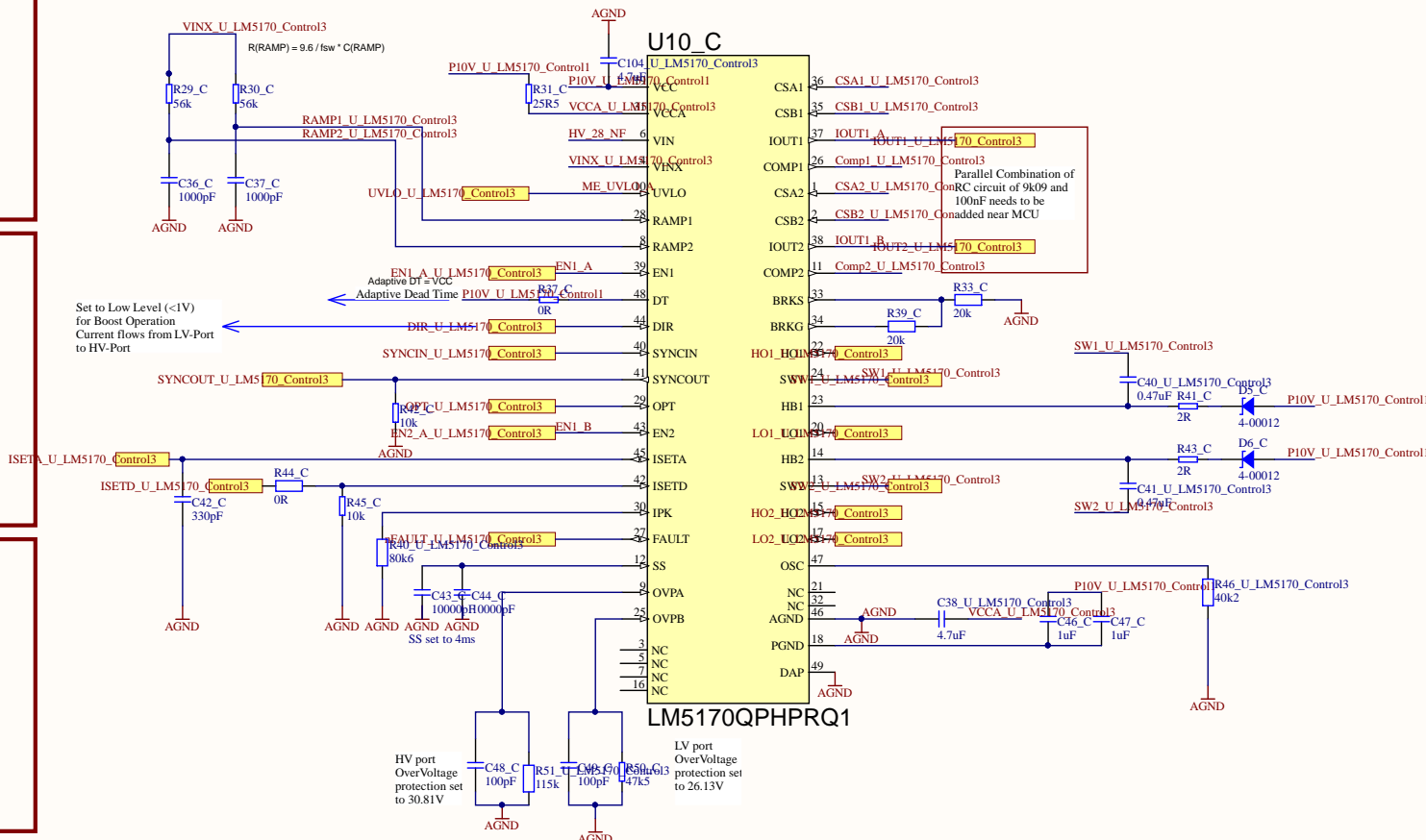
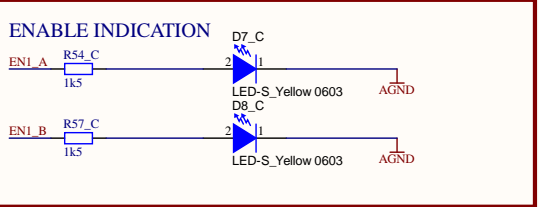
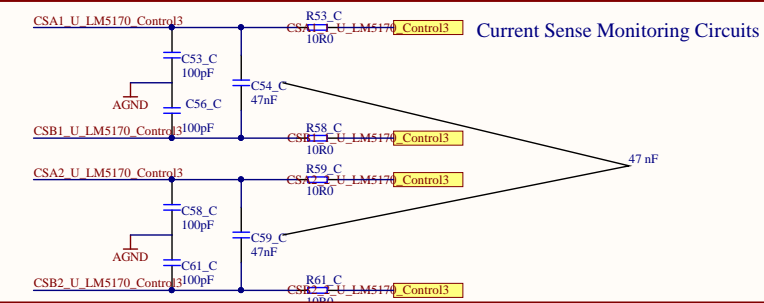
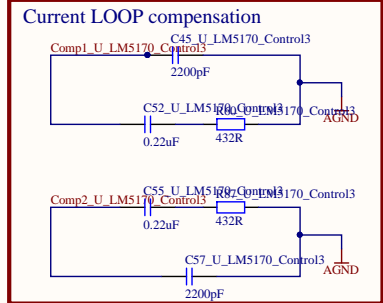
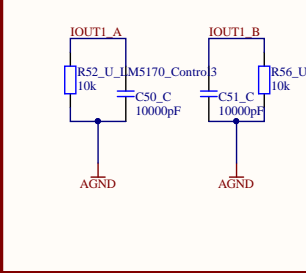
### DEAD TIME PROGRAMMING



### UV PROTECTION- DIVIDER



### Channel Current Monitor

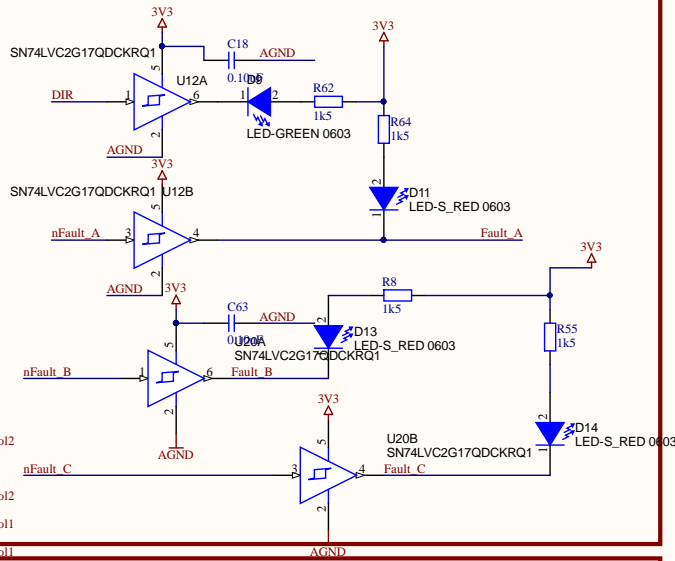


Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...LM5170_Control.SchDoc	Drawn By:

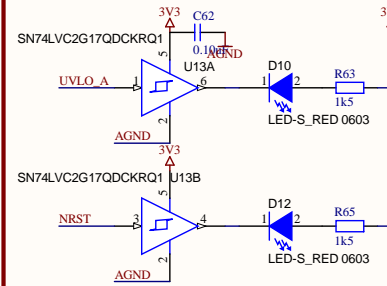
### PORTS

T_SCL	SCL
T_SDA	SDA
OT_ALERT	OVERTEMP
UVLO_A	UVLO_A
UVLO_B	UVLO_B
UVLO_C	UVLO_C
nFault_A	nFault_A
nFault_C	nFault_C
nFault_B	nFault_B
DIR	DIR
AGND	AGND
OPT	OPT1_AGND
OPT2	OPT2
OPT3	OPT3
EN1_A	EN1_A
EN2_A	EN1_A_U_LM5170_Control2
EN1_B	EN1_B
EN2_B	EN2_A_U_LM5170_Control2
EN1_C	EN1_A_U_LM5170_Control1
EN2_C	EN2_A_U_LM5170_Control1
IOUT1_A	IOUT1_A
IOUT1_B	IOUT1_B
IOUT2_A	Iout1_U_LM5170_Control2
IOUT2_B	IOUT2_B
IOUT3_A	Iout1_U_LM5170_Control1
IOUT3_B	Iout2_U_LM5170_Control1
DT_SET	DeadT
P28_M	P28_M
G28_M	G28_M
P24_M	P24_M
G24_M	G24_M
485_TXD	RS485_TX
485_RXD	RS485_RX
485_TX_EN	RS485_EN
USB D+	D+ P
USB D-	D- N
PG_3V3	PG_3V3
3V3_P	3V3
ISET_D	ISET_D
SWCLK	SWCLK
SWDIO	SWDIO
NRST	NRST
SYNC1	SYNC1
SYNC2	SYNC2
F_CURR	CS_AD

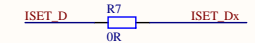
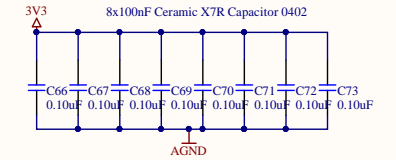
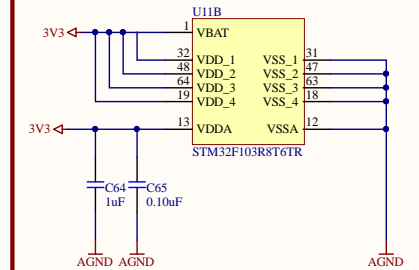
### DIRECTION AND FAULT INDICATION



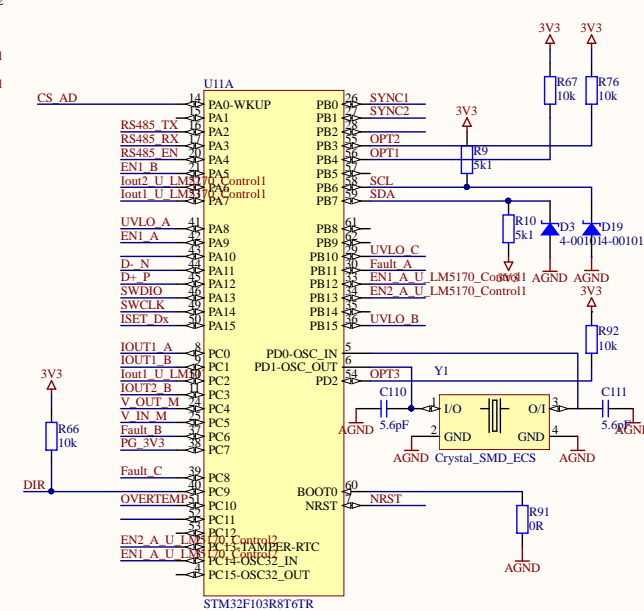
### UVLO\_A AND RST INDICATION



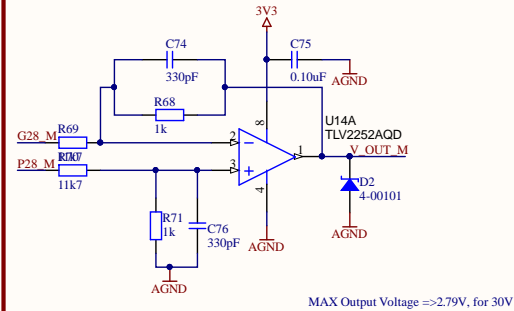
### MCU POWER



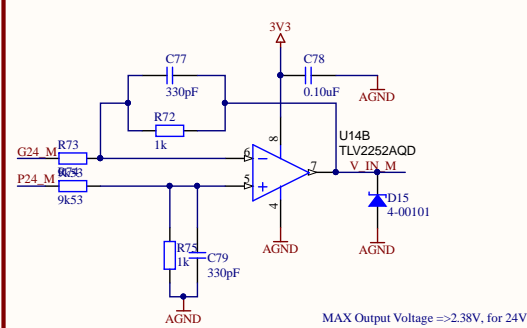
### MCU



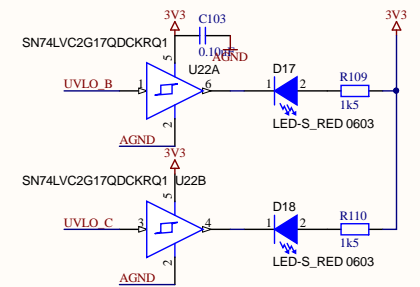
### OUTPUT VOLTAGE MEASUREMENT



### INPUT VOLTAGE MEASUREMENT

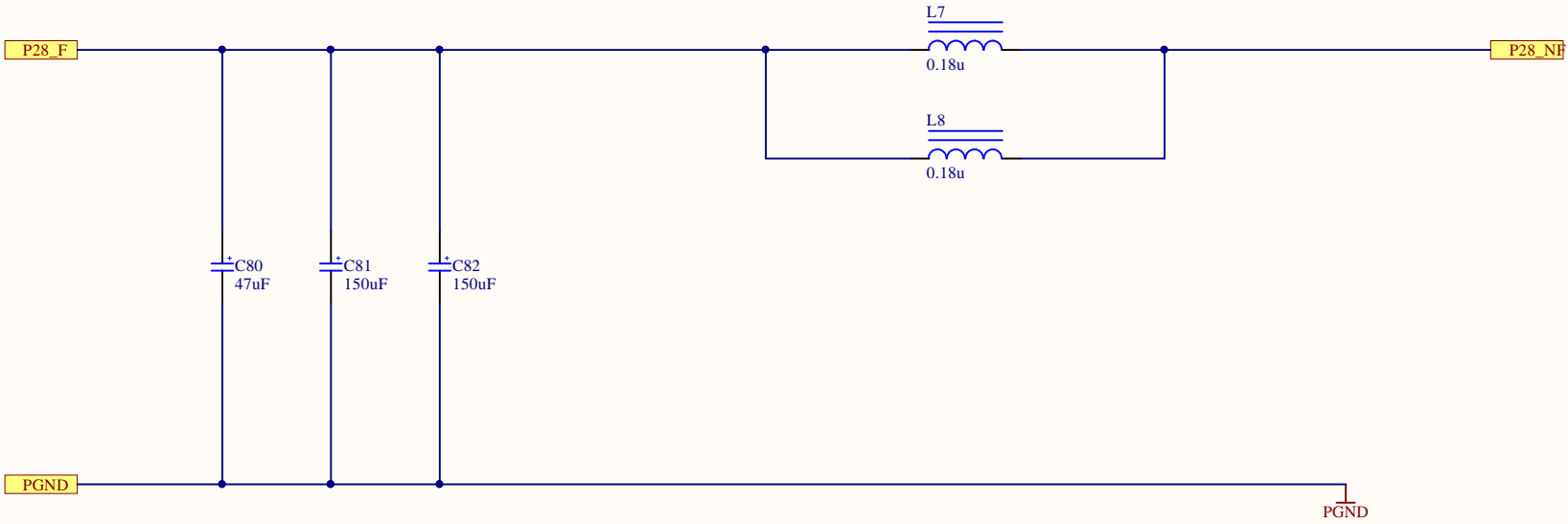


### UVLO\_B AND UVLO\_C Indication



Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...MCU.SchDoc	Drawn By:

### HV PORT FILTER



Title			
Size	Number		Revision
A4			
Date:	18.07.2018	Sheet	of
File:	C:\Users\...\Output_Filter.SchDoc	Drawn By:	

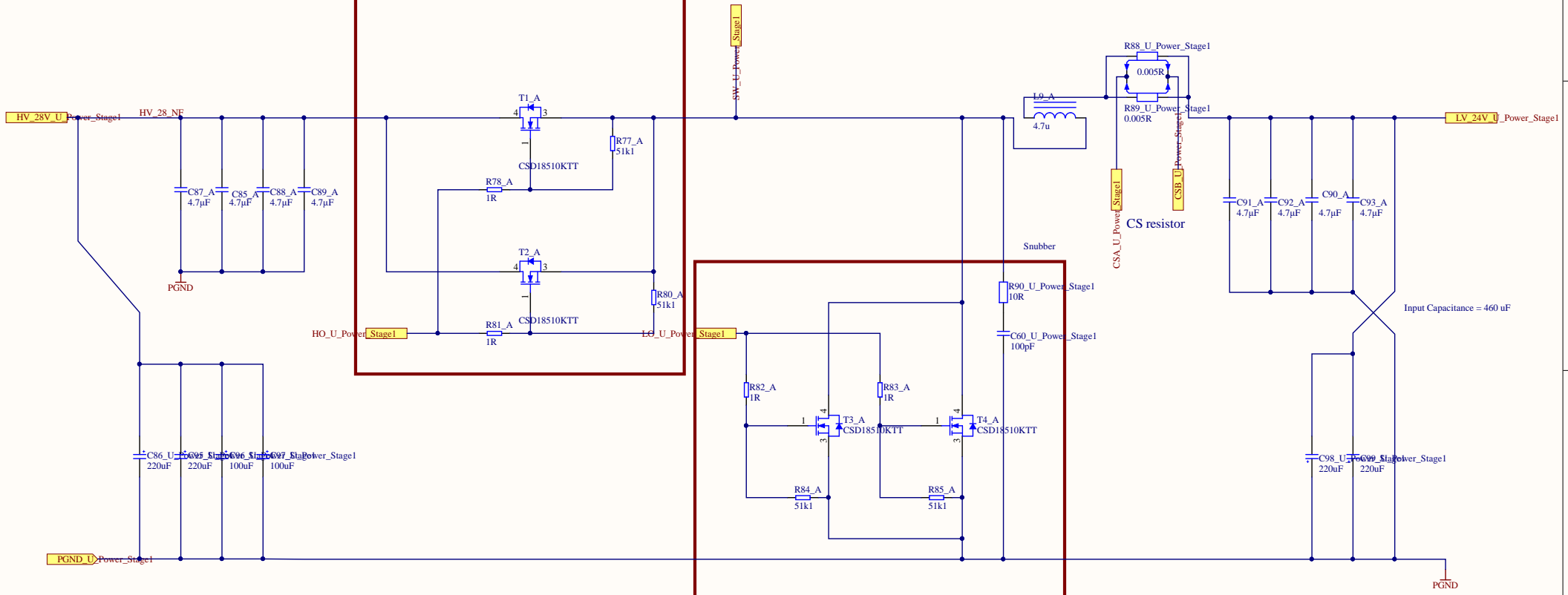


# Power Stage

SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER



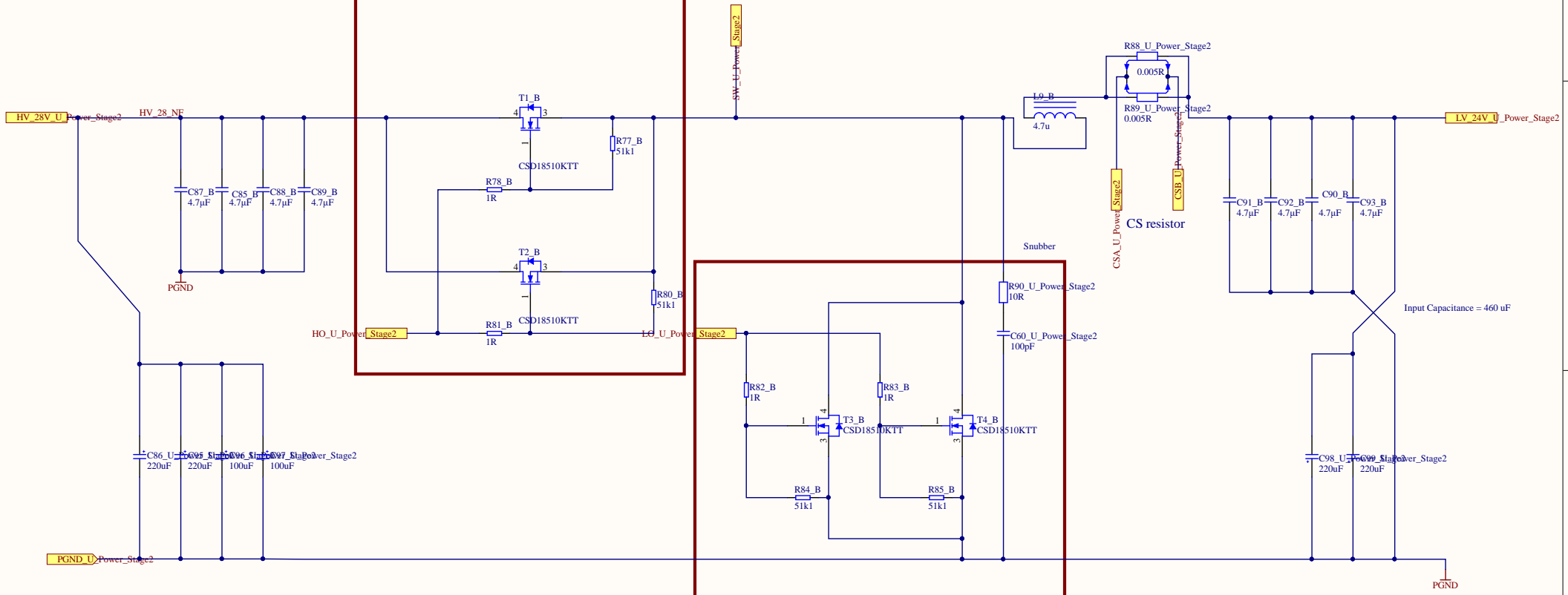
Title		
Size A3	Number	Revision
Date: 18.07.2018	Sheet of	
File: C:\Users\...Power_Stage.SchDoc	Drawn By:	

# Power Stage

SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER



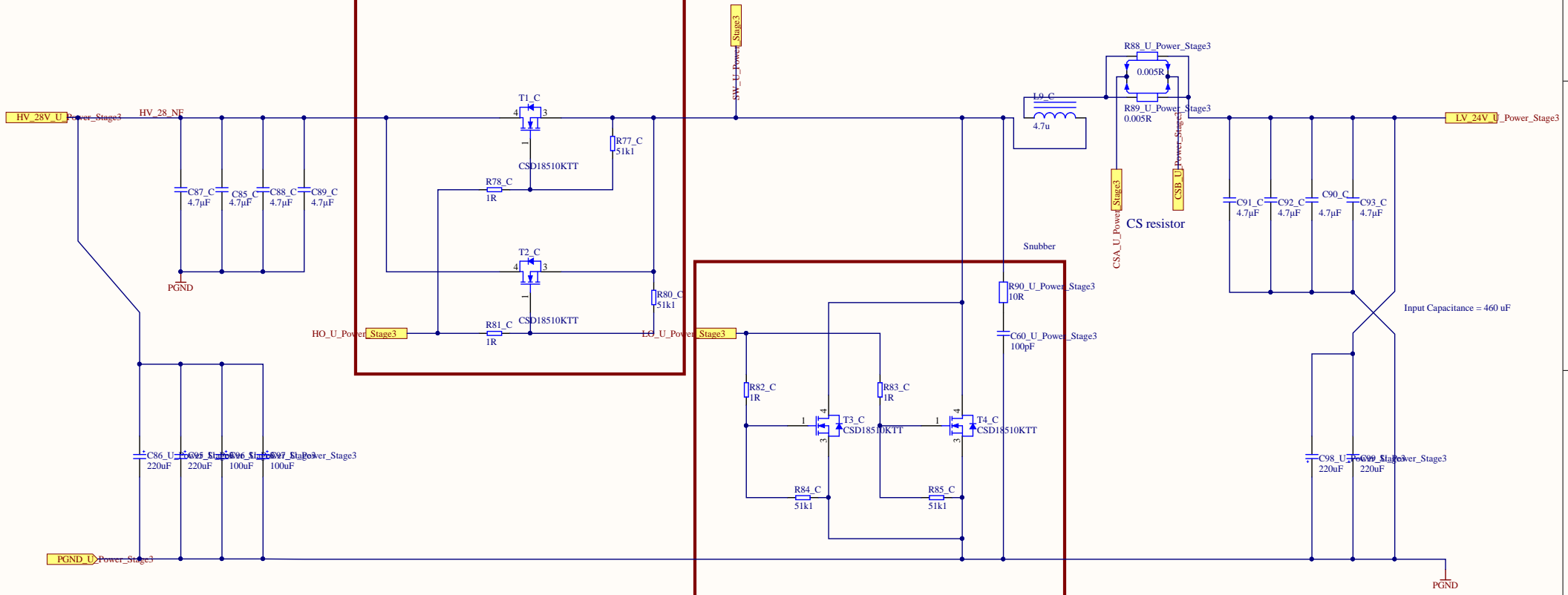
Title		
Size A3	Number	Revision
Date: 18.07.2018	Sheet of	
File: C:\Users\...Power_Stage.SchDoc	Drawn By:	

# Power Stage

SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER



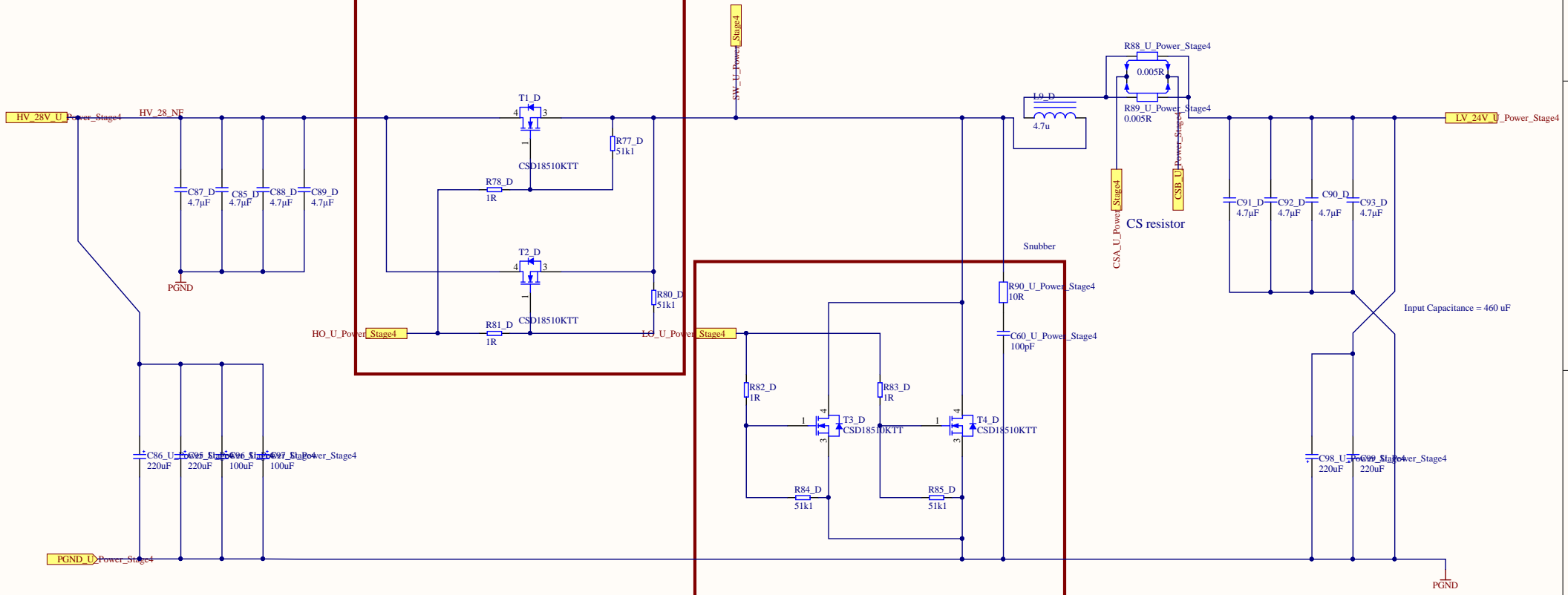
Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...Power_Stage.SchDoc	Drawn By:

# Power Stage

SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER



Input Capacitance = 460 uF

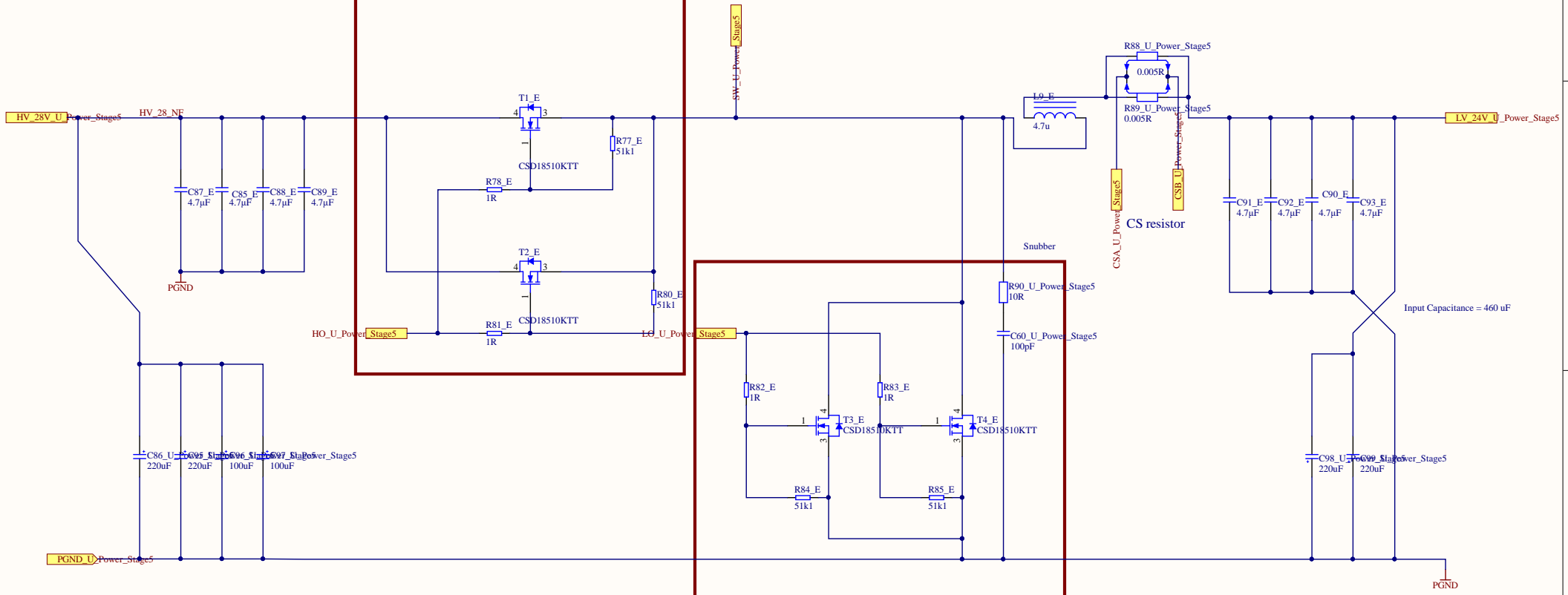
Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...Power_Stage.SchDoc	Drawn By:

# Power Stage

SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER



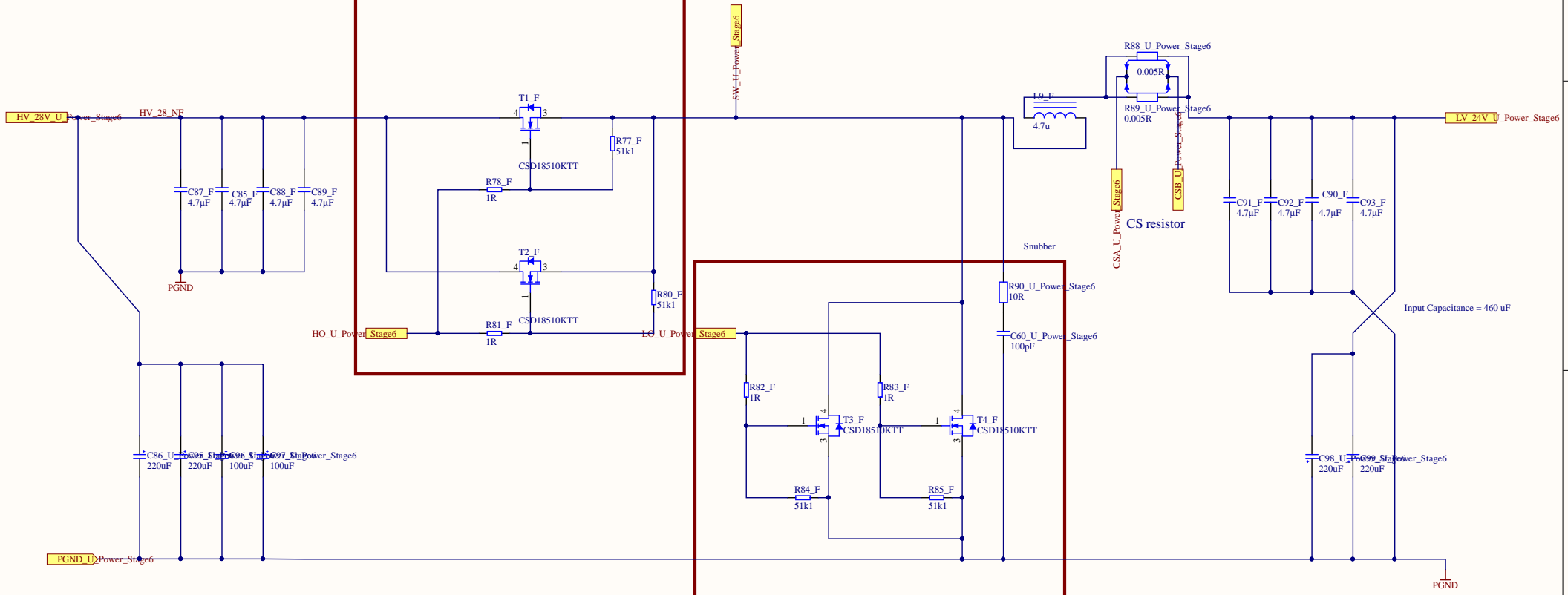
Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...Power_Stage.SchDoc	Drawn By:

# Power Stage

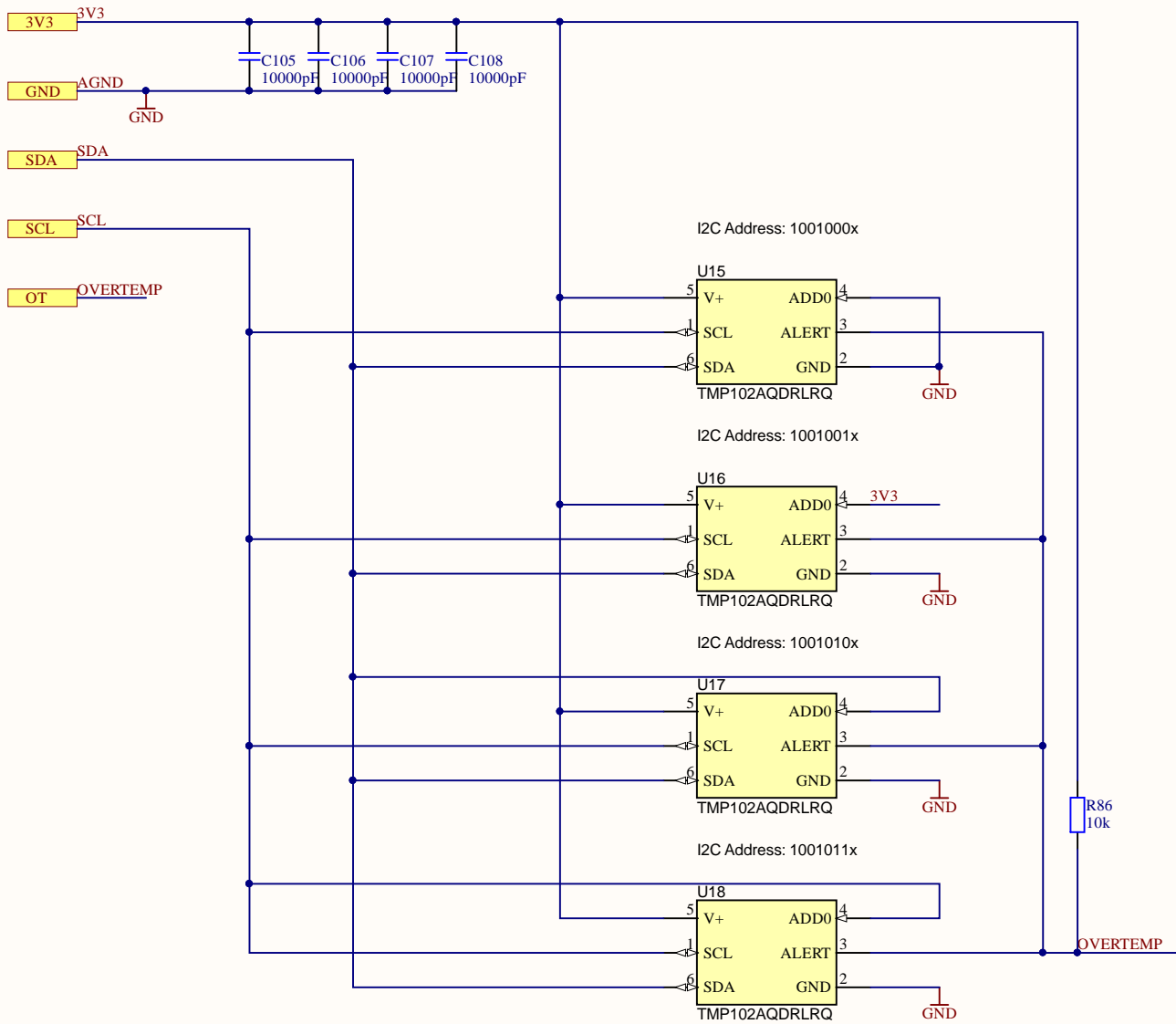
SHUNT RESISTOR

HIGH SIDE GATE DRIVER

LOW SIDE GATE DRIVER

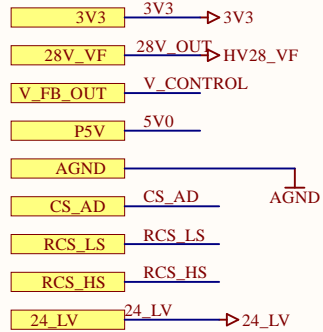


Title		
Size	Number	Revision
A3		
Date:	18.07.2018	Sheet of
File:	C:\Users\...Power_Stage.SchDoc	Drawn By:

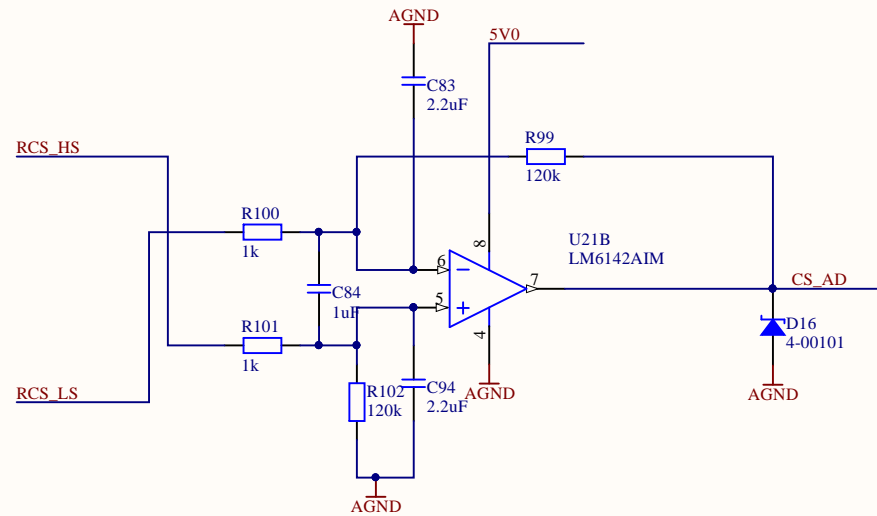
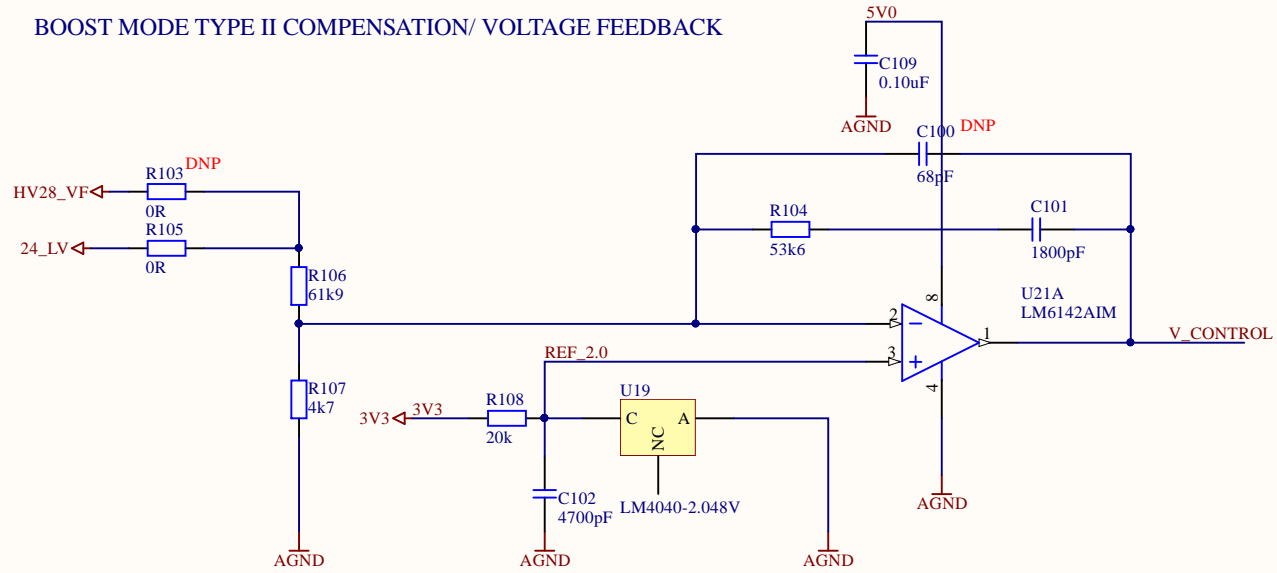


Title		
Size	Number	Revision
A4		
Date:	18.07.2018	Sheet of
File:	C:\Users\...\TEMP_protection.SchDoc	Drawn By:

**PORTS**



**BOOST MODE TYPE II COMPENSATION/ VOLTAGE FEEDBACK**



Title		
Size A4	Number	Revision
Date: 18.07.2018	Sheet of	
File: C:\Users\...\Voltage_control.SchDoc	Drawn By:	