

TIDA-00465 Test Report

Eric Wright

LP/PI

Abstract

TI design TIDA-00465 is an application using TPS23861 as a single port, type 2, PoE auto-mode PSE in a small form factor. Input voltage to the unit is 44V-57V using any commonly available 40W AC-DC power supply. The design will inject power onto any Ethernet cable for PoE powered loads up to 30W.

The circuit is placed on a 1.6" x 2.4" PCB with the key TPS23861 circuit occupying only 0.35 in^2 .

The TIDA-00465 is derived from application design PR2207. Both numbers may appear in documentation but refer to a single common design.

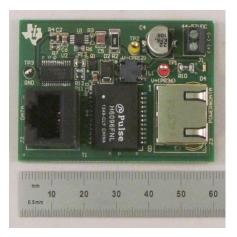


Figure 1. TIDA-00465 Photo

Document History

Version	Date	Author	Notes
1.0	January 2015	Eric Wright	First release



System Connection Diagram

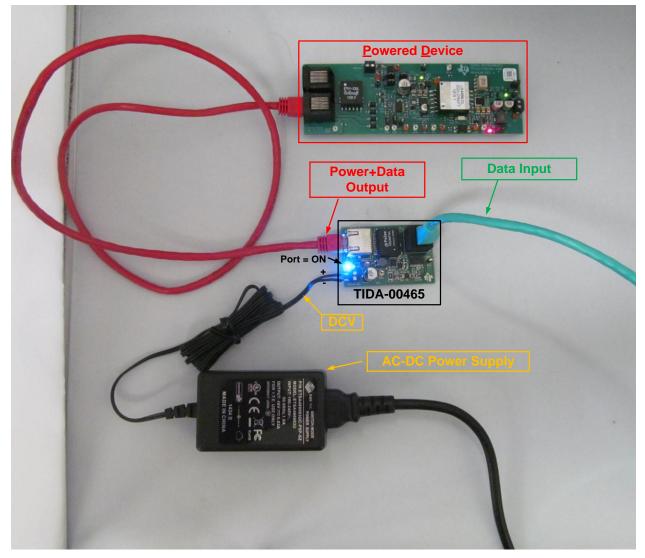


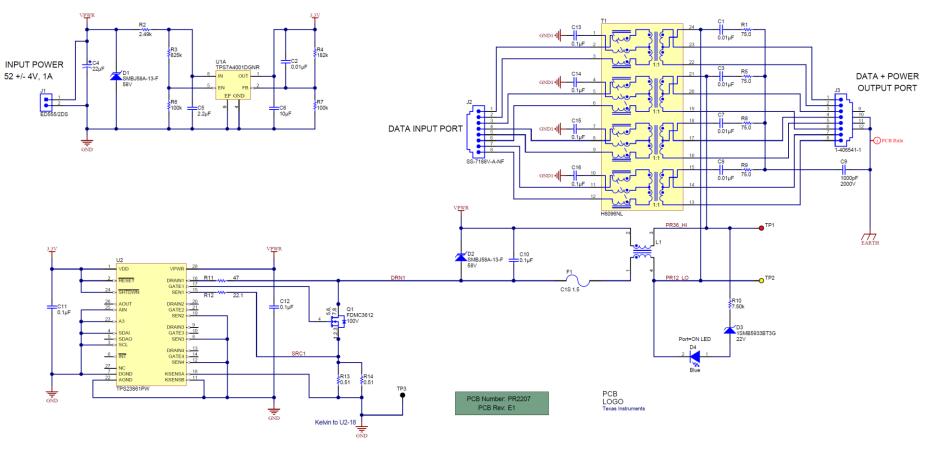
Figure 2 System Connection Diagram

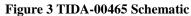


Test Report January 2015

Schematic

• The TIDA-00465 schematic is shown in Figure 3.







Test Results

 Figure 4 shows typical start up behavior for a type 2 PD. TPS23861 automatically performs four point detection, two-event physical classification of type 2 PDs, and inrush protected power ramp up.

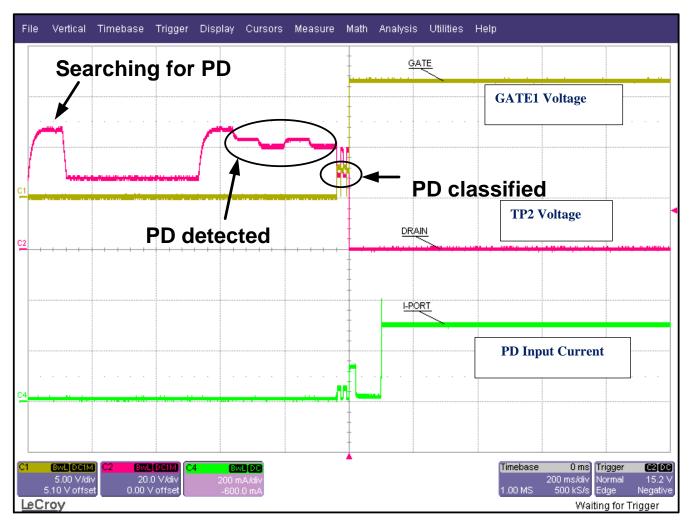


Figure 4 Start Up type 2 PD load

 Table 1 documents the IEEE 802.3at conformance test results using the Sifos[™] Technologies PSA-3000 test suite for a 30W PSE. Table 2 documents the IEEE 802.3at conformance test results using the Sifos[™] Technologies PSA-3000 test suite for a 15.4W PSE.



PSA TEST RESULTS February 9 2015		Sifos					mance Report version 4.0.77		
Port Count	1		Techno	logies ₁	Fest Mode:	30 Watt Pl	ΗY	report versio	on 4.0.13
Loop Count.	10		Error		op Index*:		/DortPo	ng/psa_error_	log tit
PSE Tested: PortBang Type-2			EITOI LOG.	C./OSEIS/Pu	1011C/31105/P3				
Chassis ID: 158.218.10.73		000 Ports				Low	P/F	High	P/F
TestLoop: 1	1-1	UNITS	Min	Мах	Average	Limit	-	Limit	
Test: det_v Open Circuit Det Voc=	19.85	volts	19.85	19.85	19.85	2.8	Pass	30	Pass
Peak Det Vvalid=	7.09	volts	7.09	7.09	-	3.8	Pass	10	Pass
Min Det Vvalid=	4.56	volts	4.56	4.56		2.8	Pass	9	Pass
Det Volt Step dVtest=	2.53	volts	2.53	2.53	2.53	1	Pass	7.2	Pass
Detection Slew=	0	V/usec	0	0	-	0	Pass	0.1	Pass
Good Sig Det Pulse=	3	edges	3	3	-	1	Pass	9	Pass
Backoff Voltage=	0.3	volts	0.3	0.3	-	0	Pass	2.8	Pass
Non 802 Step V=	0	volts	0	0	0	0	Pass	0.1	Pass
High Sig MaxV=	10.99	volts	10.99	10.99	10.99	3.8	Pass	11	Pass
Non_802 Discr ?=	0	****	0	0	0	0	Pass	0	Pass
Detect Strategy=	0	****	0	0	0	0	Pass	2	Pass
Test: det_i									
Init_Current_Isc=	0.18	mA	0.18	0.18	0.18	0	Pass	5	Pass
Det_Current_Isc=	0.21	mA	0.21	0.21	0.21	0	Pass	5	Pass
Test: det_range									
Rgood_Max=	28	Kohm	28	28	-	26	Pass	32	Pass
Rgood_Min=	17	Kohm	17	17	17	16	Pass	19	Pass
Rmid_det=	28	Kohm	28	28	-	26	Pass	33	Pass
Cgood Max=	0.1	uF ****	0.1	0.1	0.1	0	Pass	10	Pass
Rbad_Cbad_Stat=	0		0	0	0	0	Pass	0	Pass
Test: det_time	00		00	00			Dees	4500	Dees
Backoff_Time_Tdbo=	86	msec	86 86	86		-1 -1	Pass	1500	Pass
Eff_Backoff_Tdbo_eff=	86 0	msec ****	00	86 0		-1	Pass Pass	1500 0	Pass Pass
Backoff_Type=	313		313	313		5	Pass	500	Pass
Detection_Time_Tdet= Total_Det_Time=	313	msec msec	313	313	-	5	Pass	1000	Pass
Test: det rsource	510	mbec	510	510	510	5	1 055	1000	1 855
Output Impedance Zout=	450	KOhm	450	450	450	45	Pass	2000	Pass
Test: class v	100		100	100	100	10	1 400	2000	1 400
Class Voltage Vclass=	18.6	volts	18.6	18.6	18.6	15.5	Pass	20.5	Pass
Vclass Min=	18.6	volts	18.6	18.6	-	15.5	Pass	20.5	Pass
Mark Voltage Vmark=	8.4	volts	8.4	8.4	8.4	7	Pass	10	Pass
Mark Voltage Min=	8.4	volts	8.4	8.4	8.4	7	Pass	10	Pass
Test: class_time									
Event_Count=	2	****	2	2	2	2	Pass	3	Pass
Event1_Tcle1=	11.3	msec	11.3	11.3	11.3	6	Pass	30	Pass
Event2_Tcle2=	10.9	msec	10.9	10.9	10.9	6	Pass	30	Pass
Mark_Tmel=	7.4	msec	7.4	7.4	7.4	6	Pass	12	Pass
Mark Tme2=	9	msec	9	9	9	6	Pass	376	Pass
Test: class_err									
Class_lim=	75	mA	75	75		51	Pass	100	_
Vport_CL_lim=	14.7	V	14.7	14.7	14.7	0	Pass	20.5	·
Vport_CL_err_1=	18.6		18.6	18.6	-	-	Pass	20.5	Pass
Mark_lim=	6		6	6	-	5	Pass	100	Pass
Vport_CL_err_2=	3	V	3	3	-	0		20.5	Pass
Treset=	92	msec	92	92	92	15	Pass	10000	Pass

Table 1. IEEE 802.3at Conformance Report; 30W PSE

Table 1-continued

Test: pwrup_time							_		_
Pwr-On_Rise_Time_Trise=	88	USEC	88	88	88	15		50000	Pass
Power-On_Time_Tpon=	35.2	msec	35.2	35.2	35.2	0	Pass	400	Pass
Test: pwrup_inrush									
Init Iinrush=	421.13	mA	421.13	421.13	421.13		Pass	450	Pass
Max_Iinrush_c4=	421	mA	421	421	421	400	Pass	450	Pass
Min_Iinrush=	420.75	mA	420.75	420.75	420.75	400	Pass	450	Pass
Tinrush=	60.7	msec	60.7	60.7	60.7	50	Pass	75	Pass
Inrush_45m=	51.9	Volts	51.9	51.9	51.9	50		57	Pass
Inrush_Voltage=	30.6		30.6	30.6	30.6	30	Pass	57	Pass
Max_Init_Inrush=	421	mA	421	421	421	0	Pass	2000	Pass
Inrush Strategy=	0	****	0	0	0	0	Pass	0	Pass
Test: pwron_v									
Vport_min_2=	51	V	51	51	51	50		57	Pass
Vport_max_2=	52	V	52	52	52	50		57	Pass
Vport_ripple_2=	2	mVpp	2	2	2	0		500	Pass
Vport_noise_2=	21	mVpp	21	21	21	0	Pass	200	Pass
Vtrans min 2=	51	V	51	51	51	50	Pass	57	Pass
Vtrans_max_2=	52.1	V	52.1	52.1	52.1	50	Pass	57	Pass
Test: pwron_pwrcap									
Pcon_c4=	31.4	watts	31.4	31.4	31.4	30	Pass	38.9	Pass
Iconc4=	614	mA	614	614	614	526.3	Pass	683	Pass
Type-2_Enable=	1	****	1	1	1	1	Pass	1	Pass
Test: pwron_maxi									
Ilim_Peak=	98.3	mA	98.3	98.3	98.3	0	Pass	1750	Pass
	685.5	mA	685.5	685.5	685.5	683	Pass	1750	Pass
Tlim_2=	61.3	msec	61.3	61.3	61.3	10	Pass	75	Pass
Vlim_2=	50.8	V	50.8	50.8	50.8	50	Pass	57	Pass
Ilim_Max_2=	859.5	mA	859.5	859.5	859.5	0	Pass	1750	Pass
Ilim_Low_V_Tol_2=	60.2	msec	60.2	60.2	60.2	10	Pass	9999	Pass
Ktran lo 2=	101.5	%	101.5	101.5	101.5	92.4	Pass	115	Pass
Test: pwron_overld									
%Ipeak_2=	125	%	125	125	125	0	Pass	125	Pass
Vport_Ipeak_2=	50.8	V	50.8	50.8	50.8	50	Pass	57	Pass
Vport_5%DC_2=	50.9	V	50.9	50.9	50.9	50	Pass	57	Pass
Test: mps_dc_valid									
Min_Valid_Time_Tmps=	50		50	50	50	1	Pass	60	Pass
Duty_Cycle_tol=	1	****	1	1	1	1	Pass	1	Pass
Test: mps_dc_pwrdn									
Min_Valid_I_hold=	5	mA	5	5	5	5	Pass	10	Pass
Time-to-Shutdown_Tmpdo=	364	msec	364	364	364	300	Pass	400	Pass
Max_Voltage_Vopen_max=	19.9	volts	19.9	19.9	19.9	-1	Pass	30	Pass
Test: pwrdn_overld									
Icut 2=	641	mA	641	641	641	-1	Pass	683	Pass
Tcut 2=	63.5	msec	63.5	63.5	63.5	10	Pass	9999	Pass
Isoft 2=	-1	mA	-1	-1	-1	-1	Pass	683	Pass
Tsoft_2=	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
Test: pwrdn_time									
Turn-Off_Time_Toff=	15.5	mSec	15.5	15.5	15.5	0	Pass	500	Pass
Output Cap Cout=	0.0643	uF	0.0643	0.0643	0.0643	-1	Pass	0.52	Pass
Output Load Rp=	116.8	Kohm	116.8	116.8	116.8	45	Pass	50000	Pass
Test: pwrdn v							-		-
Test: pwrdn_v Avg Idle Voff=	0.1	VDC	0.1	0.1	0.1	0	Pass	2.8	Pass
	0.1 1406.3		0.1	0.1 1406.3	0.1 1406.3		-	2.8 10000	Pass Pass



PSA TEST RESULTS February 9 2015		Sif	OS [™]	802.3at Conformance Report version 4.0.77					
Port Count	1		Techno	logies	Fest Mode:	15.4 Watt		report version	on 4.0.13
Loop Count	10			Sifos Inter	op Index*:	100%			
PSE Tested: PortBang Type-1		Error Log:	None						
Chassis ID: 158.218.10.73	PSA-3	000 Ports				Low	P/F	High	P/F
TestLoop: 1	1-1	UNITS	Min	Max	Average	Limit	• • •	Limit	• • •
Test: det v		GINITO		Мил	Average			Linit	
Open Circuit Det Voc=	19.85	volts	19.85	19.85	19.85	2.8	Pass	30	Pass
Peak Det Vvalid=	7.1	volts	7.1	7.1	7.1	3.8	Pass	10	Pass
Min Det Vvalid=	4.55		4.55	4.55	4.55	2.8	Pass	9	Pass
Det Volt Step dVtest=	2.55		2.55	2.55	2.55	1	Pass	7.2	Pass
Detection Slew=	0		0	0	0	0	Pass	0.1	Pass
Good Sig Det Pulse=	3		3	3	3	1	Pass	9	Pass
Backoff Voltage=	0.3	0	0.3	0.3	0.3	0	Pass	9	Pass
Non 802 Step V=	0		0	0	0	0	Pass	0.1	Pass
High Sig MaxV=	10.99	volts	10.99	10.99	10.99	3.8	Pass	11	Pass
Non 802 Discr ?=	0	****	0	0	0	0	Pass	0	Pass
Detect Strategy=	0	****	0	0	0	0	Pass	2	Pass
Test: det i									
Init Current Isc=	0.18	mA	0.18	0.18	0.18	0	Pass	5	Pass
Det Current Isc=	0.2	mA	0.2	0.2	0.2	0	Pass	5	
Test: det range									
Rgood Max=	28	Kohm	28	28	28	26	Pass	32	Pass
Rgood Min=	17	Kohm	17	17	17	16	Pass	19	Pass
Rmid det=	28	Kohm	28	28	28	26	Pass	33	Pass
Cgood Max=	0.1	uF	0.1	0.1	0.1	0	Pass	10	Pass
Rbad Cbad Stat=	0	****	0	0	0	0	Pass	0	Pass
Test: det time				-	-				
Backoff Time Tdbo=	86	msec	86	86	86	-1	Pass	1500	Pass
Eff Backoff Tdbo eff=	86	msec	86	86	86	-1	Pass	1500	Pass
Backoff Type=	0	****	0	0	0	0	Pass	0	Pass
Detection Time Tdet=	313	msec	313	313	313	5	Pass	500	Pass
Total Det Time=	316	msec	316	316	316	5	Pass	1000	Pass
Test: det rsource						-			
Output Impedance Zout=	450	KOhm	450	450	450	45	Pass	2000	Pass
Test: class v						-			
Class Voltage Vclass=	18.9	volts	18.9	18.9	18.9	15.5	Pass	20.5	Pass
Vclass Min=	18.7	volts	18.7	18.7	18.7	15.5	Pass	20.5	Pass
Test: class time						-			
Event Count=	1	****	1	1	1	0	Pass	3	Pass
Class Time Tpdc=	11.3	msec	11.3	11.3	11.3	6	Pass	75	Pass
Test: class err									
Class lim=	75	mA	75	75	75	51	Pass	100	Pass
Vport CL lim=	14.9		14.9	-		0		57	
Vport CL err 1=	18.5	V	18.5	18.5	18.5	0	Pass	57	Pass
Test: pwrup time									
Pwr-On Rise Time Trise=	40	usec	40	40	40	15	Pass	50000	Pass
Power-On Time Tpon=	11.7	msec	11.7	11.7	11.7	0	~	400	Pass
Test: pwrup inrush									
Init Iinrush=	423	mA	423	423	423	400	Pass	450	Pass
Max Iinrush c0=	421.63		421.63				-	450	-
Min Iinrush=	420.88		420.88	420.88			/	450	-
	60		60	60		50	-	75	
Inrush 45m=	51.9		51.9	51.9	-	-	7	57	-
Inrush Voltage=	30.6		30.6	30.6		·		57	-
							-		-
Max Init Inrush=	616.3	mA	616.3	616.3	616.3	0	Pass	2000	Pass

Table 2. IEEE 802.3at Conformance Report; 15.4W PSE

Table 2-continued

Test: pwron_v							_		_
Vport_min_1=	51.5	V	51.5	51.5	51.5	50	Pass	57	Pass
Vport_max_1=	52	V	52	52	52	50	Pass	57	Pass
Vport ripple 1=	2	mVpp	2	2	2	0	Pass	500	Pass
Vport_noise_1=	14	mVpp	14	14	14	0	Pass	200	Pass
Vtrans_min_1=	51.5	V	51.5	51.5	51.5	50	Pass	57	Pass
Vtrans_max_1=	52.1	V	52.1	52.1	52.1	50	Pass	57	Pass
Test: pwron_pwrcap									
Pcon_c0=	18.2	watts	18.2	18.2	18.2	15.4	Pass	22.7	Pass
Icon_c0=	353	mA	353	353	353	270.2	Pass	399	Pass
Pcon_c1=	17.6	watts	17.6	17.6	17.6	4	Pass	22.7	Pass
Icon cl=	341	mA	341	341	341	70.1	Pass	399	Pass
Pcon_c2=	17.6	watts	17.6	17.6	17.6	7	Pass	22.7	Pass
Icon_c2=	341	mA	341	341	341	122.8	Pass	399	Pass
Pcon c3=	18.2	watts	18.2	18.2	18.2	15.4	Pass	22.7	Pass
Icon c3=	353	mA	353	353	353	270.2	Pass	399	Pass
Test: pwron maxi									
	97.8	mA	97.8	97.8	97.8	0	Pass	1750	Pass
Ilim Min 1=	401.5	mA	401.5	401.5	401.5	400	Pass	1750	Pass
Tlim 1=	62.1	msec	62.1	62.1	62.1	50	Pass	9999	Pass
Vlim 1=	51.3	V	51.3	51.3	51.3	50	Pass	57	Pass
Ilim Max 1=	98.8	mA	98.8	98.8	98.8	0	Pass	1750	Pass
Ilim Low V Tol 1=	59.4	msec	59.4	59.4	59.4	50	Pass	9999	Pass
Ktran lo 1=	102.6	%	102.6	102.6	102.6	92.4	Pass	115	Pass
Test: pwron overld									
%Ipeak 1=	125	%	125	125	125	100	Pass	125	Pass
Vport Ipeak 1=	51.5	V	51.5	51.5	51.5	50	Pass	57	Pass
Vport 5%DC 1=	51.5	V	51.5	51.5	51.5	50	Pass	57	Pass
Test: mps dc valid									
Min Valid Time Tmps=	50	msec	50	50	50	1	Pass	60	Pass
Duty Cycle tol=	1	****	1	1	1	1	Pass	1	Pass
Test: mps dc pwrdn									
Min Valid I hold=	5	mA	5	5	5	5	Pass	10	Pass
Time-to-Shutdown Tmpdo=	365	msec	365	365	365	300	Pass	400	Pass
Max_Voltage_Vopen_max=	19.9	volts	19.9	19.9	19.9	-1	Pass	30	Pass
Test: pwrdn overld	10.0	Volto	10.0	10.0	10.0		1 400		1 400
Icut 1=	373.3	mA	373.3	373.3	373.3	-1	Pass	683	Pass
Tcut 1=	62.6	msec	62.6	62.6	62.6	50	Pass	9999	Pass
Isoft 1=	-1	mA	-1	-1	-1	-1	Pass	683	Pass
Tsoft 1=	-1	msec	-1	-1	-1	-1	Pass	2000	Pass
	-1	TISEC	- 1	-1	-1	-1	F 855	2000	F 855
Test: pwrdn_time Turn-Off Time Toff=	16.5	mSec	16.5	16.5	16.5	0	Pass	500	Pass
	0.0708	uF	0.0708	0.0708	0.0708	-1	Pass	0.52	Pass
Output_Cap_Cout=							_		
Output Load Rp=	111.7	Kohm	111.7	111.7	111.7	45	Pass	50000	Pass
Test: pwrdn_v							Design	0.0	Dress
Avg_Idle_Voff=	0.1	VDC	0.1	0.1	0.1	0	Pass	2.8	Pass
Error_Delay_Ted=	1390.6	msec	1390.6	1390.6	1390.6	750	Pass	10000	Pass
Peak_Error_Delay_Ved=	0.4	VDC	0.4	0.4	0.4	0	Pass	20.5	Pass

References

1. Data Sheet: TPS23861 IEEE 802.3at Quad Port Power-over-Ethernet PSE Controller (SLUSBX9A)

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ("TI") reference designs are solely intended to assist designers ("Buyers") who are developing systems that incorporate TI semiconductor products (also referred to herein as "components"). Buyer understands and agrees that Buyer remains responsible for using its independent analysis, evaluation and judgment in designing Buyer's systems and products.

TI reference designs have been created using standard laboratory conditions and engineering practices. **TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.** TI may make corrections, enhancements, improvements and other changes to its reference designs.

Buyers are authorized to use TI reference designs with the TI component(s) identified in each particular reference design and to modify the reference design in the development of their end products. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY THIRD PARTY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT, IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS ARE PROVIDED "AS IS". TI MAKES NO WARRANTIES OR REPRESENTATIONS WITH REGARD TO THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, EXPRESS, IMPLIED OR STATUTORY, INCLUDING ACCURACY OR COMPLETENESS. TI DISCLAIMS ANY WARRANTY OF TITLE AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, QUIET ENJOYMENT, QUIET POSSESSION, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS WITH REGARD TO TI REFERENCE DESIGNS OR USE THEREOF. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY BUYERS AGAINST ANY THIRD PARTY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON A COMBINATION OF COMPONENTS PROVIDED IN A TI REFERENCE DESIGN. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, SPECIAL, INCIDENTAL, CONSEQUENTIAL OR INDIRECT DAMAGES, HOWEVER CAUSED, ON ANY THEORY OF LIABILITY AND WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES, ARISING IN ANY WAY OUT OF TI REFERENCE DESIGNS OR BUYER'S USE OF TI REFERENCE DESIGNS.

TI reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques for TI components are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

Reproduction of significant portions of TI information in TI data books, data sheets or reference designs is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards that anticipate dangerous failures, monitor failures and their consequences, lessen the likelihood of dangerous failures and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in Buyer's safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed an agreement specifically governing such use.

Only those TI components that TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components that have **not** been so designated is solely at Buyer's risk, and Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2015, Texas Instruments Incorporated