
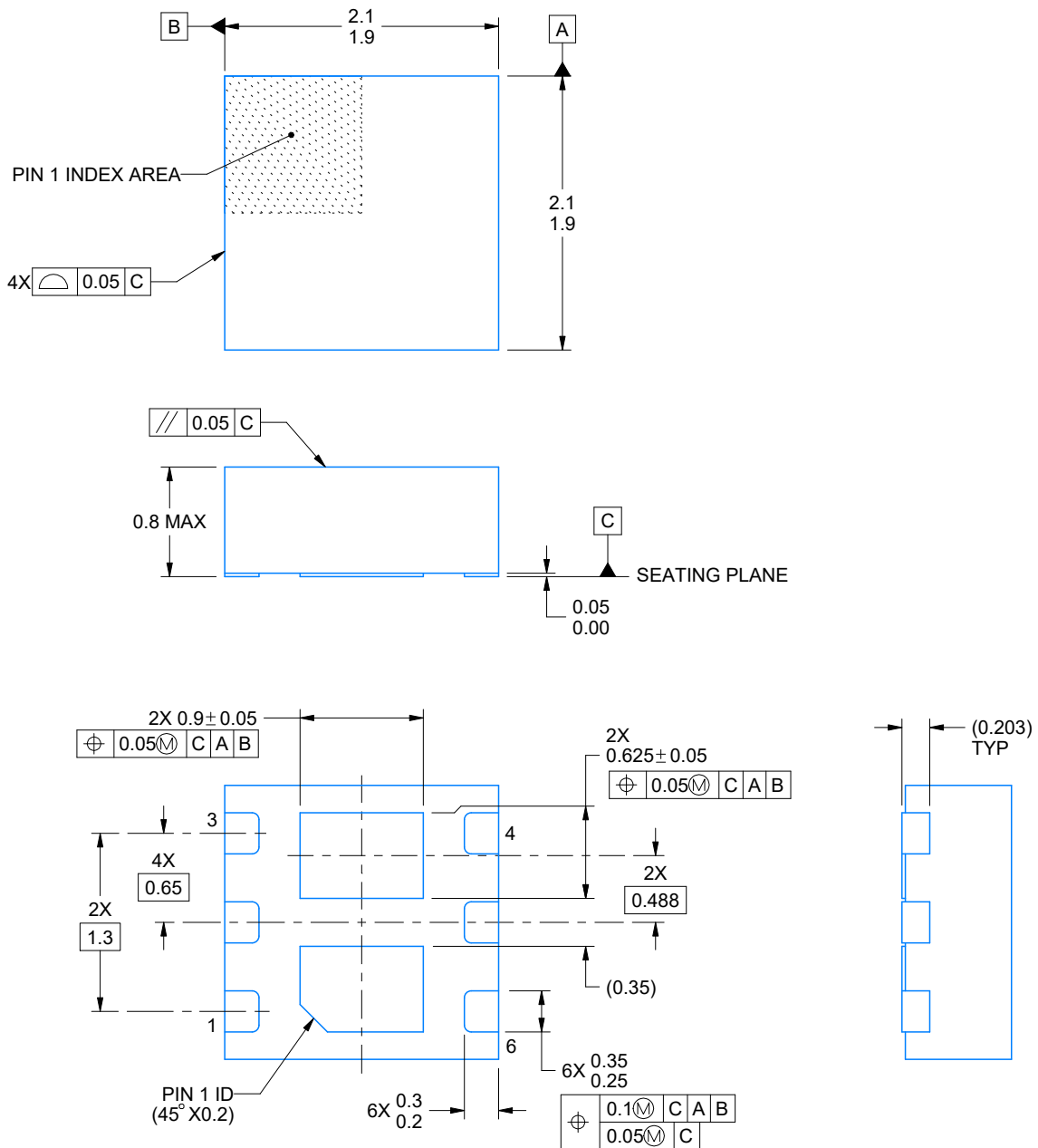
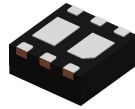


DATA BOOK PACKAGE OUTLINE

DRAFTER:	K. SINCERBOX	DATE:	04/08/2024	DIMENSIONS IN MILLIMETERS	
DESIGNER:		DATE:		 TEXAS INSTRUMENTS <small>SEMICONDUCTOR OPERATIONS</small>	CODE IDENTITY NUMBER
CHECKER:	K. SINCERBOX	DATE:	04/08/2024		01295
ENGINEER:	C. BULL	DATE:	04/08/2024	ePOD, DLV0006A / WSON, 6 PIN, 0.65 MM PITCH	
APPROVED:	K. SINCERBOX	DATE:	04/08/2024		
RELEASED:	K. SINCERBOX	DATE:	04/08/2024		
TEMPLATE INFO:		DATE:		SCALE	SIZE
	EDGE# 4218519		04/07/2016	NTS	A
				4230664	REV
				A	PAGE
					1 OF 5



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NOTES:

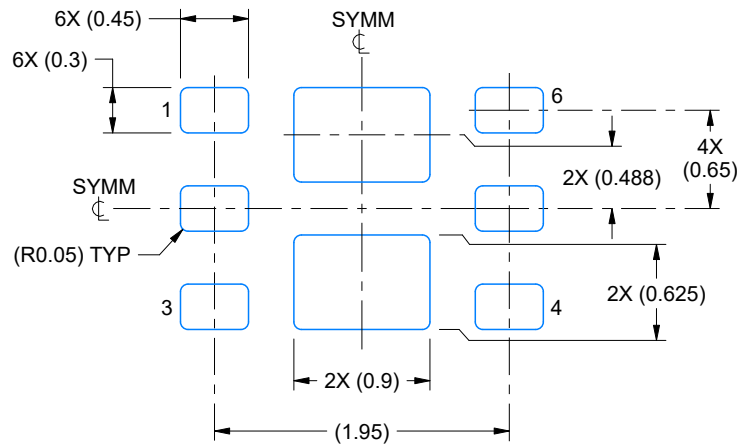
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

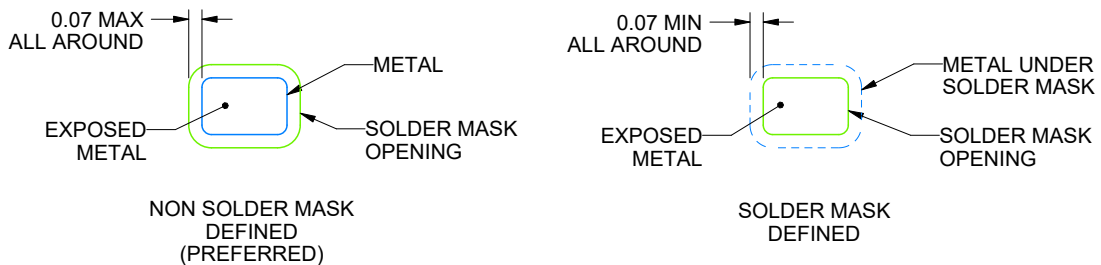
DLV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

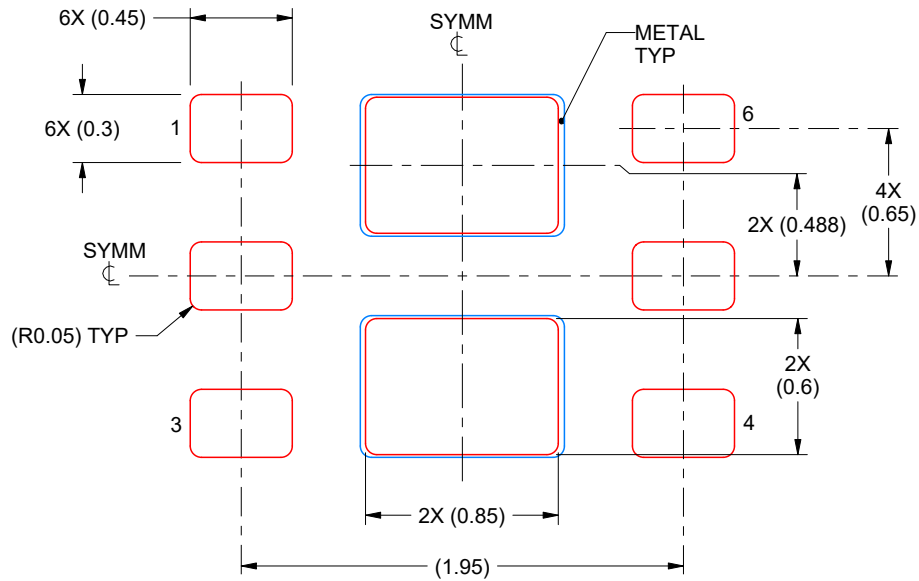
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DLV0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
EXPOSED PAD
90% PRINTED SOLDER COVERAGE BY AREA
SCALE:30X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2208157	04/08/2024	C. BULL / K. SINCERBOX