Upper side mosfet as target

1. Setup

   PWM signal from waveform generator and send into pin1, let pin2 shorted to low-voltage GND. Shorted lower mosfet with 180uH inductor.

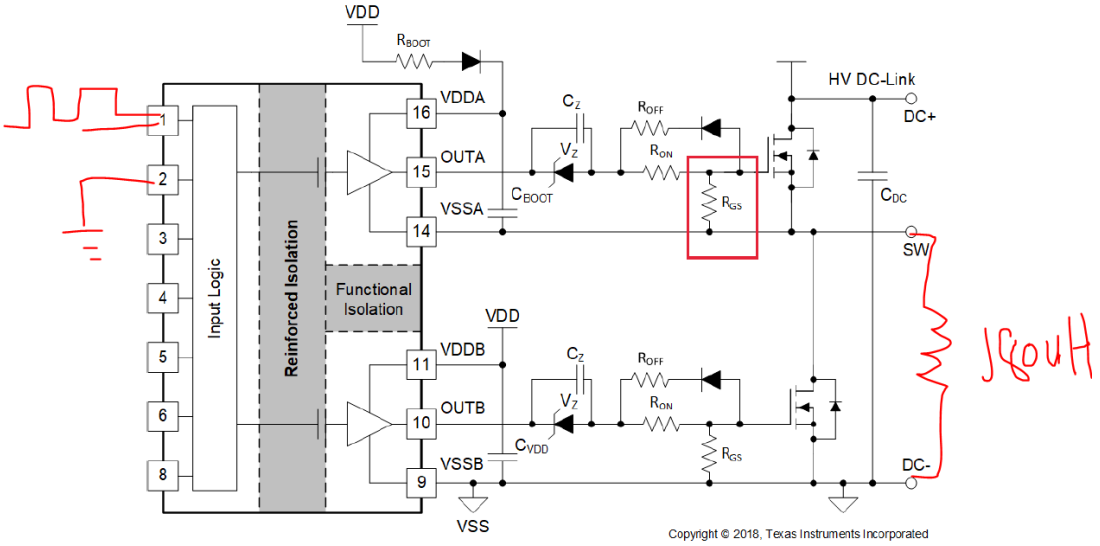
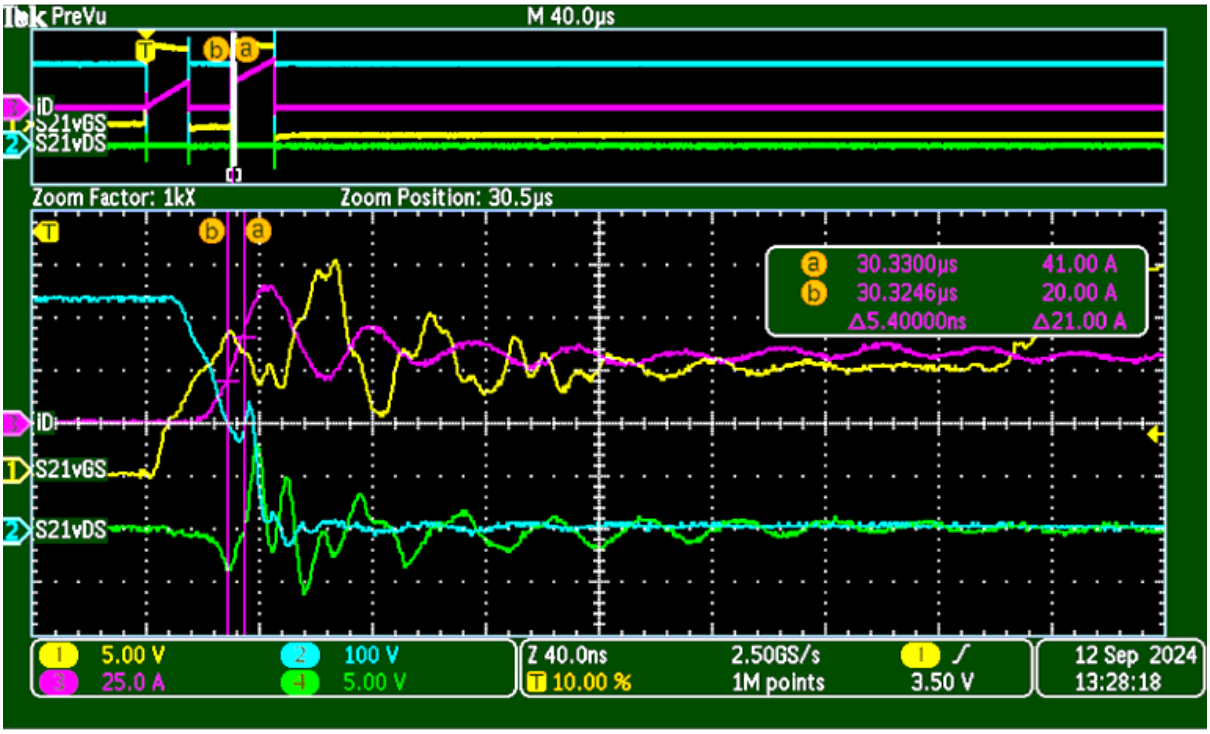


图 41. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

2. Results

   You can refer to the figure below. Ch1 is top side mosfet vGS, ch2 is vDS, ch3 is iD and ch4 is complementary lower mosfet vGS.

   You can see the lower vGS has no negative bias.



Lower side mosfet as target

1. Setup

   PWM signal from waveform generator and send into pin2, let pin1 shorted to low-voltage GND. Shorted upper mosfet with 180uH inductor.

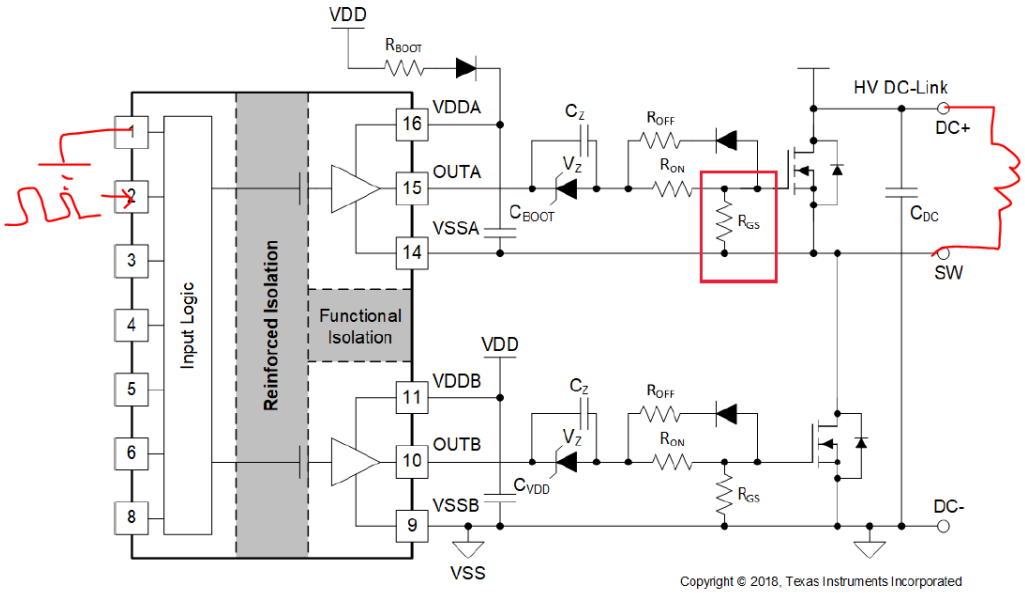


图 41. Negative Bias with Single Power Supply and Zener Diode in Gate Drive Path

2. Results

You can refer to the figure below. Ch1 is lower side mosfet vGS, ch2 is vDS, ch3 is iD and ch4 is complementary upper mosfet vGS.

You can see the upper side vGS has a negative bias(approximately -2.5V).