Date	Rev		History
1/6/2021	0.11	BMc	PDN Diag updates: 1. Add PMIC PNs with definitions, “Features Supported” list & update Notes 2. Discrete Ld Sw enabled with digital SOC_PWR_EN signal used to provide an “always ON” VIO_IN_3V3 supply to both PMIC VIO_IN inputs 3. Primary PMIC PG2.0 GPIO 3 & 9 mapping optimizations provides: A. Dual & independent Error Signal Monitoring (ESM) of both SOC & MCU safety error signals can now be supported by GPIOs #3 & #7 as originally intended and desired for some ASIL-D systems. This is now possible since GPIO_9 has been returned for PDN system use & now can support MCU +3.3V VIO load switch control (EN_VDD_MCUIO_3V3) instead of GPIO_3. B. A common Leo PMIC PN can now be defined for use in both TDA4VM recommended 3-Ph Dual Leo & Leo+Hera PDNs
V0.12	1/11/2021	BMc	PDN Diag updates: 1. Revert PMIC-A, GPIO_4 net name from “H_WAKE_PMIC” to “CAN_WKUP” that aligns with original EVM SoM net name & function.
V0.13	1/25/2021	BMc	PDN Diag updates: 1. Changed PDN identifier from “-0B” to “-0C” based upon the change to GPIO mapping that drives new PMIC NVM/PN. 2. Changed Primary Leo PMIC PN from “1212” to “1213" Pwr Seq updates: 1. Alternate VDD_MCUIO_1V8 ramp-up & down allowed steps to align with Main 1.8V Digital IO resulting in common PMIC PN for Prim Leo in J7ES Dual Leo & Leo+Hera PDNs
V0.14	1/27/2021	BMc	PDN Diag updates: 1. Added example of VDD_IO_3V3 OV/UV monitoring by SoC’s VMON_IR_VEXT input connection option to voltage buffer & voltage R-div needed to interface with SoC’s internal R-div network optimized for monitoring 1.8V power rails. Similar VMON interface circuitry used on J7VCL EVM. 2. Added 2x ext voltage monitoring inputs options for OV/UV monitoring by Hera PMIC of any safety critical system power rails. Hera’s quadbuck config can reassign remote sense feedback inputs (FB3 & FB4) for power rail monitoring.
V0.15	2/4/2021	BMc	During review of new Leo PN common for both Dual Leo PDN-0C & Leo+Hera PDN-1A for PMIC PG2.0 following updates were captured. PDN Diag updates: 1. Updated notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b. Pwr Seqs: 1. Updated title per approval of PDN-0C 2. Add alternate ramp-up & down steps approved to align VDD_MCUIO_1V8 & VDD_IO_1V8 to enable common PMIC PN for Prim Leo in J7ES Dual Leo PDN-0C & Leo + Hera PDNs. Previous PDN-0B seq up & down steps shown in “Gray-color” as original locations & still valid. 3. Change PMIC-A GPIO_9 to EN_MCUIO_LDSW control signal per PG2.0 optimz updates for common PN 4. Change PMIC-B GPIO_3 signal name to align with common name (EN_VDDR) across all PDNs
V0.16	3/2/2021	BMc	PDN Diag updates: 1. Removing discrete load switch from supplying PMIC’s VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related “Note #2” has been removed.
V0.17	3/9/2021	BMc	PDN Diag updates: 1. Reconnected Leo PMIC-A’s VINTLDO output to Leo PMIC-B’s enable input pin to ensure proper operation if Leo PMIC ever enters into lowest LP_STANDBY state.
V0.18	4/12/2021	BMc	PDN Diag update: 1. Corrected H_MCU_nINT_3V3 pull-up R to be connected to VDD_MCUIO_3V3 power rail that supplies J7 SoC’s GPIO domain used for MCU_nINT interface.

DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C

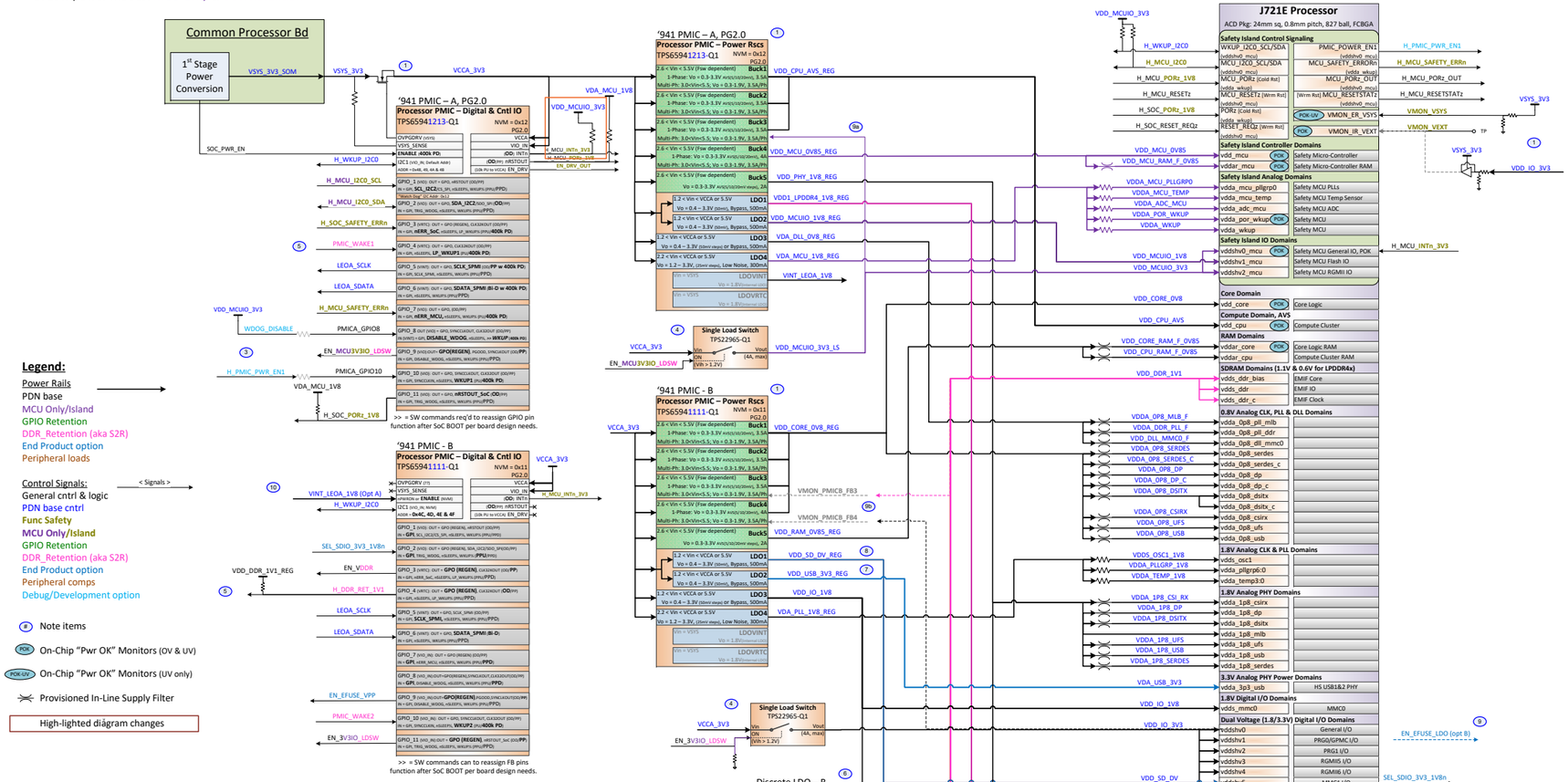
(Power Rail & GPIO Mapping Overview)

Leo PMIC-A, PN TPS6594**1213**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **13,** PG2.0)
Leo PMIC-B, PN TPS6594**1111**RWERQ1 (TI PN ID = 1, MP Buck Rails = 2, NVM ID = **12,** PG2.0)

Features Supported (EVM Max Features):

1. SoC performance: Max 2.0GHz clock with SERDES interfaces operational
2. Functional Safety: ASIL-D capable system with independent MCU & Main power for FFI
3. SDRAM: 32Gb, 4-Die, 32b, 4266MTs, LPDDR4 mode
4. Boot & Mass Flash: Octal SPI or Hyperflash (SR1.1 only) & eMMC, UFS
5. Low power modes: MCU Only & DDR Retention
6. Signaling Levels: MCU & Main Dual VIO
7. End Product Options:
   a. Compliant high-speed SD Card
   b. Compliant USB 2.0 data eye
   c. HS SoC Efuse programming on-board

V0.15	2/13/2021	Following final PMIC NVM review for defining new common PN ("1213") for Leo PG2.0 used in PDN-0C & -1A: 1. Update notes 2. Changed PMIC-A FB3 VMON input to be connected to VCCA_3V3 since VDD_MCUIO_3V3 rail is not supported, see note 9a. 3. Added PMIC-B FB3 & FB4 assignment for VMON by SW after SoC boot for ext power rail monitoring options, see note 9b.
V0.16	3/2/2021	1. Removing discrete load switch from supplying PMIC's VIO_IN since PG2.0 PMICs validation testing confirms no excessive glitches on GPIO or reset signals during of NVM initialization. Related "Note #2" has been removed.
V0.17	3/9/2021	1. Reconnected Leo PMIC-A's VINTLDO output to Leo PMIC-B's enable input pin to ensure proper operation if Leo PMIC ever enters into lowest LP_STANDBY state.
V0.18	4/12/2021	1. Corrected H_MCU_nINT_3V3 pull-up R to be connected to VDD_MCUIO_3V3 power rail that supplies J7 SoC's GPIO domain used for MCU_nINT interface.



Notes:
1) Functional Safety requires monitoring all "safety critical" power rails, including key SoC voltage domains, that could cause severe system failures. This classification depends on the use case and what SoC resources the customer is using that are considered to be safety-related. SoC has internal OV & UV monitoring for key SoC MCU & Main voltage domains. The status is reported by domain POK (POK) status bits. An optional buffer & R-div circuit can be connected to SoC's VMON_IN & EXT pin to extend OV/UV monitoring to VDD_IO_3V3 if desired. The following SoC Main & SDRAM domains are classified as non-critical & do not require direct monitoring: VDDSHV5 (SD Card), VPP_CORE, VPP_MCU, VDDA_3P3_USB & VDD1_LPDDR4_1V8.

3) Two optional development & debug control signals have been provisioned to interface to PMIC-A at GPIO_8 & _10 with NVM default functions set as DISABLE _WDOG & WKUP1.
   1. The DISABLE_WDOG (GPIO_8) input logic state is latched on rising edge of PMIC nRSTOUT = H_MCU_PORz_1V8 at end of power-up seq. A low signal enables normal watch dog timer operation while a high signal disables watch dog timer following a power up seq. This GPIO could be multiplexed & reassigned by SW if another signal is needed that is not required for SoC power sequencing.
   2. The WKUP1 (GPIO_10) input can be connected to SoC's PMIC_PWR_EN1 to enable emulator debug & control of PMIC power resources such as VDD_CORE to activate core logic needed in support of JTAG signaling across the device.
   If neither of these optional controls are needed, then alternative functions can be assigned after boot by system SW by overwriting NVM setting to recover GPIO_8 & _10.

4) Two external Load Switches (LdSw) have been used to create VDD_MCUIO_3V3 & VDD_IO_3V3 power rails from VCCA_3V3 to provide the following benefits:
   A) Sequencing SoC power domains in desired order by using PMIC GPIO control signals with desired start-up & shut-down timing delays per NVM settings.
   B) PMIC monitoring of "VCCA Over Voltage" (+5 to +10%) allows PMIC GPIOs to disconnect 3.3V power rails (VDD_MCUIO_3V3 & VDD_IO_3V3) from SoC if OV is detected.
   C) Enables DDR Retention & MCU Only low power states since VDD_MCUIO_3V3 & VDD_IO_3V3 rails must be disabled independently for 1 or both low power modes.

5) DDR Retention (aka S2R) function requires:
   A) PMIC-B's GPIO_4 configured for open-drain buffer type with Rpu to VDD_DDR_1V1 supply for SoC's DDR_RET input that is set high as part of entering DDR_RET mode.
   B) For LPDDR4 systems, all SoC EMIF & SDRAM DDR voltage domains remain energized while all other SoC MCU & Main domain supplies will be shut off to minimize power.
   C) PMIC-A's GPIO_4 must be set high as part of exiting DDR_RET mode and restoring processing operations.

6) SoC devices come in two types: General Purpose (GP) & High Security (HS). All GP devices can leave the VPP domains unconnected per DM. Pre-programmed HS devices can also leave VPP domains unconnected if no additional EFUSE programming is needed. If customer desires to on-board EFUSE programming, then an additional 1.8V, 100mA LDO is needed with a high impedance output when LDO is disabled. Recommended PNs: TPS73101-EP, fixed 1.8V TPS73118-Q1 or TLV70018-Q1. The EN_EFUSE_VPP control signal can be sourced from either a PMIC or SoC unused GPIO. Either approach will allow SoC SW to control Efuse VPP voltage level by enabling & disabling dedicated LDO as needed to program High Security SoC Efuses (see SoC DM for details).

7) PDN shows SoC's VDA_3P3_USB domain supplied from a low noise LDO as preferred for USB 2.0 data eye mask performance. If USB 2.0 I/F is not used or is only needed for development tasks, then the digital VDD_IO_3V3 rail can be connected as an alternate supply with an optional supply filter. Selecting digital VDD_IO_3V3 rail while supporting USB 2.0 I/F could negatively impact data eye performance due to higher supply noise causing data eye mask violations.

8) PDN shows SoC's Main VDDSHV5 domain supplied from a dual voltage LDO as preferred for compliant high-speed SD card operation. If SD card is not used or only standard data rate operation is sufficient, then the digital VDD_IO_3V3 rail can be connected as an alternate supply with an optional supply filter.

9a) PMIC-A, Buck3 unused remote sense feedback has been assigned by NVM to provide OV/UV VMON by default upon power-up for rail VDD_MCUIO_3V3. This VMON has been added to PMIC-A's "MCU power group" along with all PMIC-A MCU power resources for safe state transition in case of any errors. If VMON connection to VDD_MCUIO_3V3 is not desired, then VCCA_3V3 must be connected instead since a missing voltage will cause an error in MCU supply group resulting in immediate shutdown of all SoC supplies.
9b) PMIC-B, Buck3 & 4 have unused remote sense feedback inputs that can be assigned to provide OV & UV voltage monitoring after SoC SW boot for 2x external power rails per end product's desired functional safety needs. PDN diagram shows optional (dashed lines) OV/UV monitoring of VDD_DDR_1V1 & VDD_IO_3V3 power rails as examples.

10) Secondary Leo PMIC-B's ENABLE input pin should connect PMIC-A's VINTLDO output to ensure proper operation whenever Leo PMIC enters lowest power state of LP_STANDBY. Two optional enabling schemes are possible as follows:
1) Only if secondary Leo PMIC never enters lowest power state of LP_STANDBY, then same logic signal used to enable Leo-A can be used to enable Leo-B.
2) Only if the secondary PMIC is a Hera PMIC, then the PMIC dedicated SPMI comm bus can enable a Hera PMIC. This frees up Hera's GPIO_4 since it removes the need to assign the Enable function to Hera's GPIO_4 pin & connect PMIC-A's enable logic signal.

11) PMIC-A's GPIO_9 default setting is to provide "EN_MCUIO_LDSW" control signal but this Leo + Hera PDN does not need it. The same PMIC-A PN can be used for both Leo + Hera & Dual Leo PDNs and the NVM default setting is to support "EN_MCUIO_LDSW" signal since it is needed for load switch control during power sequencing in Dual Leo PDN-0B/C. It can be reassigned in Leo + Hera PDN only after SoC pwr up & SW boot can then overwrite with a new function. Any new signaling use/connection must not be negatively impacted due to default toggling of logic during power-up seq.

DRA829/TDA4VM 3-Phase Dual Leo2.0 PDN-0C Power Sequences

Leo PMIC-A, PN TPS6594**12**1**3**RWERQ1 (TI PN ID = **1**, MP Buck Rails = **2**, NVM ID = **13**, PG2.0)
Leo PMIC-B, PN TPS6594**11**1**1**RWERQ1 (TI PN ID = **1**, MP Buck Rails = **2**, NVM ID = **12**, PG2.0)

Date	Rev	By	Desc
1/25/2021	0.14	BMc	Add alternate ramp-up & down steps approved to align VDD_MCUIO_1V8 & VDD_IO_1V8 to enable common PMIC PN for Prim Leo in J7ES Dual Leo PDN-0C & Leo + Hera PDNs. Previous PDN-0B seq up & down steps shown in "Gray-color" as original locations & still valid.
2/4/2021	0.15	BMc	During new common PG2.0 Leo PN "1213" NVM settings review: Updated title per approval of PDN-0C Add alternate ramp-up & down steps approved for VDD_MCUIO_1V8, VDD_IO_1V8 and VDD_MCU_0V85 power rails to enable a common PMIC PN for primary Leo-A in J7ES Dual Leo PDN-0C & Leo + Hera PDN-1x. Original 2-Ph PDN-0A & 3-Ph PDN-0B power up & down step locations are shown in "Gray-color" since they are still valid. Change PMIC-A GPIO_9 to EN_MCU3V3IO_LDSW control signal per PG2.0 optimz updates for common PN Change PMIC-B GPIO_3 signal name to align with common name (EN_VDDR) across all PDNs

Legend:

System Time
Device Time
Board Power Rail – Active State / Control Signal Nets / SoC voltage domains
Board Power Rail – GPIO Retention / Control Signal Nets / SoC voltage domains
Board Power Rail – DDR Retention / Control Signal Nets / SoC voltage domains
Power Resource
NVM Settings, Pwr Rsc: (Resource, Current Capacity, Boot Voltage, Delay After Enable [us], Slew Rate [mV/us])
GPIO Rsc: (GPIO# = Function, Ref Voltage, Output Buffer Type, Logic @ T=0, Elapsed Time [us], Logic @ elapsed time)

 # Indicates signals &/or power rails that transition during power sequences

Verified per NVM file