5V High Efficiency Synchronous Buck PWM Controller

General Description

The RT8131B is a high efficiency single phase synchronous Buck DC-DC controller with 5V supply voltage.

The RT8131B has embedded MOSFET gate driver with high driving capability, supporting driving voltage up to 5V. This device uses lossless low-side MOSFET $R_{DS(ON)}$ current sense technique for over-current protection with adjustable threshold set by the LGATE pin (LGOCS). Other features include power good indication, enable/disable control and internal soft-start. The RT8131B also provides fault protection functions to protect the power stage output. With above functions, the IC provides customers a cost-effective solution for high efficiency power conversion. The RT8131B is available in the WDFN-10L 3x3 package.

Ordering Information

RT8131B □□

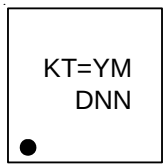
- Package Type
  QW : WDFN-10L 3x3 (W-Type)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Marking Information



KT= : Product Code

YMDNN : Date Code

Features

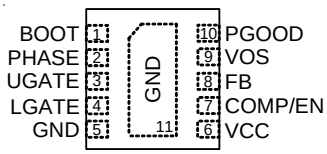
- **High Light Load Efficiency**
- **Single 5V Driver Voltage**
- **Integrated High Driving Capability N-MOSFET Gate Drivers**
- **300kHz Fixed Frequency Internal Oscillator**
- **88% Maximum PWM Duty Cycle**
- **Power Good Indicator**
- **Enable/Disable Control**
- **Internal Soft-Start**
- **Lossless Low-Side MOSFET $R_{DS(ON)}$ Current Sensing for Over-Current Fault Monitoring**
- **LGATE Over-Current Setting (LGOCS)**
- **OCP, UVP, OVP, OTP, UVLO**

Applications

- Motherboard, Memory/Chip-Set Power
- Graphic Card, GPU/Memory Core Power
- Low Voltage, High Current DC-DC Regulator

Pin Configuration

(TOP VIEW)

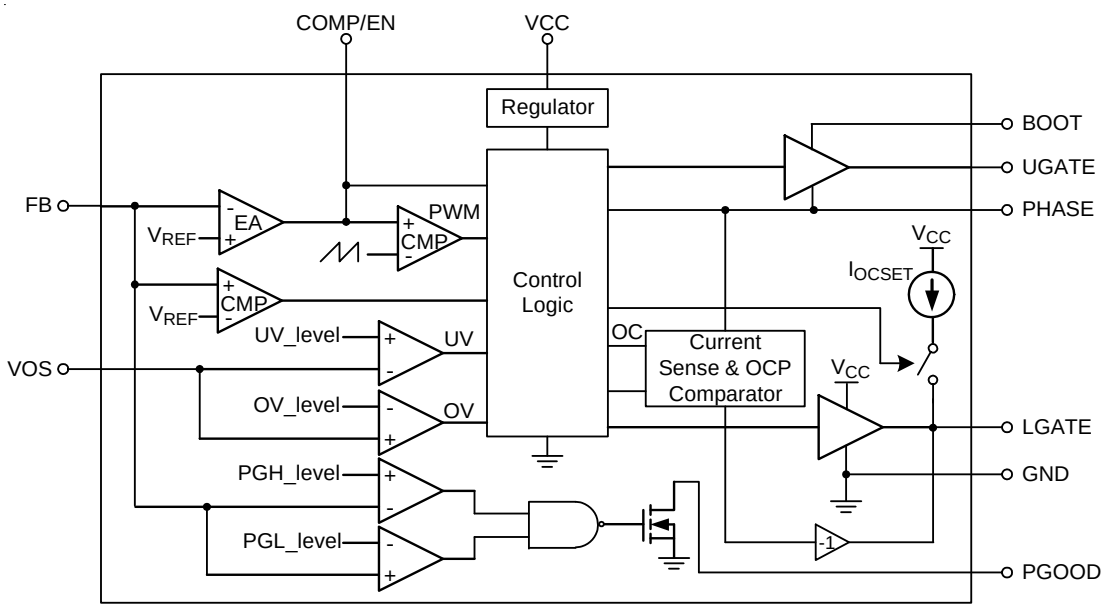


WDFN-10L 3x3

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	BOOT	Bootstrap supply for high-side gate driver. Connect this pin to a power source V_{CC} through a bootstrap diode, and connect a 0.1μF or greater ceramic capacitor from this pin to the PHASE pin to supply the power for high-side gate driver.
2	PHASE	Switch node. Connect this pin to the switching node of Buck converter. This pin is also the floating drive return of the high-side MOSFET gate driver.
3	UGATE	High-side MOSFET gate driver output. Connect this pin to the Gate of high-side MOSFET for floating drive.
4	LGATE	Low-side MOSFET gate driver output. Connect this pin to the Gate of low-side MOSFET. This pin is also used for Over-Current Protection (OCP) threshold setting. Connect a resistor (R_{OCSET}) from this pin to the GND pin to set the OCP threshold.
5, 11 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
6	VCC	Supply voltage input. It is recommended to connect a 1μF or greater ceramic capacitor from this pin to the GND pin. VCC also powers the low-side gate driver.
7	COMP/EN	Compensation node. Connect R-C network between this pin and the FB pin for PWM control loop compensation. This pin is also used for enable/disable control. Connect a small signal MOSFET to this pin to implement enable/disable control.
8	FB	Feedback voltage input. This pin is used for output voltage feedback input and it is also monitored for power good indication. Connect this pin to the converter output through voltage divider resistors for output voltage regulation.
9	VOS	Voltage of output feedback sense input. This pin monitors output over-voltage protection and under-voltage protection. Connect this pin to output through voltage divider resistors.
10	PGOOD	Power good indicator output. This pin provides an open-drain output. Connect this pin to a voltage source through a pull-up resistor. The PGOOD voltage goes high to indicate the output voltage is in regulation. This pin can be left open if the power good indication function is not used.

Functional Block Diagram



Operation

The RT8131B is a high efficiency single-phase synchronous Buck controller with integrated MOSFET driver. The controller has a fixed frequency control, a fixed frequency 300kHz oscillator is integrated to minimize external components.

Enable

The RT8131B remains in shutdown if the COMP/EN pin is lower than 0.3V (Max). When the COMP/EN pin rises above the enable trip point, the RT8131B will begin a soft-start cycle.

Over-Current Threshold Setting

Current limit threshold is externally programmed by adding a resistor (R_{OCSET}) between LGATE and GND. Once VCC exceeds the POR threshold, an internal current source I_{OC} flows through R_{OCSET}. The voltage across R_{OCSET} is stored as the current limit protection threshold. After that, the current source is switched off.

Under-Voltage Protection

If the VOS voltage is lower than the UVP threshold during normal operation, UVP will be triggered. When the UVP is triggered, both UGATE and LGATE go low until VCC is resupplied and exceeds the POR rising threshold voltage.

Over-Voltage Protection

If the VOS voltage is higher than the OVP threshold during normal operation, OVP will be triggered. When OVP is triggered, UGATE will go low and LGATE will go high until VCC is resupplied and exceeds the POR rising threshold voltage.

Absolute Maximum Ratings (Note 1)

- Supply Voltage, VCC ---------- –0.3V to 7V
- BOOT to PHASE
  - DC ---------- –0.3V to 7V
  - < 100ns ---------- –5V to 8.5V
- PGOOD ---------- –0.3V to 15V
- Input, Output or I/O Voltage ---------- –0.3V to 7V
- PHASE to GND
  - DC ---------- –0.3V to 30V
  - < 100ns ---------- –10V to 36V
- BOOT to GND
  - DC ---------- –0.3V to 37V
  - < 100ns ---------- –0.5V to 43V
- UGATE to GND
  - DC ---------- –0.3V to 37V
  - < 100ns ---------- –5V to 43V
- UGATE to PHASE
  - DC ---------- –0.3V to 7V
  - < 100ns ---------- –5V to 7V
- LGATE to GND
  - DC ---------- –0.3V to 7V
  - < 100ns ---------- –5V to 7V
- Power Dissipation, P_D @ T_A = 25°C (Note 2)
  - WDFN-10L 3x3 ---------- 3.27W
- Package Thermal Resistance
  - WDFN-10L 3x3, θ_{JA} ---------- 30.5°C/W
  - WDFN-10L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Power Input Voltage, VIN ---------- 5.5V to 26.5V
- Supply Input Voltage, VCC ---------- 4.5V to 6V
- Output Voltage Setting, VOUT ---------- 4.5V to 22V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{CC} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
General						
Supply Input Voltage	V_{CC}		4.5	5	6	V
VCC Supply Current	I_{CC}	No Load for UGATE/ LGATE	--	2	--	mA
VCC POR Threshold	V_{PORH}	V_{CC} rising	--	4.1	4.2	V
	V_{RORL}	V_{CC} falling	3.6	3.8	--	
VCC POR Hysteresis			--	0.3	--	V
Soft-Start Interval	t_{SS}	V_{FB} from 10% to 90%	--	17	--	ms
Reference Voltage	V_{REF}		0.793	0.8	0.807	V
Protection						
Thermal Shutdown Limit	T_{SD}		--	165	--	°C
Over-Voltage Threshold	V_{OVP}	Relative to VOS voltage	140	150	160	%
Under-Voltage Threshold	V_{UVP}	Relative to VOS voltage	40	50	60	%
OVP Propagation Delay	t_{OVP_DLY}		--	10	--	µs
UVP Propagation Delay	t_{UVP_DLY}		--	10	--	µs
OC Current Source	I_{OC}		9	10	11	µA
OC Preset Trigger Voltage	V_{OC_Preset}	R_{OCSET} is not populated	--	0.6	--	V
Over Current Setting Time Delay	t_{OCP}	From V_{CC} > 4.5V to Soft-Start	--	--	25	ms
MOSFET Gate Driver						
UGATE Drive Source	$I_{UGATEsr}$	V_{BOOT} – V_{PHASE} = 5V, Max Source current	--	1.5	--	A
LGATE Drive Source	$I_{LGATEsr}$	V_{LGATE} = 5V, max source current	--	1.5	--	A
UGATE Drive Sink	$R_{UGATEsk}$	V_{UGATE} – V_{PHASE} = 0.1V	--	1.8	--	Ω
LGATE Drive Sink	$R_{LGATEsk}$	V_{LGATE} = 0.1V	--	1.2	--	Ω
Dead Time	t_{DEAD}		--	30	--	ns
PWM Controller						
EA Open Loop Gain	G_{EA}	(Note 5)	--	80	--	dB
EA Bandwidth	BW	(Note 5)	--	15	--	MHz
Maximum Duty	D_{MAX}		--	88	--	%
Ramp Valley			--	0.9	--	V
Ramp Amplitude	ΔV_{OSC}	V_{IN} = 12V	--	0.7	--	V
COMP/EN Disable Threshold			--	--	0.3	V
PWM Frequency	f_{OSC}		270	300	330	kHz
PGOOD Threshold	V_{PGOOD_H}	Relative to FB voltage	0.86	0.89	0.92	V
	V_{PGOOD_L}	Relative to FB voltage	0.68	0.71	0.74	
PGOOD Low Level	V_{OL_PGOOD}	Sink current = 4mA	--	--	0.4	V
EN to Soft-Start Delay	t_{DELAY_EN}	(Note 5)	--	--	500	µs

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

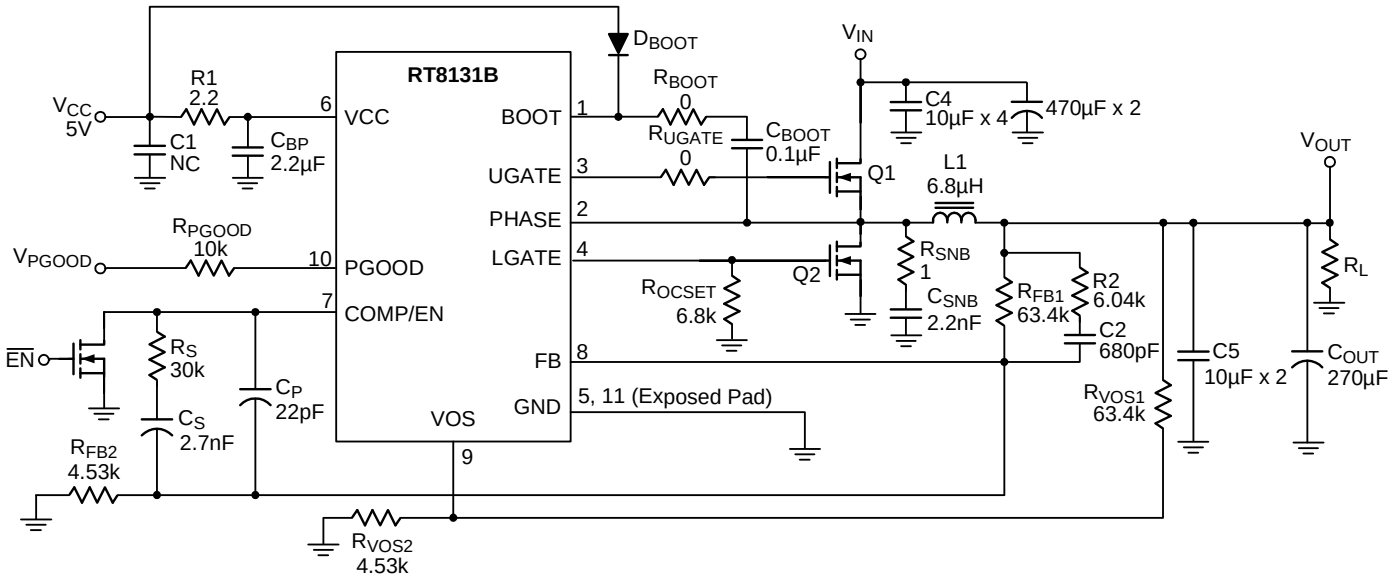
Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

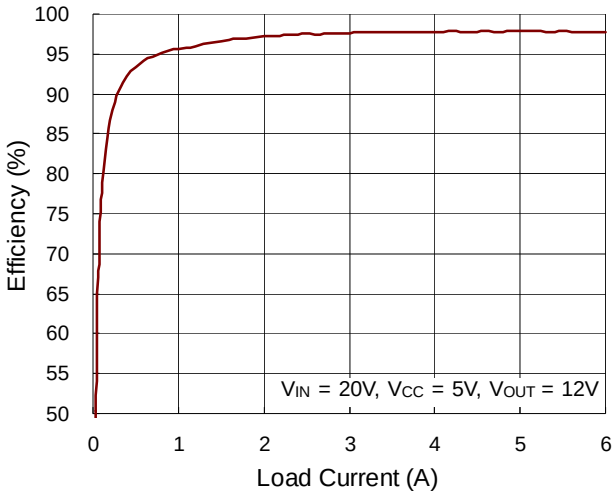
Note 5. Guaranteed by design.

Typical Application Circuit

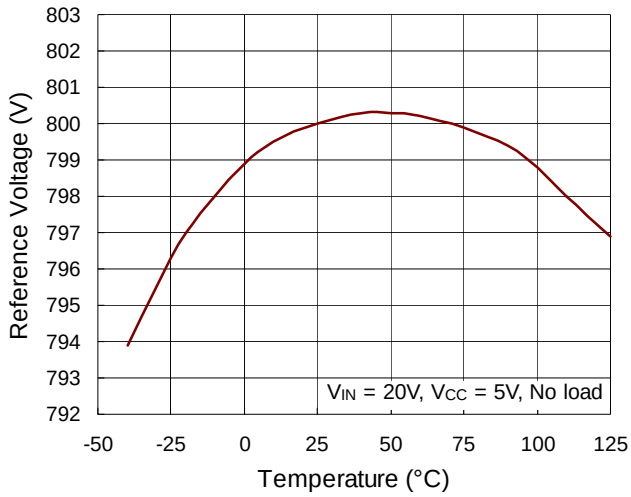


Typical Operating Characteristics

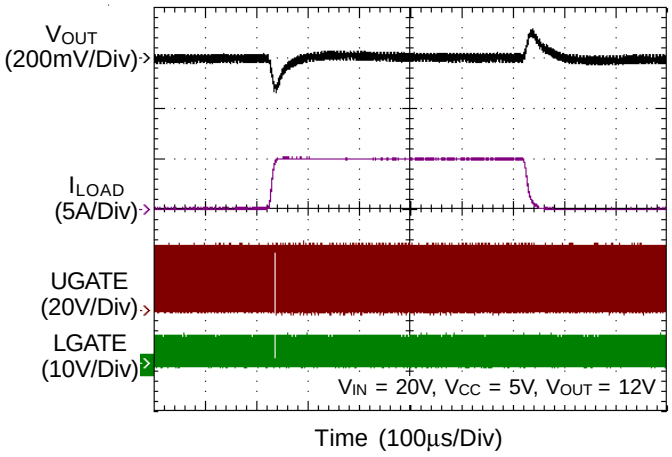
Efficiency vs. Load Current



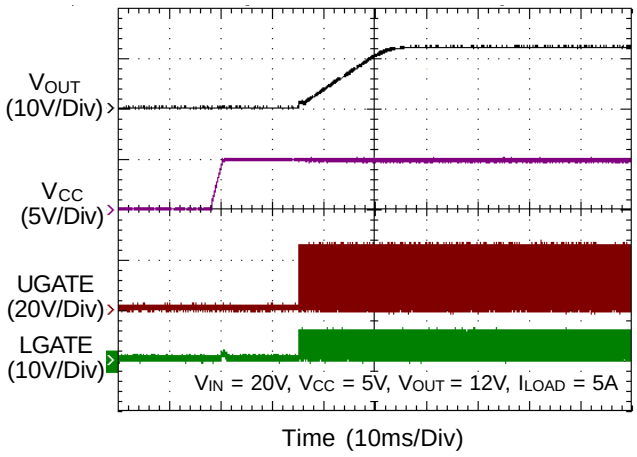
Reference Voltage vs. Temperature



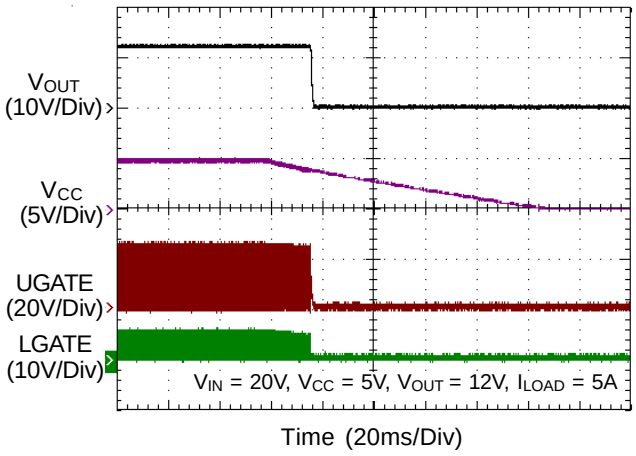
Load Transient Response



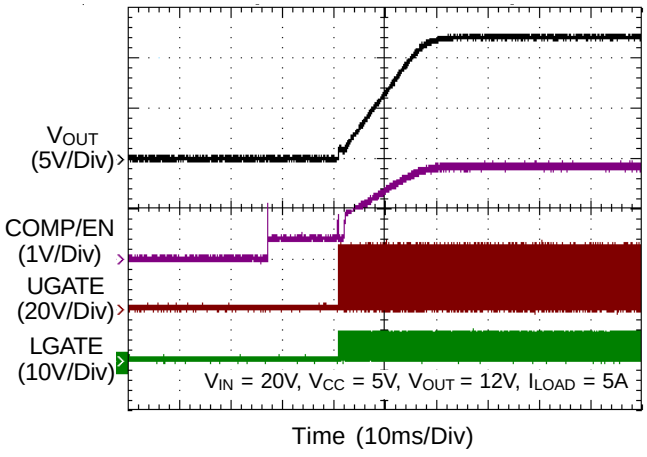
Power On from V_{CC}



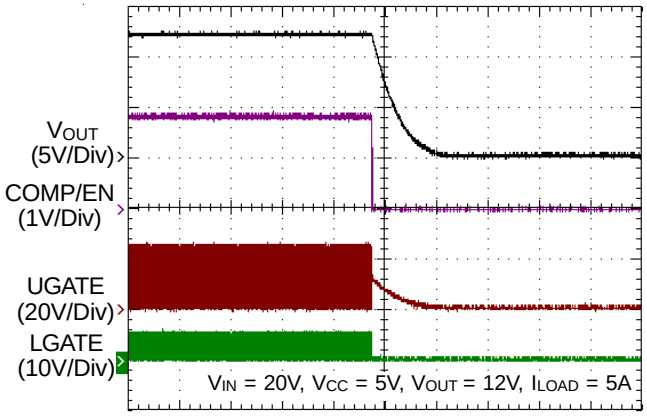
Power Off from V_{CC}



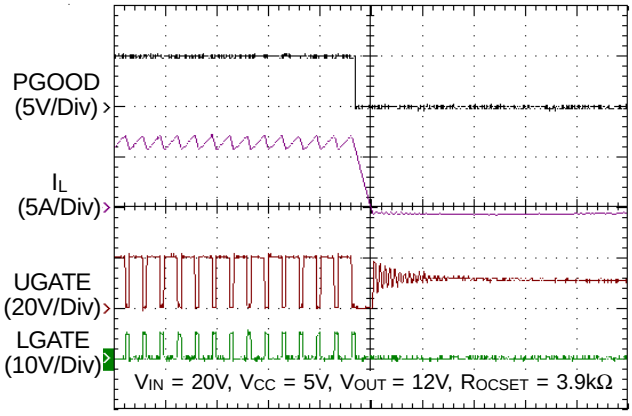
Power On from COMP/EN



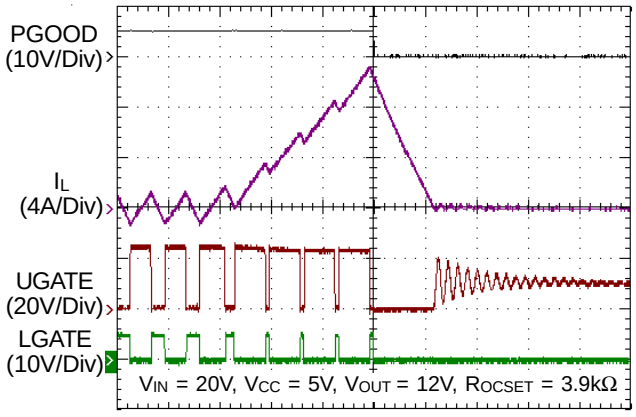
Power Off from COMP/EN



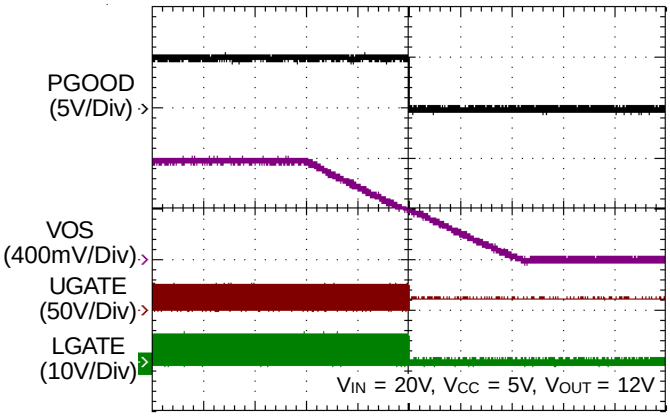
OCP



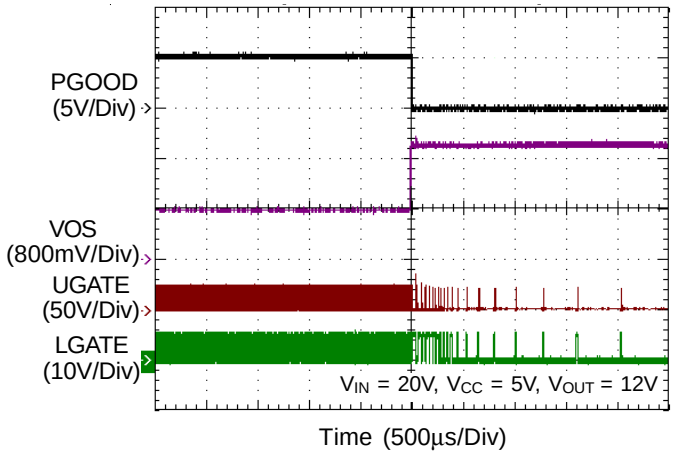
Short OCP



UVP



OVP



Application Information

Supply Voltage and Power-On Reset

The VCC pin is the power supply pin of the RT8131B. The input voltage range (V_{CC}) is from 4.5V to 6V with respect to the GND pin. An internal linear regulator regulates the supply voltage for internal control logic circuit. The VCC pin also supplies the power for the integrated low-side MOSFET gate driver. A 1µF ceramic capacitor or greater is recommended for the Vcc voltage de-coupling. Place the de-coupling capacitor physically close to the VCC pin.

The Power-On Reset (POR) circuit monitors the VCC pin voltage. If V_{CC} exceeds the POR rising threshold, the controller begins to work and prepares for soft-start operation. If V_{CC} falls below the POR falling threshold, the controller stops working. All MOSFETs stop switching, and all protections are reset. There is a hysteresis between the POR rising and falling thresholds to prevent inadvertently reset caused by noise.

Soft-Start

When the controller input voltage (V_{CC}) rises and exceeds the POR rising threshold at power up, the RT8131B initiates soft-start operation after the t_{OCP} time delay. The soft-start function is used to prevent large inrush current from input power source while converter is powered up. The IC provides soft-start function internally. The FB voltage will track the internal soft-start voltage, which ramps up from zero in a monotone during the soft-start period. Therefore, the duty cycle of PWM signal will increase gradually and so does the input current.

Figure 1 shows the power-up operation of the RT8131B.

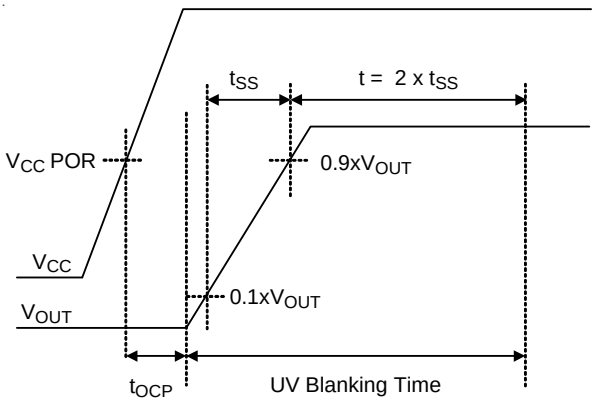


Figure 1. Power Up Operation

Power Up with Pre-Bias Voltage

Conventionally, when the converter output capacitor has been pre-charged to a non-zero positive voltage, the FB pin voltage of the PWM controller is non-zero. If the converter is powered up under this condition, the soft-start function of PWM controller will turn on low-side MOSFET with maximum duty ratio to rapidly discharge the output capacitor so as to force the FB voltage to track the internal soft-start voltage. Large current is then drawn from the output capacitor while the discharge is taking place. The discharge current depends on the inductance and the output capacitance. Output voltage may oscillate and go negative. The negative output voltage could damage the load.

The RT8131B implements control circuits specifically to prevent the negative voltage when the converter is powered up with pre-biased voltage on the output capacitor.

In order to prevent the high inrush current at power up beginning. The RT8131B control circuits specifically design the pre-biased power up circuit. And it only can be activated when V_{FB} < 0.1V.

Figure 2 shows the waveform that converter is powered up with pre-biased output voltage.

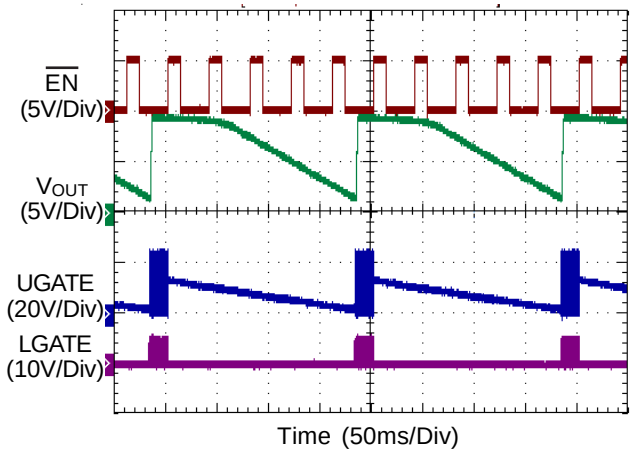


Figure 2. Power Up with Pre-biased Output Voltage

Enable/Disable Function

The COMP/EN pin is used to enable or to disable the controller. Because the COMP/EN pin is also the error amplifier output, it is recommended to use a small signal MOSFET with low capacitance C_{gd} to minimize the influence of the COMP/EN pin capacitance on loop response. Use a small signal MOSFET or BJT to implement the enable/disable control. Connect the Drain of small signal MOSFET (or the Collector of BJT) to the COMP/EN pin and its Source (or the Emitter of BJT) to ground for enable/disable control. If the COMP/EN voltage is pulled down below the enable level V_{EN}, the controller is disabled with both UGATE and LGATE go low after about 700ns delay time. If the COMP/EN pin is released, the COMP/EN voltage rises and then begins to soft-start. Since COMP/EN directly affects the behavior of voltage mode controller. Thus it should be pulled low as soon as possible during shutdown procedure, less than 0.3µs is recommended.

Power Good Indication

The RT8131B monitors the converter output voltage through the FB pin for power good indication. The PGOOD pin is an open-drain output, and it should be tied to a voltage source V_{PGOOD} no greater than 12V through a pull up resistor R_{PGOOD}. Referring to the typical application, it is recommended to choose the R_{PGOOD} to set maximum 1mA sink current into the PGOOD pin. If the FB pin voltage stays within the voltage window of ±11.25% of V_{REF} (typical), the PGOOD voltage will go high to indicate that the converter output voltage is in regulation. If the FB pin voltage is out of the voltage window, the PGOOD voltage goes low after about 10µs delay time to indicate that the converter output voltage is out of regulation. If the power good indication function is not used, the PGOOD pin can be left open.

Over-Voltage Protection (OVP)

If the VOS voltage is higher than the OVP threshold during normal operation, OVP will be triggered. When OVP is triggered, UGATE will go low and LGATE will go high to discharge the converter output capacitor to protect the load from over voltage condition. When the FB pin voltage falls below 0.1V, LGATE will go low to stop the discharge. The OVP function belongs to a latch protection. The RT8131B will not repeat the soft-start operation unless the VCC voltage is toggled off and on to reset the OVP.

Under-Voltage Protection (UVP)

If the VOS voltage is lower than the UVP threshold during normal operation, UVP will be triggered. When UVP is triggered, both UGATE and LGATE will go low to protect the load from under-voltage condition. Referring to Figure 1, the UVP function is not activated until three times soft-start time completes. The UVP function belongs to a latch protection, and it is masked during the period of three times soft-start time. The RT8131B will not repeat the soft-start operation unless the VCC voltage is toggled off and on to reset the UVP.

A power on sequence should be concerned. When VCC exceeds than POR threshold but VIN is not present, the UVP will be triggered. So, the VIN sequence should be earlier than VCC for successfully power up.

Over-Current Protection (OCP)

The RT8131B utilizes low-side MOSFET $R_{DS(ON)}$ current sense technique for over-current protection (OCP). After low-side MOSFET is turned on, the controller monitors the voltage across low-side MOSFET by sensing the PHASE voltage. The RT8131B uses cycle-by-cycle inductor valley current sense, the controller samples and holds the PHASE voltage before low-side MOSFET is turned off. This sampled PHASE voltage represents the inductor valley current, and it is compared with the user defined threshold voltage for OCP. When the inductor current exceeds the user defined threshold level for two consecutive PWM switching cycles, OCP will be triggered. When OCP is triggered, both UGATE and LGATE will go low to protect the load from over-current condition. The OCP function belongs to a latch protection. The IC will not repeat the soft-start operation unless the VCC voltage is toggled off and on to reset the OCP.

LGATE Over-Current Protection Threshold Setting (LGOCS)

The LGATE pin is not only for driving the low-side MOSFET, but also is used to set the over-current protection (OCP) threshold. Figure 3 shows the connection for OCP

threshold setting, in which a resistor R_{OCSET} connected from the LGATE pin to the GND pin sets the OCP threshold.

After the controller input voltage VCC exceeds the POR rising threshold at power up, the IC waits for a period of time for OCP setting before soft-start operation begins. During this period, the UGATE output is low and the LGATE output is in tri-state. An internal current source I_{OCSET} is switched on and then flows out of the LGATE pin to the external resistor R_{OCSET} to set the OCP threshold. The voltage drop across R_{OCSET} is stored by the controller as the OCP threshold V_{OCSET}. After that, the current source is switched off, and the LGATE output leaves tri-state then goes low. The resistance value of R_{OCSET} is determined by the following equation :

$$R_{OCSET} = \frac{V_{OCSET}}{I_{OCSET}} = \frac{R_{DS(ON)} \times I_{MAX}}{I_{OCSET}}$$

where I_{MAX} represents the maximum inductor valley current, $R_{DS(ON)}$ is the on state channel resistance of the low-side MOSFET.

If the R_{OCSET} is not connected, the internal current source I_{OCSET} will charge the C_{gs} of the low-side MOSFET during the OCP threshold setting period. Under this condition, the LGATE voltage may be high enough to turn on the low-side MOSFET so that the output capacitor is discharged. Although the LGATE voltage may be high enough to turn on the low-side MOSFET, the OCP threshold voltage is internally clamped at 600mV (typical) and stored as the preset value.

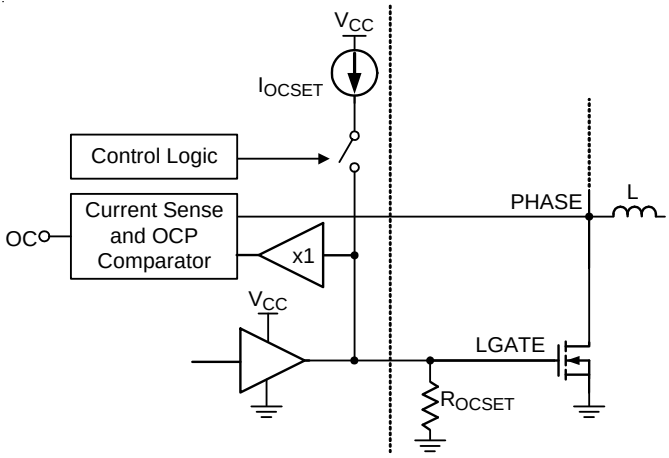


Figure 3. OCP Threshold Setting

Although the OCP threshold voltage is internally clamped at 600mV when R_{OCSET} is not connected, this preset threshold voltage may be very high to most of applications. Hence, it is recommended to keep the R_{OCSET} always well-connected to protect the converter from over-current condition.

Bootstrap Circuit

Figure 4 shows the bootstrap circuit, which is used for the high-side MOSFET driving. The C_{BOOT} is used to store and supply the energy for high-side MOSFET floating drive, and the D_{BOOT} is used for voltage blocking. Choose the D_{BOOT} with sufficient voltage rating to block the PHASE peak voltage (consider switching spike) plus the voltage V_{CC}.

When the low-side MOSFET is on, the PHASE voltage is pulled down to ground and the D_{BOOT} conducts to charge the C_{BOOT}. When the high-side MOSFET driver is on, part of the charge stored in the C_{BOOT} is transferred to the high-side MOSFET to turn it on. Use 0.1µF or greater ceramic capacitor as the C_{BOOT} to ensure the high-side MOSFET gate driver operation. The C_{BOOT} and D_{BOOT} should be placed physically close to the BOOT and PHASE pins to minimize the trace parasitic components.

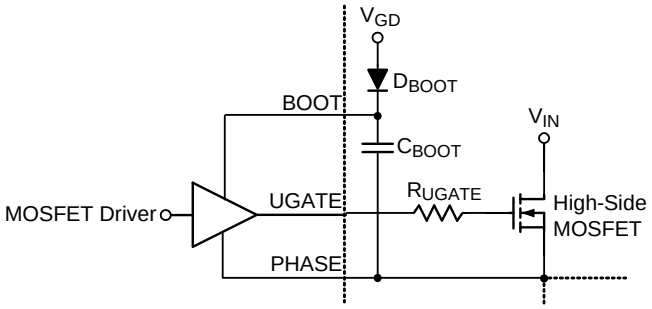


Figure 4. Bootstrap Circuit

MOSFET Gate Drivers

In synchronous rectified Buck topology, the dead-time is utilized to prevent cross conduction of high-side and low-side MOSFETs. The RT8131B implements non-overlapping MOSFET gate drivers with dead-time control scheme to ensure a safe operation of MOSFET switching.

For high output current applications, multiple power MOSFETs are usually paralleled to reduce the total $R_{DS(ON)}$. The MOSFET gate driver needs to have higher

driving capability to switch on/off these paralleled MOSFETs. The RT8131B integrates MOSFET gate drivers that have high current driving capability to have lower switching loss and thus better performance of conversion efficiency. The embedded MOSFET drivers contribute to the majority of power dissipation of the controller. Therefore, WDFN package is chosen because of its power dissipation rating. If gate resistor is not used, the power dissipation of the controller can be approximately calculated by the following equation :

$P_{SW} = f_{SW} (Q_{g\_High} \times V_{BOOT-PHASE} + Q_{g\_Low} \times V_{CC})$

where $V_{BOOT-PHASE}$ represents the voltage across the bootstrap capacitor.

It is important to make sure that the controller can dissipate the switching loss and have enough room for safe operation when power MOSFETs are paralleled.

Inductor Selection

Inductor plays an important role in step-down converters because the energy from the input power rail is stored in it and then released to the load. From the viewpoint of efficiency, the DC resistance (DCR) of inductor should be as small as possible to minimize the conduction loss. In addition, because inductor uses most of the board space, its size is also important. Low profile inductors can save board space especially when the height has limitation. However, low DCR and low profile inductors are usually cost ineffective.

Additionally, larger inductance results in lower ripple current, which means lower power loss. However, the inductor current rising time increases with inductance value. This means the transient response will be slower. Therefore, the inductor design is a trade-off between performance, size and cost.

In general, inductance is designed so that the ripple current ranges between 20% to 40% of full load current. The inductance can be calculated by the following equation :

$$L_{MIN} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times k \times I_{OUT\_FULL\ LOAD}} \times \frac{V_{OUT}}{V_{IN}},$$

where k is 0.2 to 0.4

Input Capacitor Selection

Voltage rating and current rating are the key parameters in selecting input capacitor. Generally, input capacitor has a voltage rating 1.5 times greater than the maximum input voltage is a conservatively safe design.

The input capacitor is used to supply the input RMS current, which can be approximately calculated by the following equation :

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The next step is to select proper capacitor for RMS current rating. Using more than one capacitor with low equivalent series resistance (ESR) in parallel to form a capacitor bank is a good design. Besides, placing ceramic capacitor close to the Drain of the high-side MOSFET is helpful for reducing the input voltage ripple at heavy load.

Output Capacitor Selection

The output capacitor and the inductor form a low-pass filter in the Buck topology. The electrolytic capacitor is used for this application because it can provide large capacitance value. In steady state condition, the output capacitor supplies only AC ripple current to the load, which means the output capacitor must be able to handle the inductor ripple current. The ripple current flows into/out of the capacitor results in ripple voltage, which can be determined by the following equation :

$\Delta V_{OUT\_ESR} = \Delta I_L \times ESR$

In addition, the output voltage ripple is also influenced by the switching frequency and the capacitance value.

$$\Delta V_{OUT\_C} = \Delta I_L \times \frac{1}{8 \times C_{OUT} \times f_{SW}}$$

Another parameter that has influence on the output voltage sag is the equivalent series inductance (ESL). The rapid change in load current results in di/dt during transient. Therefore, ESL contributes to part of the voltage sag. Using capacitors that have low ESL can obtain better transient performance. Generally, using several capacitors connected in parallel can have better transient performance than using single capacitor for the same total ESR.

Unlike the electrolytic capacitor, the ceramic capacitor has relative low ESR and can reduce the voltage deviation during load transient. However, the ceramic capacitor can only provide low capacitance value. Therefore, using a mixed combination of electrolytic capacitor and ceramic capacitor can also have better transient performance.

PWM Feedback Loop Compensation

In continuous conduction mode, the RT8131B operates with fixed frequency and uses voltage mode control for output voltage regulation. The IC utilizes voltage error amplifier with external compensation to provide flexibility in feedback loop compensator design. Figure 5 shows the voltage mode control loop of a Buck converter. The control loop consists of the modulator, power stage and the compensator.

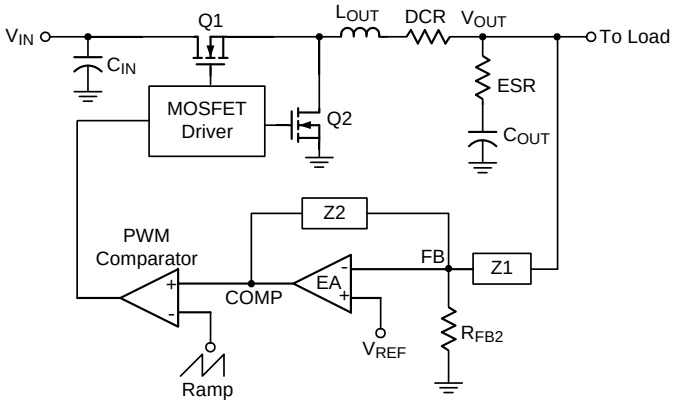


Figure 5. Voltage Mode Control Loop of Buck Converter

Output voltage of the converter is scaled by the divider resistors and then compared to the reference voltage, which is the regulation level seen by the controller. The error amplifier output voltage V_{COMP} is compared to the saw-tooth waveform from the oscillator to generate PWM signal. The output voltage is then regulated according to the duty cycle of the PWM signal.

The system open loop gain $\frac{\hat{V}_{OUT}}{\hat{V}_{COMP}}$ has two poles at f_{LC} and one zero at f_{ESR}. The frequency of f_{LC} and f_{ESR} can be calculated by the following expressions :

$$f_{LC} = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi \times C_{OUT} \times ESR}$$

In order to obtain an accurate output voltage regulation and fast transient response, a compensator is necessary. Depending on the inductor and output capacitor, different type of compensator can be used to finish the feedback loop compensation. By inserting a well designed compensator into the feedback loop, the closed loop control-to-output transfer function can be shaped to have adequate crossover frequency and sufficient phase margin.

The design goals are:

- Obtain high gain at low frequency for DC regulation accuracy
- Obtain sufficient bandwidth for transient performance (generally, 1/10 to 1/5 switching frequency)
- Obtain sufficient phase margin for stability (generally >45°)

Figure 6 shows the Type-III compensator, which is composed of voltage error amplifier, impedance network Z1 and Z2.

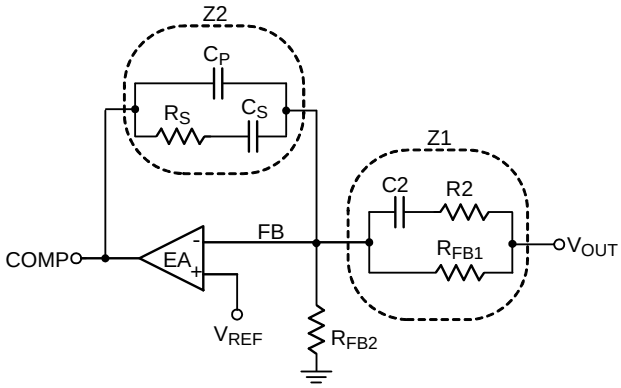


Figure 6. Type-III Compensator

The Type-III compensator introduces three poles and two zeros to the system. The first pole is located in low frequency to increase the DC gain for voltage regulation accuracy and is usually referred to as the pole at zero. The location of rest of the two poles and two zeros can be determined as follows :

$$f_{Z1} = \frac{1}{2\pi \times R_S \times C_S},\ f_{Z2} = \frac{1}{2\pi \times (R2 + R_{FB1}) \times C2}$$

$$f_{P1} = \frac{1}{2\pi \times R2 \times C2},\ f_{P2} = \frac{1}{2\pi \times R_S \times \left(\frac{C_S \times C_P}{C_S + C_P}\right)}$$

Figure 7 shows the system Bode plot. The close loop gain is the sum of modulation gain and the compensation gain. The modulation DC gain is determined by $V_{IN}/\Delta V_{OSC}$, where ΔV_{OSC} is peak to peak voltage of the saw-tooth ramp. In general, f_{Z1} is placed at half of f_{LC}, and f_{Z2} is placed at f_{LC} to boost the large phase lag created by the double pole especially when ESR is low. f_{P1} is typically placed at f_{ESR} to obtain a –20dB/dec slope at crossover frequency. f_{P2} is placed at half of the switching frequency to increase the attenuation in high frequency.

After calculating the compensation values, draw the system Bode plot to check the crossover frequency and phase margin. Due to the circuit parasitic components and the characteristic deviation in the inductor and output capacitors, further tuning of the compensation value to obtain the required crossover frequency and phase margin is necessary.

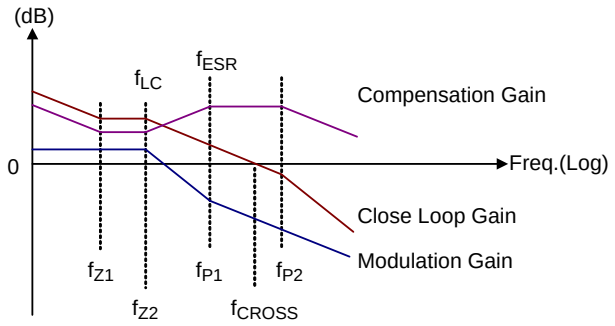


Figure 7. System Bode Plot

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WDFN-10L 3x3 package, the thermal resistance, θ_{JA}, is 30.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (30.5°C/W) = 3.27W for a WDFN-10L 3x3 package

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 8 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

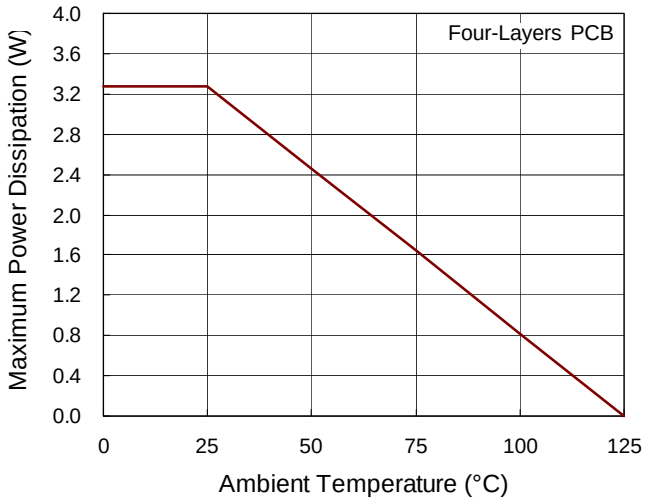


Figure 8. Derating Curve of Maximum Power Dissipation

Layout Considerations

PCB layout plays an important role in high current, high frequency switching converter design. The general layout guide line is listed as follows.

- Minimize the high-current loop as short as possible. The current transition between MOSFETs usually causes di/dt voltage spike and thus the EMI issue due to parasitic components on PCB trace and component lead. The PCB trace parasitic components cause not only excessive voltage spike, but also power loss. To reduce the PCB trace parasitic, place the high-side, low-side MOSFETs and the inductor with short current loop as possible.
- Connect the controller and power MOSFETs with wide width and short length PCB traces. Because the RT8131B has integrated high-current MOSFET gate drivers, the PCB trace for MOSFET driving should be sized to carry at least 2A peak current.
- For bootstrap circuit, place the bootstrap diode D_{BOOT} close to the BOOT pin, and place the bootstrap capacitor C_{BOOT} physically close to BOOT pin and PHASE pin with wide and short copper trace connection.
- Place the ceramic capacitor close to the VCC pin for noise de-coupling.
- Place all the function setting and compensation components as close to their associated pins as possible. This includes :
- Place the compensation components close to the VOS pin, FB pin and COMP pin to avoid noise pickup. Voltage divider resistors connected to the FB pin should be placed close to the controller.
- Place the OCP setting resistor R_{OCSET} close to the LGATE pin.
- Place the small-signal MOSFET or BJT used for enable/disable function close to the COMP pin.
- Place ceramic capacitor close to the drain of high-side MOSFET to decrease the input voltage ripple.
- The output voltage feedback trace should be away from the switching node, power MOSFETs and inductor to avoid noise pickup.
- Place the bulk capacitors close to the load.

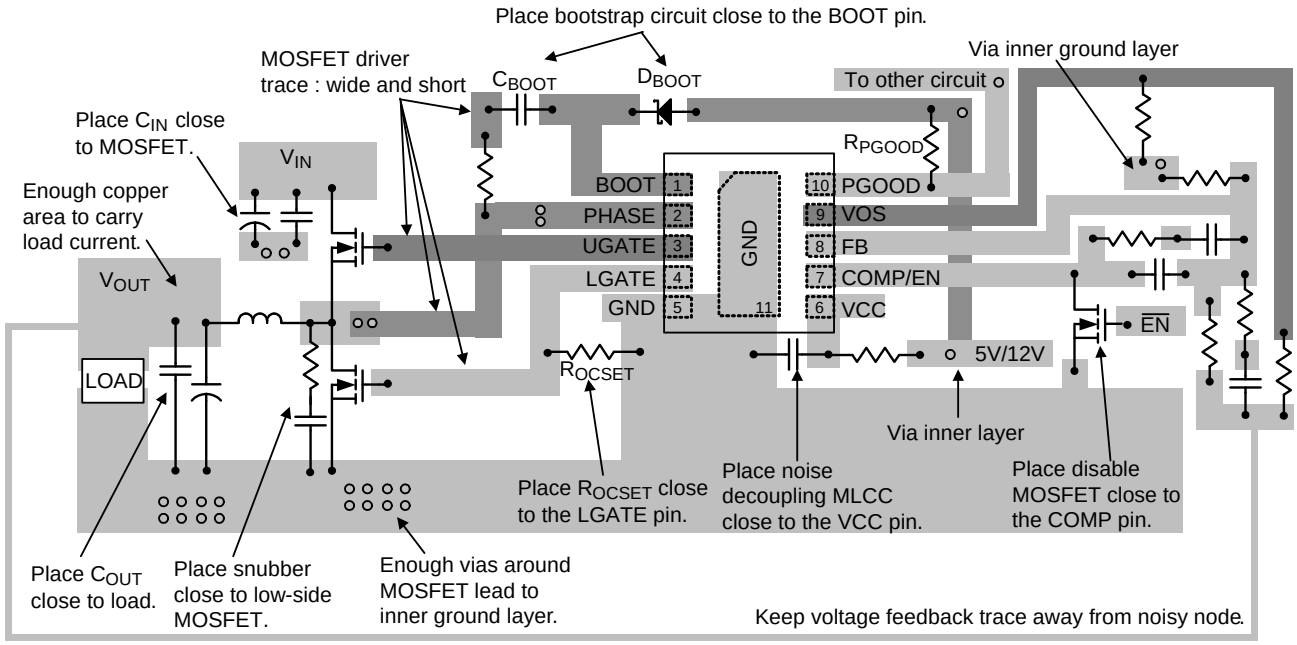
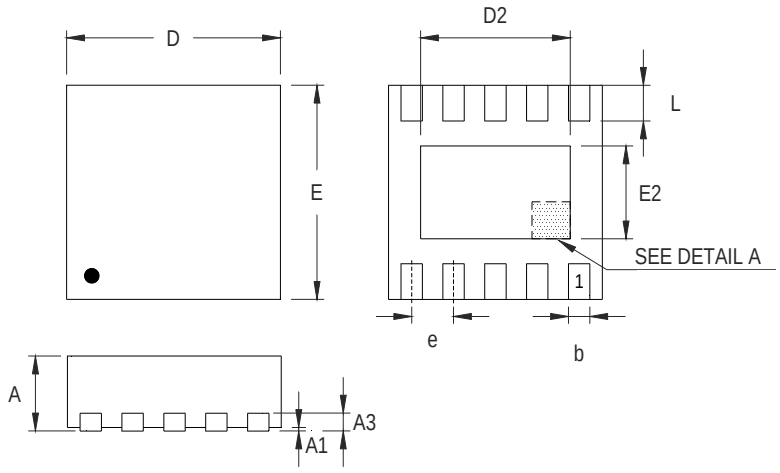
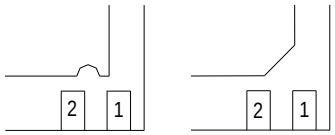


Figure 9. PCB Layout Guide

Outline Dimension





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	2.300	2.650	0.091	0.104
E	2.950	3.050	0.116	0.120
E2	1.500	1.750	0.059	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 10L DFN 3x3 Package

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