

Design Procedure for TPS54120

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Battery Power Applications

ABSTRACT

This application report details the design procedure of a low-noise, 1-A power supply with the integrated switcher and low-dropout (LDO) regulator of the TPS54120. The designer must know a few parameters in order to start the design process and typically determines them at the system level.

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1 Introduction

A design tool calculator for the TPS54120 is available in the TPS54120 product folder under the Tools & Software (SLVC411) on the TI Web site. The following application report provides a detailed explanation of the design procedure for a low-noise power supply.

The following known parameters apply to this example:

Table 1. Parameters

Parameters	Value
SW Output Voltage (SW VOUT)	4.1 V
LDO Output Voltage (VOUT)	3.3 V
Transient response at SW output	Δ SW Vout = 4%
Input voltage (Vin)	12 V nominal, 7 V to 17 V
Output Voltage Ripple at the SW output	1% (41 mVpp)
Start Input Voltage (Rising Vin)	6.806 V
Stop Input Voltage (Falling Vin)	4.824 V
Switching Frequency (fsw)	480 kHz
Output Current(Iout)	1 A

2 Typical Application Schematic

The application schematic (Figure 1) meets the Table 1 parameters. This circuit is available as the TPS54120EVM-103 evaluation module. The design procedure is given in this section. For more information about Type II and Type III frequency compensation circuits, see *Understanding Compensation Network for the TPS54120* (SLVA503).

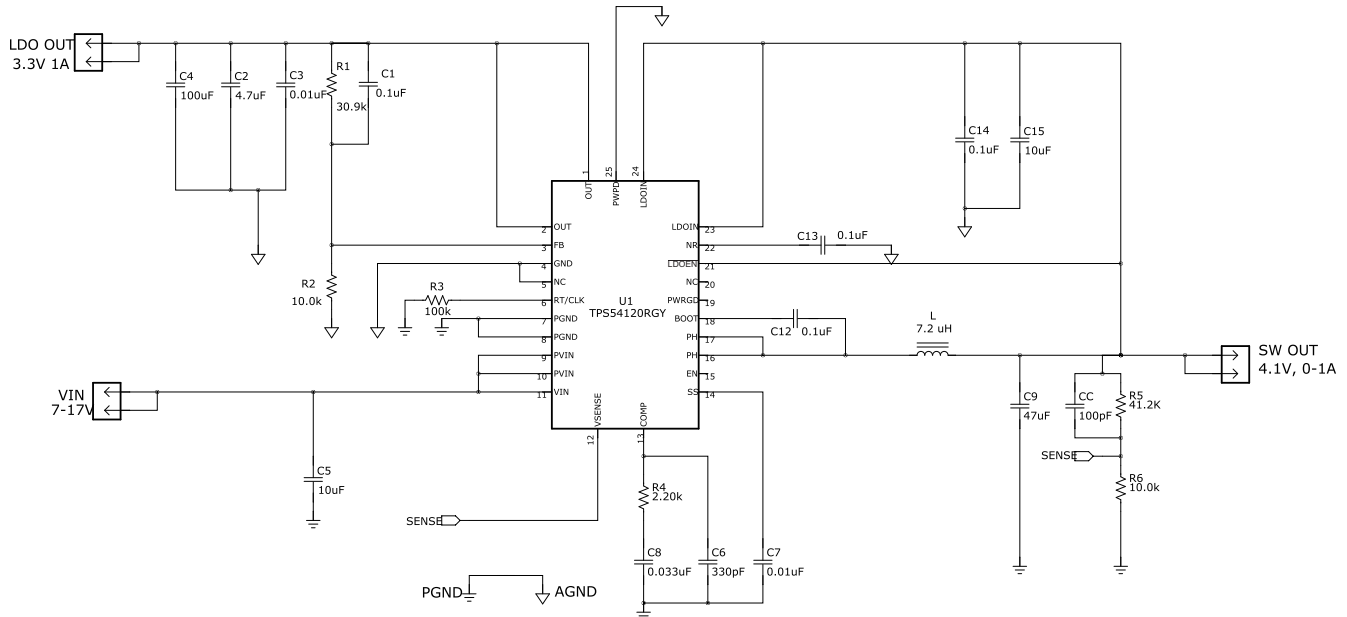


Figure 1. Typical Application Circuit

3 Operating Frequency

The first step is to decide on a switching frequency for the regulator, which involves a trade-off between higher and lower switching frequencies. Higher switching frequencies may produce a smaller solution size, using lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes additional switching losses, which negatively impact the converter's efficiency and thermal performance. In this design, the selection of a moderate switching frequency of 480 kHz achieves both a small solution size and a high-efficiency operation. Using the resistor at the RT/CLK pin (R3) sets this frequency.

$$R3 \text{ (k}\Omega\text{)} = 60281 \times f_{sw}(\text{kHz})^{-1.033} \quad (1)$$

Using Equation 1, the required resistance for a switching frequency of 480 kHz is 102 k Ω . This design uses a 100-k Ω resistor.

4 Inductor Selection

Equation 2 is a calculation of the value of the output inductor. KIND is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The output capacitor filters the inductor ripple current. Therefore, choosing a high inductor ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Typically, the designer selects the inductor ripple value; however, KIND is normally from 0.2 to 0.4 for the majority of applications.

$$L = \frac{V_{in \max} - SW V_{out}}{I_{out} \times K_{ind}} \times \frac{SW V_{out}}{V_{in \max} \times F_{sw}}$$

$$L = \frac{17 - 4.1}{1 \times 0.3} \times \frac{4.1}{17 \times 480,000} = 21.6 \mu\text{H} \quad (2)$$

For this design example, by using KIND = 0.3, the calculated inductor value is 21.6 μH . The chosen nearest standard value was 22 μH . For the output filter inductor, the RMS current and saturation current ratings must not be exceeded. Use Equation 3, Equation 4, and Equation 5 to find the inductor ripple current, RMS current, and peak inductor current.

$$I_{ripple} = \frac{V_{in \max} - SW V_{out}}{L} \times \frac{SW V_{out}}{V_{in \max} \times f_{sw}} \quad (3)$$

$$I_{Lrms} = \sqrt{I_{out}^2 + \frac{1}{12} \left(\frac{SW V_{out} \times (V_{in \max} - SW V_{out})}{V_{in \max} \times L \times f_{sw}} \right)^2} \quad (4)$$

$$I_{Lpeak} = I_{out} + \frac{I_{ripple}}{2} \quad (5)$$

For this design, the inductor ripple current is 294.61 mA, the RMS inductor current is 1 A, and the peak inductor current is 1.15 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

5 Output Capacitor Selection of the Switcher

Consider the three following primary requirements for selecting the value of the output capacitor of the switcher:

- Minimum capacitance to meet the load transient
- Minimum capacitance to meet the output voltage ripple
- Maximum ESR to meet the output voltage ripple

Select the output capacitor based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criterion. The output capacitor needs to supply the load with current when the regulator cannot. This is the situation if desired hold-up times occur for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is also temporarily unable to supply sufficient output current if a large, fast increase occurs in the load current needs such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the change in load current and output voltage to affect the control loop and adjust the duty cycle to react to the change. Size the output capacitor to supply the extra current to the load until the control loop responds to the load change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. Equation 6 shows the minimum output capacitance necessary to accomplish this.

$$C_{out} > \frac{2 \times \Delta I_{out}}{f_{sw} \times \Delta SW V_{out}} \quad (6)$$

Where ΔI_{out} is the change in output current, f_{sw} is the regulator's switching frequency, and ΔV_{out} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{out} for a load step of 0.75 A. Using these numbers ($\Delta I_{OUT} = 0.75$ A and $\Delta SW V_{out} = 0.04 \times 4.1 = 0.164$ V) gives a minimum capacitance of 19.05 μ F. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

Equation 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where f_{sw} is the switching frequency, V_{ripple} is the maximum allowable output voltage ripple of the switcher output, and I_{ripple} is the inductor ripple current calculated to be 294 mA. In this case, the maximum output voltage ripple is 41 mV. Under this requirement, Equation 7 yields 1.87 μ F.

$$C_{out} > \frac{1}{8 \times f_{sw}} \frac{I_{ripple}}{SW V_{ripple}} \quad (7)$$

Equation 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 8 indicates the ESR must be less than 139.45 m Ω .

$$R_{e\ sr} < \frac{SW V_{ripple}}{I_{ripple}} \quad (8)$$

The capacitance of ceramic capacitors highly depends on the dc output voltage. Use Equation 9 to select output capacitors based on their voltage rating. For 6.3-V C_{eff}=22.4 μ F in section13 minimum capacitance that meets the load step specification is 49.7 μ F. This example uses one 47- μ F, 6.3-V, X5R ceramic capacitor with 4 m Ω of ESR.

$$C = \frac{(C_{eff} - V_{rating})}{(V_{rating} - SW V_{out})} \quad (9)$$

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. Specify an output capacitor that can support the inductor ripple current. Some capacitor data sheets specify the RMS (root mean square) value of the maximum ripple current. Equation 10 can calculate the RMS ripple current the output capacitor needs to support. For this application, Equation 10 yields 85 mA.

$$I_{c\ rms} = \frac{SW V_{out}(V_{in\ max} - SW V_{out})}{\sqrt{12} \times V_{in\ max} \times L \times f_{sw}} \quad (10)$$

6 Input capacitor

The TPS54120 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of 4.7 μ F on each input voltage rail. In some applications, additional bulk capacitance also may be required for the PVIN input. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54120. The input ripple current for this design, using Equation 11, is 493 mA.

$$I_{c\ rms} = I_{out} \sqrt{\frac{SW V_{out}}{V_{in\ min}} \frac{(V_{in\ min} - SW V_{out})}{V_{in\ min}}} \quad (11)$$

The value of a ceramic capacitor varies significantly over both temperature and the amount of dc bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. The high capacitance-to-volume ratio and stability over temperature make the X5R and X7R ceramic dielectrics good selections for power regulator capacitors. The capacitance value of a capacitor decreases as the dc bias across it increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is necessary to support the maximum input voltage. For this example, 10- μ F, 25-V capacitors are the VIN and PVIN inputs tied together, so that the TPS54120 can operate from a single supply. The input capacitance value determines the input ripple voltage of the regulator. Use [Equation 12](#) to calculate the input voltage ripple. Using the design example values, $I_{outmax} = 1$ A, $C_{IN} = 10$ μ F, $f_{sw} = 480$ kHz, [Equation 12](#) yields an input voltage ripple of 52 mV.

$$\Delta V_{in} = \frac{I_{outmax} \times 0.25}{C_{in} \times f_{sw}} \quad (12)$$

7 Input Capacitor of the LDO

Although an input capacitor is unnecessary for stability, connecting a 0.1- μ F to 1- μ F low equivalent series resistance (ESR) capacitor across the input supply near the LDO input pin is good analog design practice. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if users anticipate large, fast, rise-time load transients, or if the device location is several inches from the power source. If source impedance is not sufficiently low, a 0.1- μ F input capacitor may be necessary to ensure stability. This design example uses a 10- μ F input capacitor.

8 Output Capacitor of the LDO

The internal LDO of the TPS54120 is stable with standard ceramic capacitors of capacitance values 4.7 μ F or larger. Higher values are recommended for better noise performance. The evaluated device used a 100- μ F ceramic capacitor of 6.3-V rating, 20% tolerance, X5R type, and 1812 size. X5R- and X7R-type capacitors are excellent choices because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω .

9 Slow-Start Capacitor Selection

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also useful if the output capacitance is large and requires a large amount of current to charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may either make the TPS54120 reach the current limit or the excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems. Use [Equation 13](#) to calculate the soft-start capacitor value. The example circuit has the soft-start time set to an arbitrary value of 3.5 ms which requires a 10-nF capacitor. In the TPS54120, I_{ss} is 2.3 μ A and V_{ref} is 0.8 V. For more details on how to use the soft-start capacitor for sequencing and tracking, see [SLVA497](#).

$$C_{ss} = \frac{T_{ss}(ms) * I_{ss}(\mu A)}{V_{ref}(V)} \quad (13)$$

10 Bootstrap Capacitor

Connect a 0.1- μ F ceramic capacitor between the BOOT to PH pin for proper operation. Use a ceramic capacitor with X5R or better- grade dielectric. The capacitor must have 10 V or higher voltage rating.

11 Output Voltage Feedback Resistor Selection

Use the resistor divider network, R5 and R6, to set the output voltage of the switcher, and use R1 and R2 to set the output voltage of the LDO. This example design uses 10 k Ω for R6 and R2. Calculated results of [Equation 14](#) and [Equation 15](#) for R5 and R1 are 41.2 k Ω and 30.9 k Ω , respectively. SW V_{out} is the output of the switcher, V_{out} is for the LDO, and V_{ref} is 0.8 V. Note that the LDO output must be 0.8 V below the SW output for best PSR and noise performance.

$$R5 = \frac{SW\ Vout - Vref}{Vref} R6 \quad (14)$$

$$R1 = \frac{Vout - Vref}{Vref} R2 \quad (15)$$

12 Switcher Minimum Output Voltage

The internal design of the TPS54120 sets a minimum switcher output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.8 V. Above 0.8 V, the minimum controllable on-time may limit the output voltage. In this case, [Equation 16](#) gives the minimum output voltage.

$$Vout\ min = ontime\ min \times Fs\ max (V_{INMAX} + I_{OUTMIN} (RDS2\ min - RDS1\ min)) - I_{OUTMIN} (R_L + RDS2\ min) \quad (16)$$

Where:

- V_{OUTMIN} = minimum achievable output voltage
- Ontimemin = minimum controllable on-time (135 ns maximum)
- Fsmax = maximum switching frequency including tolerance
- V_{INMAX} = maximum input voltage
- I_{OUTMIN} = minimum load current
- RDS1min = minimum high-side MOSFET on resistance (57 mΩ typical)
- RDS2min = minimum low-side MOSFET on resistance (50 mΩ typical)
- R_L = series resistance of output inductor

13 Compensation Component Selection

Several industry techniques can compensate dc/dc regulators; see the [SLVA503](#) application report for more details about different compensation networks for the TPS54120. The method in this application report is easy to calculate and yields high phase margins. For most conditions, the regulator has a phase margin between 60 degrees and 90 degrees. The method ignores the effects of the slope compensation that is internal to the TPS54120. Because this method ignores the slope compensation, the actual crossover frequency is usually lower than the crossover frequency in the calculations.

Type III compensation is used to achieve a high-bandwidth, high-phase-margin design. This design targets a crossover frequency (bandwidth) of 22.4 kHz. [Equation 17](#) and [Equation 18](#), calculates the power stage pole and zero at 1.73 kHz and 1778 kHz, respectively. For the output capacitance of the switcher, Cout, use a derated value of 22.4 μF, (unless otherwise noted).

$$f_{p\ mod} = \frac{I_{out}}{2\pi \times SW\ Vout \times C_{out}} \quad (17)$$

$$f_{z\ mod} = \frac{1}{2\pi \times RESR \times C_{out}} \quad (18)$$

Now the compensation components calculations are possible. First, calculate the value for R4, which sets the gain of the compensated network at the crossover frequency. Use [Equation 19](#) to determine the value of R4, and use Cout (the output capacitor of the switcher) without the derated value (47 μF).

$$R4 = \frac{2\pi \times f_c \times SW\ Vout \times C_{out}}{g_{m_{ea}} \times Vref \times g_{m_{ps}}} \quad (19)$$

Next, calculate the value of C8. Together with R4, C8 places a compensation zero at the modulator pole frequency. Use [Equation 20](#) to determine the value of C8.

$$C8 = \frac{SW\ Vout \times C_{out}}{I_{out} \times R4} \quad (20)$$

Using [Equation 19](#) and [Equation 20](#), the standard values for R4 and C8 are 2.2 kΩ and 0.041 μF. Select the next higher standard value for C8 to give a compensation zero that is slightly lower in frequency than the power stage pole.

In order to provide a zero around the crossover frequency to boost the phase at crossover, add a capacitor (C11) parallel to R5. [Equation 21](#) gives the value of this capacitor. The nearest standard value for C11 is 100 pF.

$$C11 = \frac{1}{2\pi \times R5 \times fc} \quad \leftarrow \text{C11=174pF} \quad (21)$$

Using the feedforward capacitor, C11, creates a low, ac impedance path from the output voltage to the VSENSE input of the integrated circuit that can couple noise at the switching frequency into the control loop. Do not use a feedforward capacitor for high-output voltage ripple designs (greater than 15 mV peak-to-peak at the VSENSE input) operating at duty cycles of less than 30%. When using the feedforward capacitor, C11, always limit the closed-loop bandwidth to no more than 1/10th of the switching frequency.

Use an additional high-frequency pole if necessary by adding a capacitor in parallel with the series combination of R4 and C8. Equation 22 gives the pole frequency. Set this pole at roughly half of the switching frequency (of 480 kHz) by using a 330-pF capacitor for C6. This helps attenuate any high-frequency signals that may couple into the control loop.

$$fp = \frac{1}{2\pi \times R5 \times C6} \quad \leftarrow \text{R5 should be R4, C6=300pF} \quad (22)$$

14 Noise-Reduction Capacitor

In most LDOs, the bandgap is the dominant noise source. If a noise-reduction capacitor (CNR) is used with the TPS54120, the bandgap does not contribute significantly to noise. Instead, the output resistor divider and the error amplifier input dominate the noise. To minimize noise in a given application, use a 0.01-μF (minimum) noise-reduction capacitor.

In addition to noise-reduction purposes, the capacitor on the NR pin slows start-up time. The noise-reduction effect is nearly saturated at 0.01 μF. Changing the value of CNR can adjust the start-up time of the LDO. For more detail on how to use this pin, see [SLVA497](#).

15 Test Results

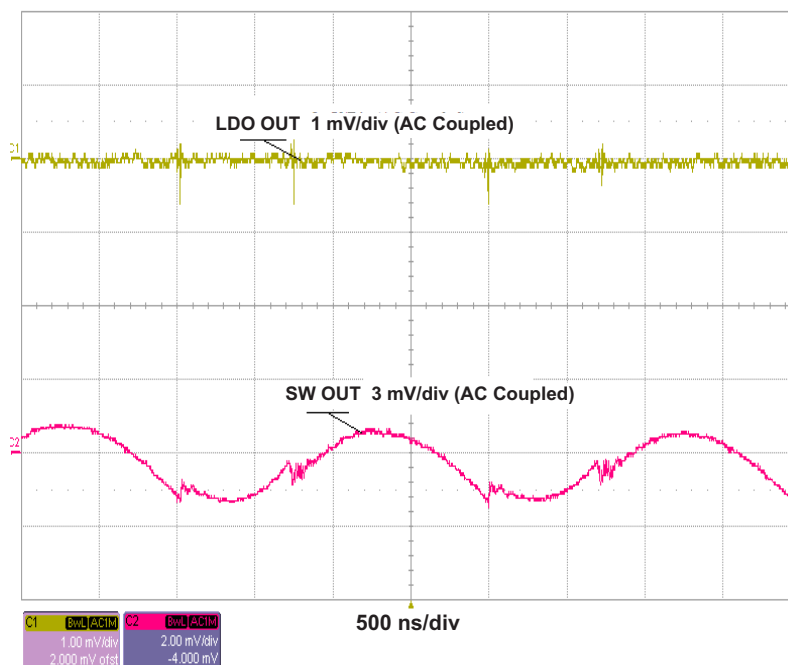


Figure 2. SW Output and LDO Output IN = 12 V, SWOUT = 4.1 V, LDO OUT = 3.3 V, Load = 400 mA

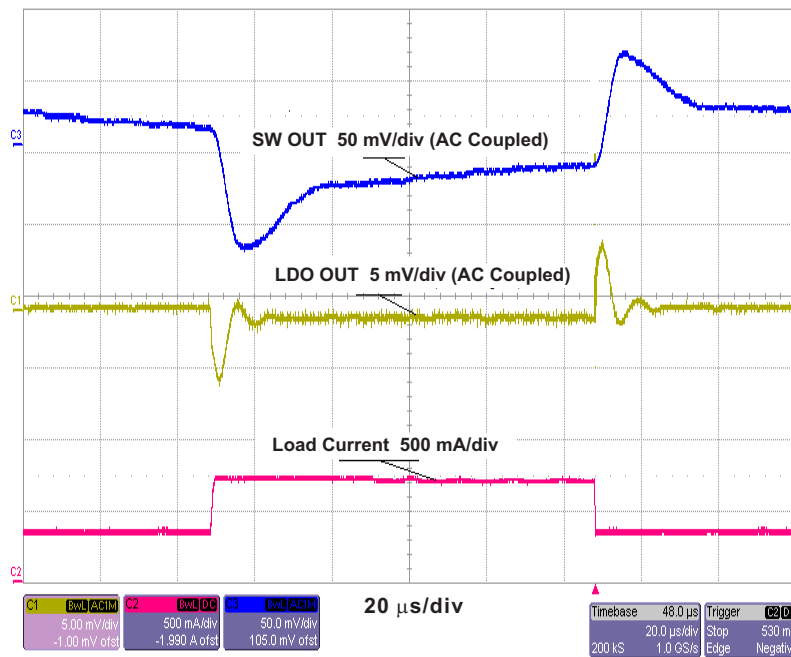


Figure 3. Transient Response VIN = 12 V, SWOUT = 4.1 V, LDO OUT = 3.3 V, Load = 400 mA to 750 mA

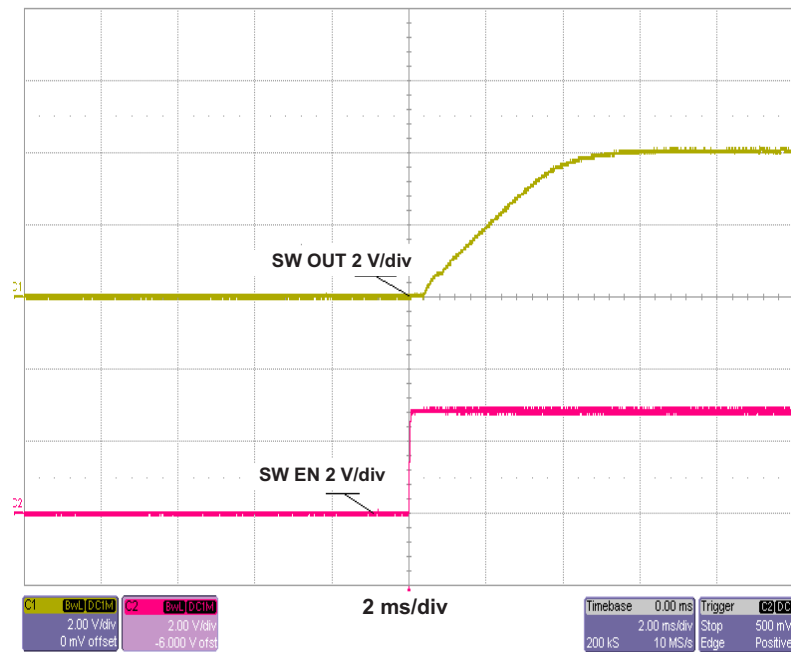


Figure 4. Start-Up at SW Using SW Enable VIN = 12 V, SWOUT = 4.1 V, LDO OUT = 3.3 V, Load = 400 mA

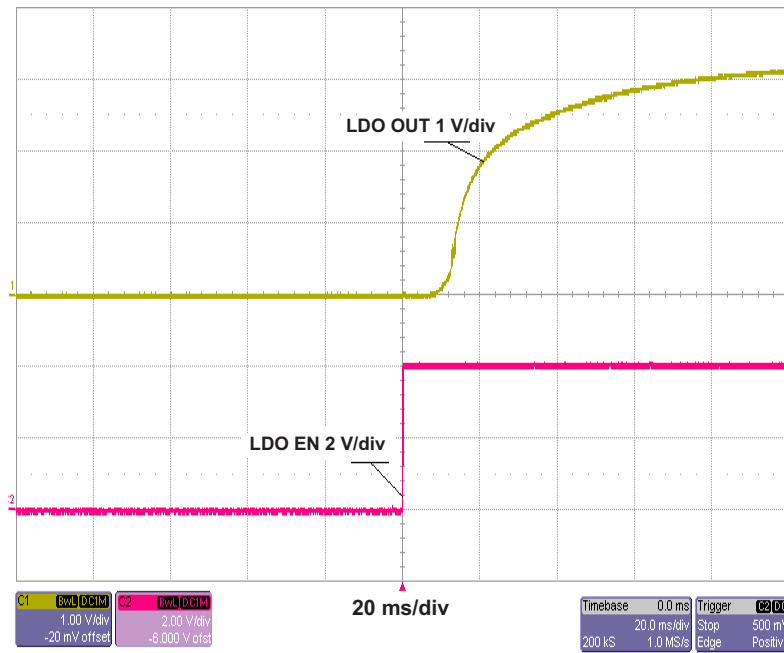


Figure 5. Start-Up at LDO Using LDO Enable VIN = 12 V, SWOUT = 4.1 V, LDO OUT = 3.3 V, Load = 400 mA

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