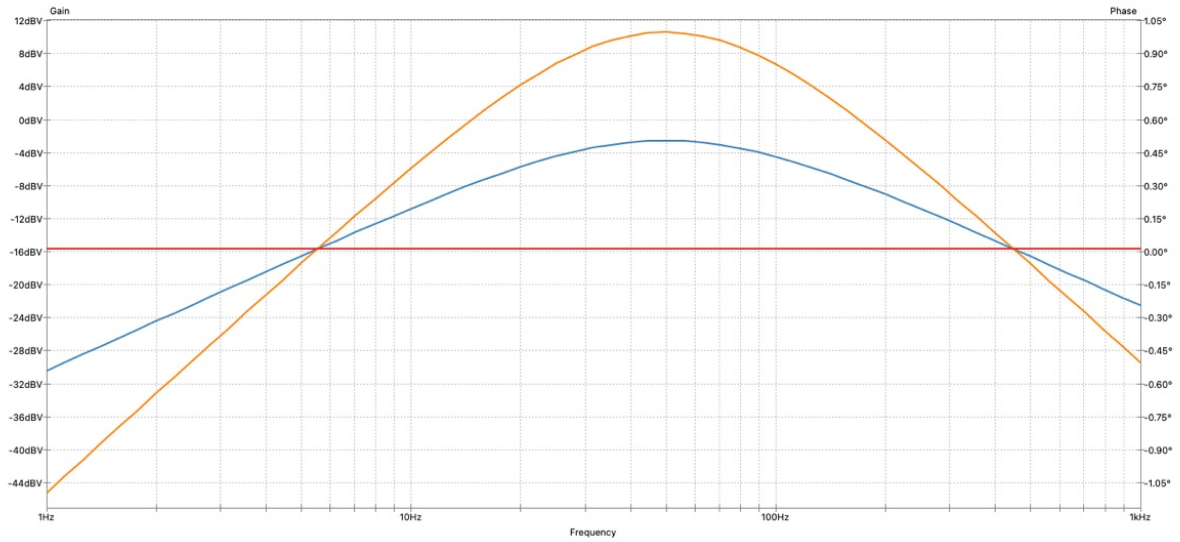
## Atish - Phase Selection

| Version | Changes |
|---|---|
| V0.1 | - Changed to a rail to rail opamp.<br>- Corrected the filter values for correct cutoff frequencies.<br>- Changed the overall gain to 20x<br>- Removed voltage divider Resistors.<br>- Added a voltage reference with buffer.<br>- |
| V0.2 | Schematic:<br>- Correct filter values based on ngspice simulation.<br>- Use internal oscillator and remove requirement for a crystal.<br>- PIC with lower pincount.<br><br>PCB<br>- Updated layout. Not complete. |

## V0.2 Updates

### Filter values

With the updated filter values the overall gain is +/- 24dBV with a bandwidth of +/- 40Hz around 50Hz nominal mains frequency. Modelled with ngspice:




### Oscillator

Using the internal oscillator removes the requirement to have an external crystal. Therefore pins 13 and 14 are no longer connected.

### PIC18F26K22

Lower pin count as the number of I/O pins required is low. Also allows for in circuit programming.

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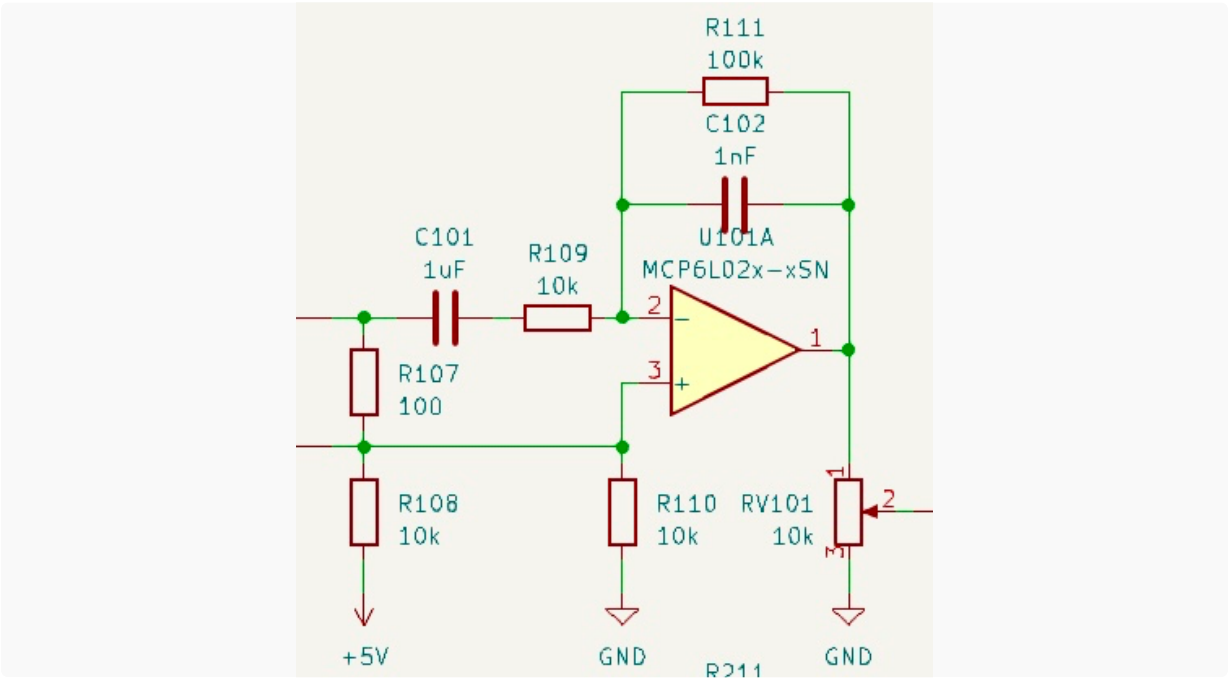
## V0.1 Updates

### OpAmp Selection

I have chosen the MCP6002 from Microchip as we are already using the PIC microcontroller from MCP. This is a single voltage rail to rail dual opamp.

### Filter calculation




This is a band pass filter with following characteristics:

- Gain: 10
- Calculated Low Cutoff Frequency: 45Hz
- Calculated High Cutoff Frequency: 55Hz

Gain of 10 is achieved by the ratio between R111 and R109; In fact it is -10 because it is an inverting opamp circuit

$$Gain = \frac{R111}{R109} = \frac{100k}{10k} = 10$$

The High Cutoff Frequency with the given values was:

$$HCF = \frac{1}{2 * \pi * C101 * R109} = \frac{1}{2 * \pi * 1 * 10^{-}6 * 1 * 10^{4}} = \pm 16Hz$$

With the given resistance value required for the gain to be 10, C101 becomes:

$$C101 = \frac{1}{2 * \pi * HCF * R109} = \frac{1}{2 * \pi * 55 * 1 * 10^{4}} = \pm 290nF$$

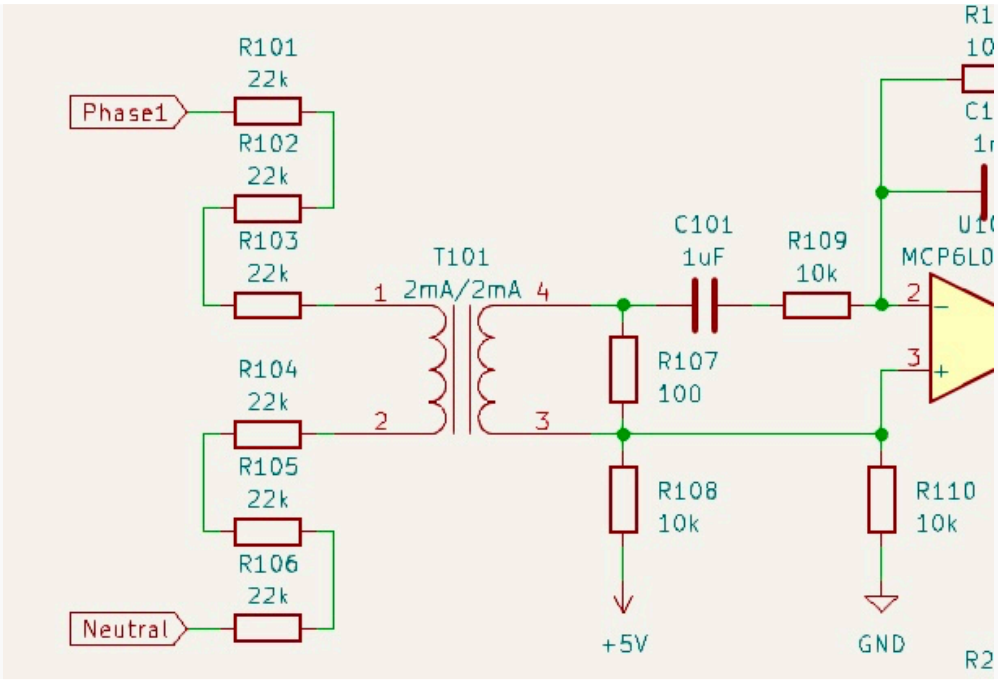
The Low Cutoff Frequency with the given values was:

$$LCF = \frac{1}{2 * \pi * C102 * R111} = \frac{1}{2 * \pi * 1nF * 100K} = \pm 1600Hz$$

With the given resistance value required for the gain to be 10, C102 becomes:

$$C102 = \frac{1}{2 * \pi * LCF * R111} = \frac{1}{2 * \pi * 45 * 100k} = \pm 35nF$$

## Sense value and opamp set point




Phase1 and Neutral carry 230Vrms over 6 * 22k + 150; the peak current is therefore:

$$I_{T101} = \frac{\sqrt{2} * 230}{6 * 22 * 10^{3} + 150} = 2.46mA$$

The recommended current value is around 1.5mA. This requires the resistors R101-R106 to be 33k. This results in a current of 1.64mA.

R107 is the sampling resistor with the recommended value of 100R. The peak voltage over this resistor is therefore 164mV. This voltage is superimposed on the 2.5V created by R108 and R110 and supplied to the opamp where it is filtered and amplified by 10.

Alternatively a common voltage reference could be used for the 6 opamps and the MCU.

The output from the first stage is therefor 2.5V +/- 1.64V or 0.86V to 4.14V. This also means that the second stage doesn't require 10x gain and the resistor and capacitor values will be modified accordingly. I opted for a 2x gain setup to allows for fine-tuning and calibration using the potmeter.

## Sampling method vs. bridge rectifier.

Given that the cycletime is 20ms, the positive peak of the signal will fall at around 5ms after a negative to positive zero crossing. Starting a sampling cycle at this point and provided that enough samples are taken, the peak will be recognized without the need for rectification of the signal. This avoids having to add additional (non-linear) circuitry.

The sampling cycle has to be started for the three phases separately due to the 120° phase difference. Depending on the speed of the processor this could be a few cycles apart.