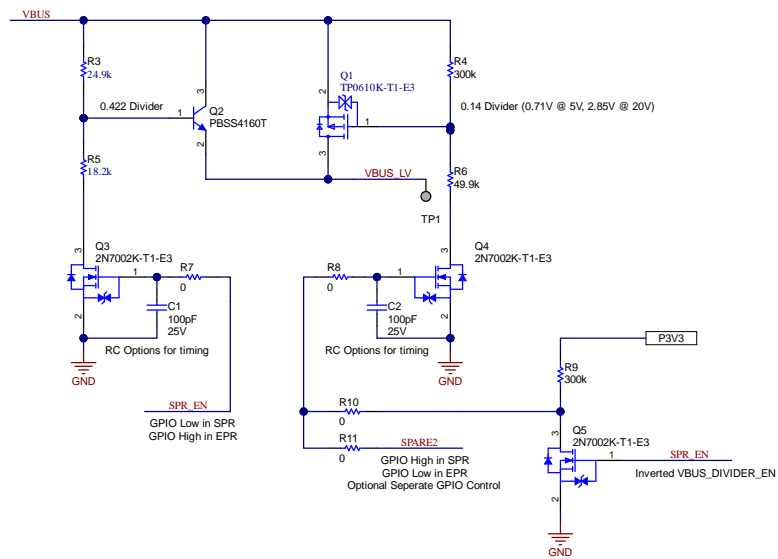
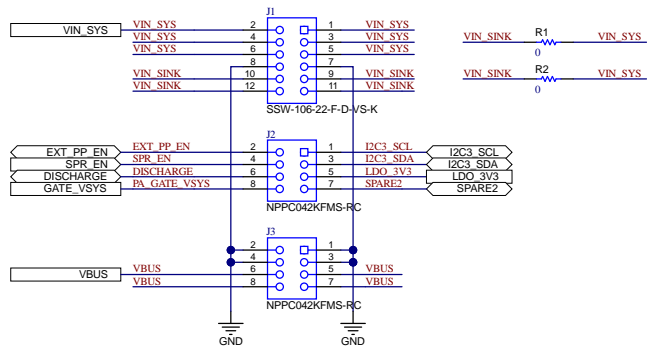


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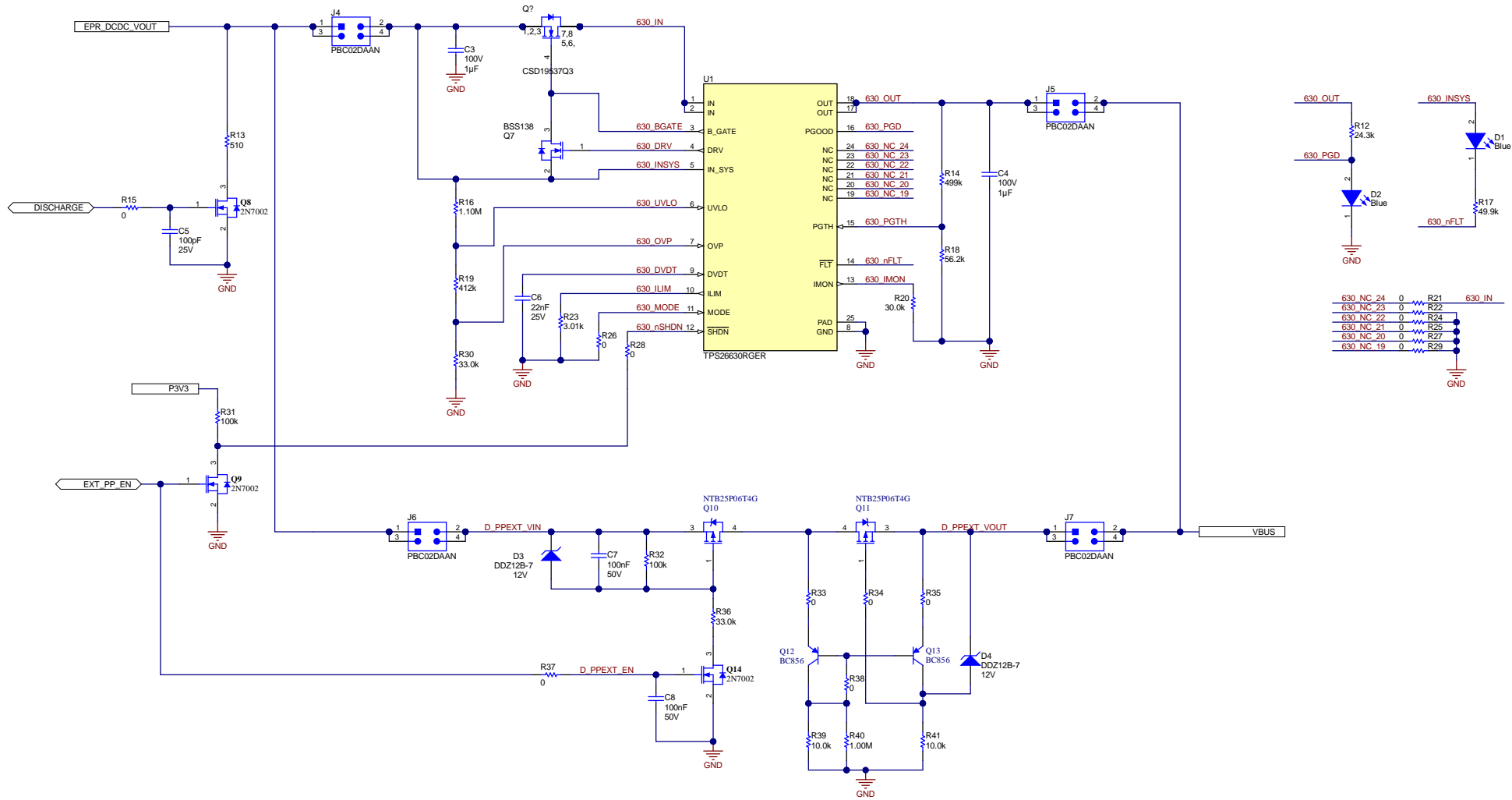
Orderable:	Designed for: Public Release	Mod. Date: 2/4/2022
TID #:	N/A	Project Title: Change in menu Project\Project Options\Parameters
Number: XXX##	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 1 of 5
Drawn By:	File: EPR_LM5176_Source_Board_Block_Diagram.SchDoc	http://www.ti.com
Engineer: Enter name of project lead	Contact: http://www.ti.com/support	©Texas Instruments 2018





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Orderable:	Designed for: Public Release	Mod. Date: 2/4/2022
TID #:	Project Title: Change in menu Project\Project Options\Parameters	
Number: XXX###	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 2 of 5
Drawn By:	File: EPR_LM5176_Source_Board_Header.SchDoc	Size: B
Engineer: Enter name of project lead	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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Orderable:	Designed for: Public Release	Mod. Date: 2/4/2022
TID #:	Project Title: Change in menu Project\Project Options\Parameters	
Number: XXX###	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 3 of 5
Drawn By:	File: EPR_LM5176_Source_Board_Power_Paths.Sch	Size: B
Engineer: Enter name of project lead	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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H1 NY PMS 440 0025 PH  
 H2 NY PMS 440 0025 PH  
 H3 NY PMS 440 0025 PH  
 H4 NY PMS 440 0025 PH

H5 1902C  
 H6 1902C  
 H7 1902C  
 H8 1902C

H9 SJ-5303 (CLEAR)  
 H10 SJ-5303 (CLEAR)  
 H11 SJ-5303 (CLEAR)  
 H12 SJ-5303 (CLEAR)

FID1  
 FID2  
 FID3

PCB Number: XXX##  
 PCB Rev: E1

PCB LOGO  
 Texas Instruments



PCB LOGO  
 FCC disclaimer

PCB LOGO  
 WEEE logo

You should delete the nylon screws/standoffs and/or the bumpers as needed for your design (or substitute other parts from Hardware.IntLib). Bumpers are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You should delete this note too.

Variant/Label Table	
Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1  
 PCB Label  
 THT-14-423-10  
 Size: 0.65" x 0.20"

ZZ1  
 Label Assembly Note  
 This Assembly Note is for PCB labels only

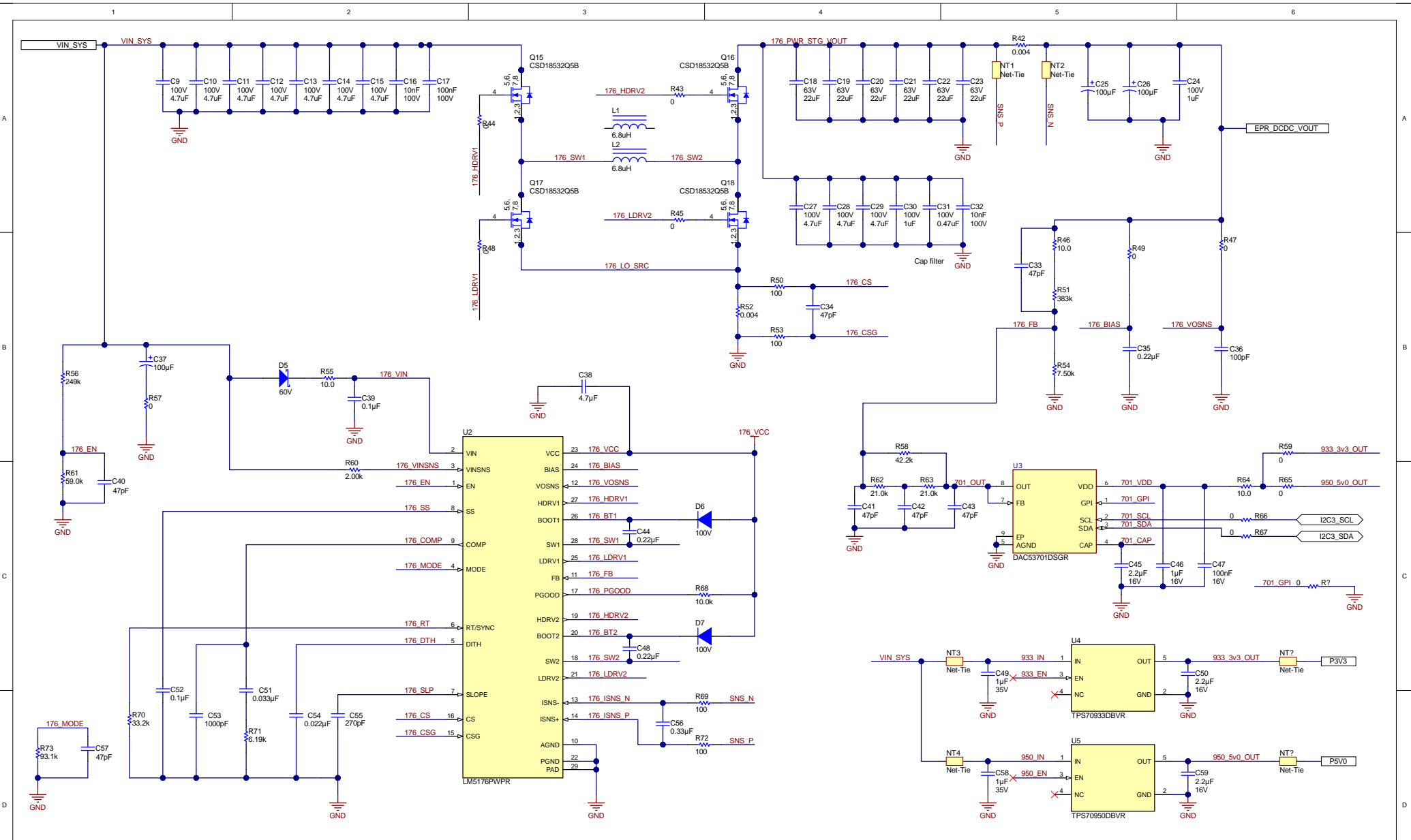
ZZ2  
 Assembly Note  
 These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3  
 Assembly Note  
 These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4  
 Assembly Note  
 These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Orderable:	Designed for: Public Release	Mod. Date: 2/4/2022
TID #:	N/A	Project Title: Change in menu Project\Project Options\Parameters
Number: XXX##	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 4 of 5
Drawn By:	File: EPR_LM5176_Source Board_Hardware.SchDoc	Size: B
Engineer: Enter name of project lead	Contact: http://www.ti.com/support	http://www.ti.com



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Orderable:	Designed for: Public Release	Mod. Date: 2/4/2022
TID #:	Project Title: Change in menu Project/Project Options/Parameters	
Number: XXX##	Rev: E1	Sheet Title:
SVN Rev: Not in version control	Assembly Variant: [No Variations]	Sheet: 5 of 5
Drawn By:	File: EPR_LM5176_DCDC_Power_Supplies_SchDoc	Size: B
Engineer: Enter name of project lead	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	



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Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.40mil	3,5	
1	Top Layer		1.40mil		
	Dielectric1	FR-4 High Tg	59.20mil	4,8	
2	Bottom Layer		1.40mil		
	Bottom Solder	Solder Resist	0.40mil	3,5	
	Bottom Overlay				

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.  
 Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.  
 Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.  
 Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

DESIGN INFORMATION

MIN. TRACK WIDTH: 8 MIL  
 MIN. CLEARANCE: 7,874 MIL  
 MIN. VIA PAD SIZE: 24 MIL

MINIMUM ANNULAR RING 0.05mm (2ML) EXTERNAL  
 PER IPC-D-275 CLASS 2 LEVEL C  
 REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL  
 HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:  
 FR-408  FR-4 High Tg  OTHER \_\_\_\_\_

THICKNESS:  62 MIL (1.6mm) +/-10%  OTHER \_\_\_\_\_

TOLERANCE:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

BOW & TWIST:  ANSI IPC-6012 TYPE 3 CLASS 2  
 OTHER +/- \_\_\_\_\_

DRILLING:  
 REFERENCE:  AS SHOWN  NC\_DRILL FILES  
 PTH COPPER THICKNESS:  20-30 um  OTHER \_\_\_\_\_

BOARD FINISH:  
 SILKSCREEN:  TOP  BOTTOM  
 SILKSCREEN COLOR:  WHITE  OTHER \_\_\_\_\_  
 SOLDER RESIST COLOR:  GREEN  OTHER \_\_\_\_\_  
 MATTIE  SEMI-GLOSS

SURFACE FINISH:  IMMERSION GOLD (ENG)  ENERP  
 IMM. TIN/SILVER OR EQUIV  OTHER \_\_\_\_\_

ARRAY/PANEL:  CUT AND TRM PER M1 BOARD OUTLINE  
 N.C. ROUTE  V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:  
 ANSI IPC-A-600F CLASS ->  1  2  3  
 RoHS  OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.  
 PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:  
 MICROSECTION:  YES

BARE BOARD ELEC. TEST:  NONE  REQUIRED  PER ORDER  
 XX MIL VIAS REQUIRE NON-CONDUCTIVE FILL AND PLANARIZE  
 XX MIL VIAS REQUIRE CONDUCTIVE FILL AND PLANARIZE  
 OUTER XX MIL TRACES REQUIRE 50 OHM SINGLE-ENDED IMPEDANCE  
 LAYER 2 & 3 (INNER LAYERS) XX MIL WIDE, XX MIL SPACE  
 TRACES REQUIRE 100 OHM DIFFERENTIAL IMPEDANCE

For evaluation only; not FCC approved for resale.

This document can handle board shapes up to 7.9in x 10in, although our panel vendors top out at 7in x 10in.  
 To re-size the board shape, do the following:  
 Select lines on MI Board Outline and delete (easy in single layer mode...shift+)  
 Draw a rectangle using lines (example will be for a 4 x 6 board)  
 Enter Place Line mode (keyboard pl)  
 keyboard jo to jump to origin, hit enter  
 keyboard jl to jump to location, set x to 6000, hit enter twice  
 keyboard jl to jump to location, set x to 6000 and y to 4000, hit enter twice  
 keyboard jl to jump to location, set x to 0 and y to 4000, hit enter twice  
 keyboard jo to jump to origin, hit enter  
 Hit ESC twice to exit place line mode  
 Select lines on MI Board Outline  
 Menu DesignBoard ShapeDefine from Selected Objects (keyboard dsd)

If you re-size the board, don't forget to move the drill table strings on the Drill Drawing Layer...they should be just to the right of your board shape

COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED. COMPONENTS MARKED 'DNP' SHOULD NOT BE ORDERED.  
 ASSEMBLY VARIANT: [No Variations] [No Variations]

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TEXAS INSTRUMENTS

PROJECT TITLE:  
Change in menu Project\Project Options\Parameters

DESIGNED FOR:  
Public Release

FILE NAME:  
EPR LM5176 Source Board.PcbDoc

ENGINEER:  
Enter name of project

LAYOUT BY:  
beddid the Layout?

SCALE: 1.00

ALTIM DESIGNER VERSION:  
22.1.2.22

