ESD Summary | TPSI2140-Q1

1 March 2024

LP-PS

Testing with Y1 capacitor to mimic customer solution

8 April 2024

Summary: Test setup with Y1 capacitor

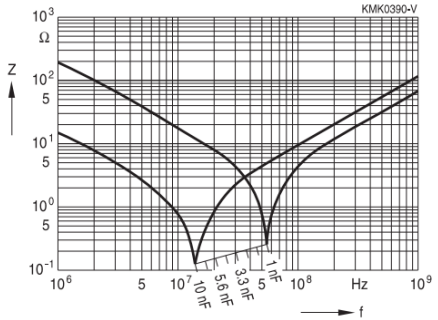
Takeaways

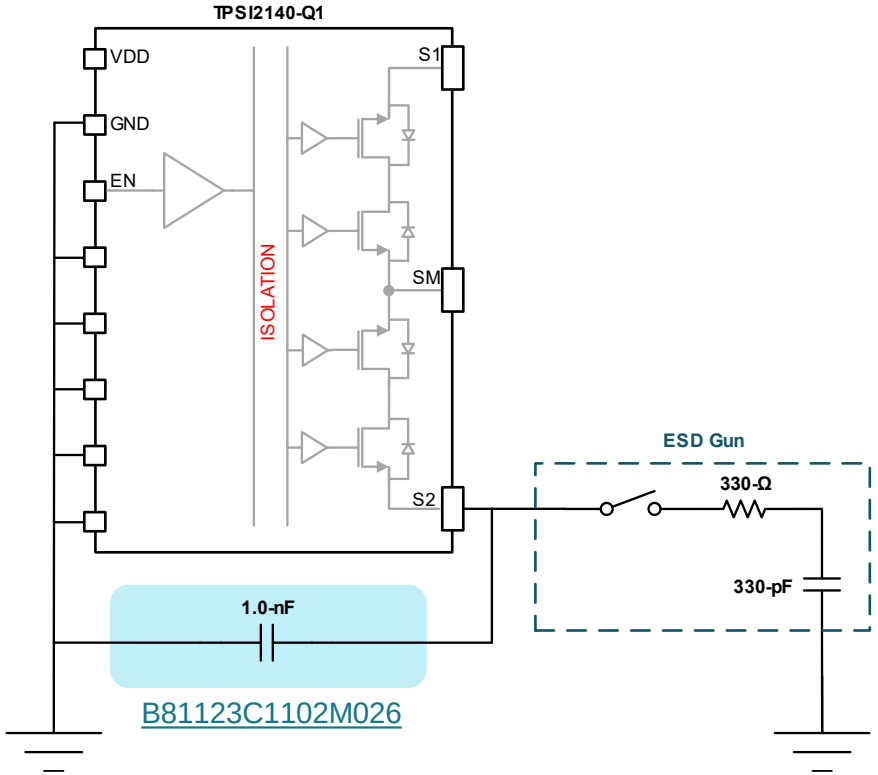
✓ 1-nF Y1 capacitor seems to be sufficient for single 15-kV ESD strike
- Multiple strikes would require either discharge resistor (1-MΩ ± 20% per IEC 10605) or manual discharge in-between strikes

Uncertainties

- Unclear why failure signature was different for tested units (fail closed vs. fail open)
- Need to confirm capacitor's energy absorption capabilities with manufacturer
- Need to confirm impedance vs. frequency behavior with manufacturer

Impedance Z versus frequency f
(typical values)





Test setup with Y1 capacitor

Considered Y1 Capacitor Specifications

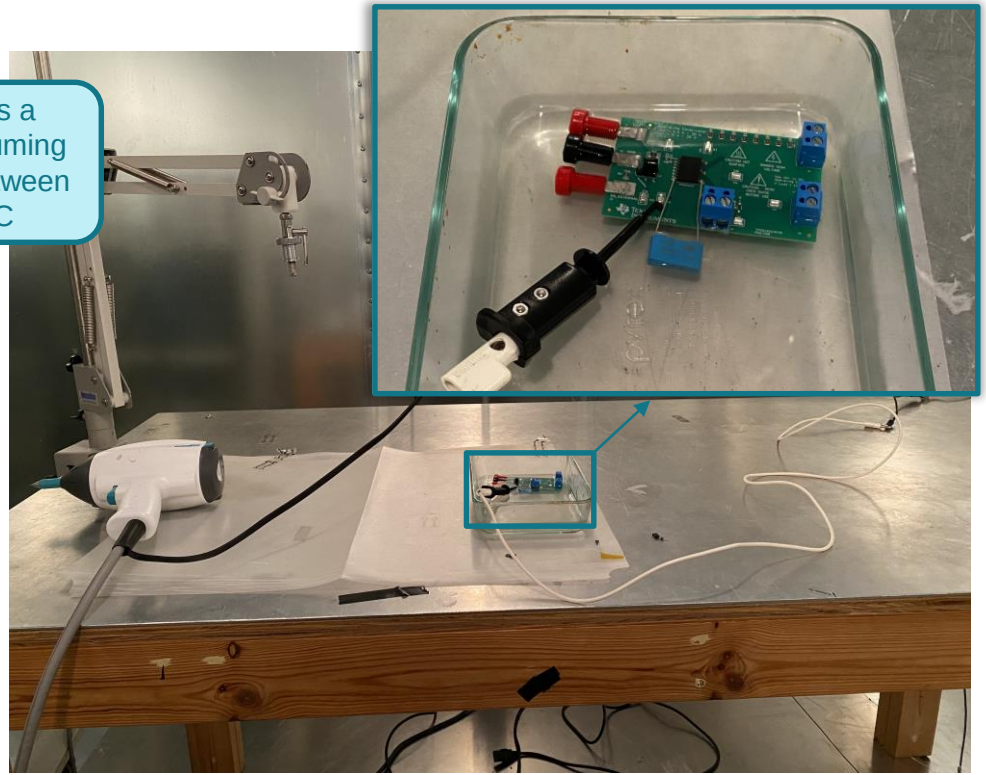
Testing and Standards

Test	Reference	Conditions of test	Performance requirements
Electrical parameters	IEC 60384-14:2013/ AMD1:2016	Voltage Proof: Between terminals: 4000 V AC, 1 min Terminals and enclosure: 4000 V AC, 1 min Insulation resistance, R_{ins} Capacitance, C Dissipation factor, tan δ	Within specified limits

Max. operating temperature $T_{op,max}$	+110 °C	
Dissipation factor tan δ (in 10^{-3}) at 20 °C (upper limit values)	at 1 kHz	1.0
	at 100 kHz	5.0
Insulation resistance R_{ins} or time constant $\tau = C_R \cdot R_{ins}$ at 20 °C, rel. humidity ≤ 65% (minimum as-delivered values)	30 000 MΩ	
DC test voltage	4800 V, 2 s	

The repetition of this DC voltage test may damage the capacitor. Special care must be taken in case of use several capacitors in a parallel configuration.

ESD pulse is a transient, assuming behavior is between AC and DC



Voltage Reduction

- Need to keep voltage across TPSI2140-Q1 ≤ 5.0-kV
- Charge in capacitor is determined by $Q = C \cdot V$
- ✓ Final voltage across Y1-cap/TPSI2140-Q1 = 3.7-kV

Uncertainties

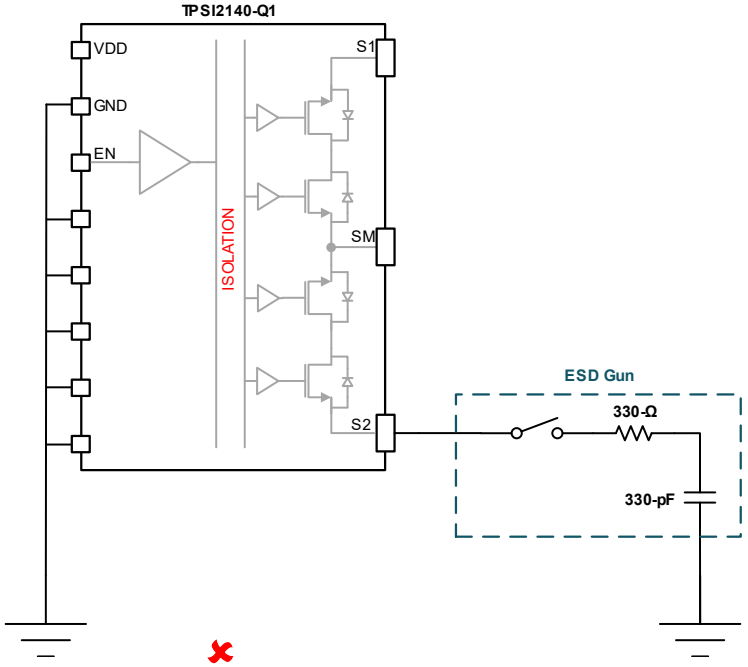
- Need to confirm capacitor's energy absorption capabilities with manufacturer
- Need to confirm impedance vs. frequency behavior with manufacturer

Test Details

Unit	V	I_{DD}	R_{DSOFF}				R_{DSON}				
			S1-SM	SM-S1	S2-SM	SM-S2	S1-SM	SM-S1	S2-SM	SM-S2	
1	15-kV	8.8-mA	OL				60-Ω				
	20-kV	✓	✓				✓				
	25-kV	✓	✓				✓				
	30-kV	✓	✓				✓				
	30-kV (2x)	250-mA	62-Ω				62-Ω				Fail closed
2	15-kV	8.9-mA	OL				60-Ω				
	20-kV	✓	✓				✓				
	25-kV	✓	✓				✓				
	30-kV	150-mA	✓				OL				Fail open

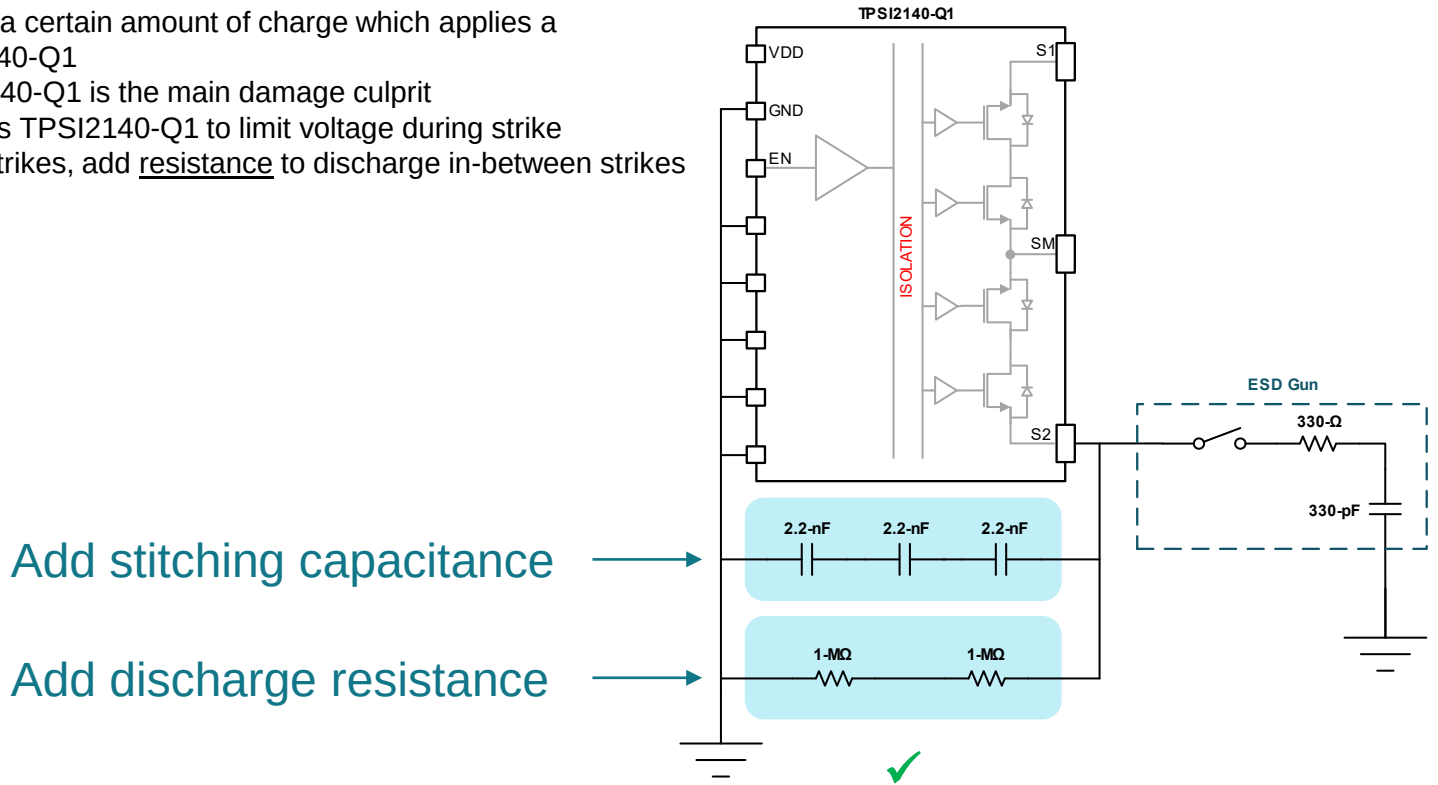
Background

- Customer applies 15-kV ESD strike across device and notices failure



Solution: Add Capacitance

- An ESD strike delivers a certain amount of charge which applies a voltage across TPSI2140-Q1
- Voltage across TPSI2140-Q1 is the main damage culprit
- Add capacitance across TPSI2140-Q1 to limit voltage during strike
- If performing multiple strikes, add resistance to discharge in-between strikes



How to Determine Capacitance Needed

Example ESD Test

- 50 strikes, 50-ms interval at 15-kV
- 330-pF/330-Ω cartridge

Capacitance Selection

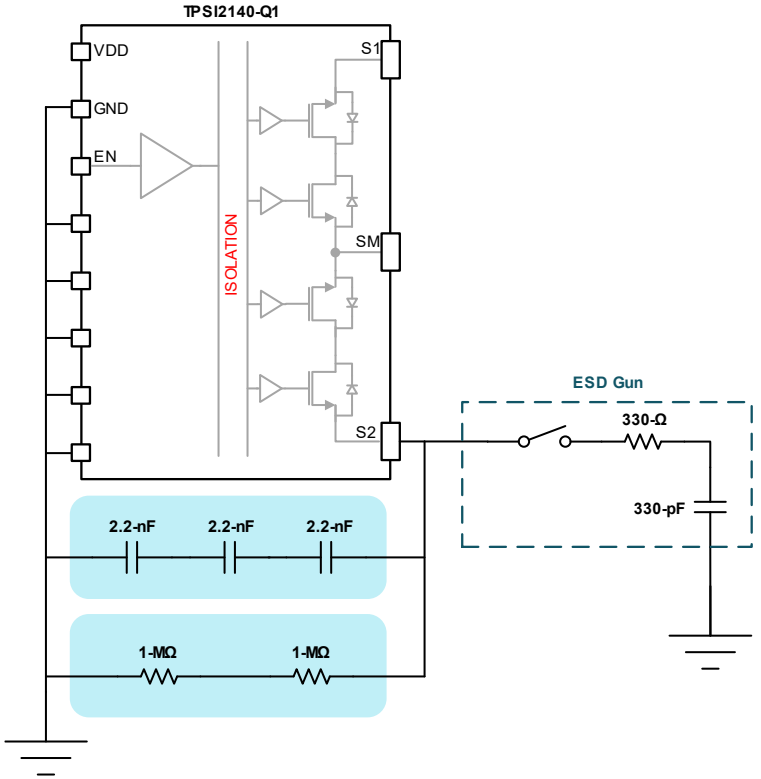
- Charge in capacitor is determined by $Q = C \cdot V$
- Keep voltage across TPSI2140-Q1 ≤ 5.0-kV
- This means stitch capacitance needs to be ≥ 660-pF

Resistance Selection

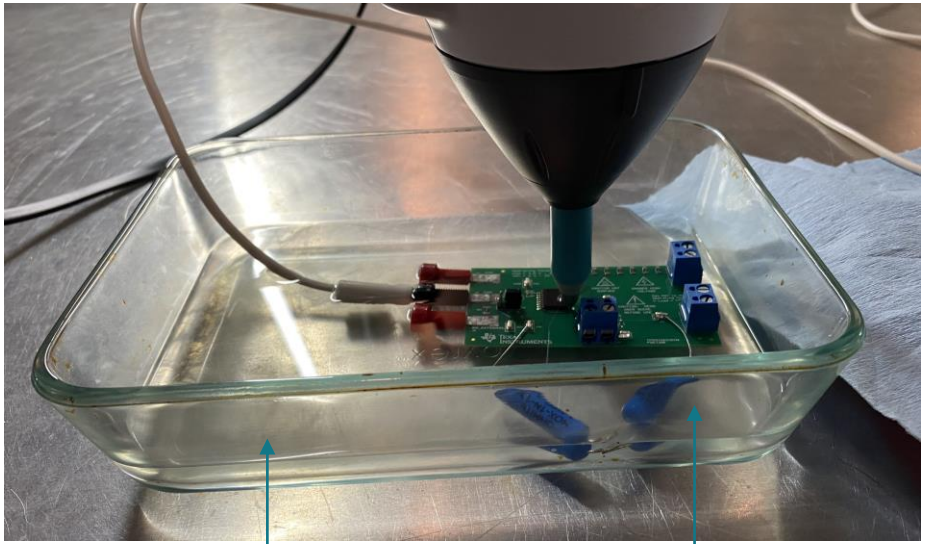
- Stitch capacitance needs to discharge in-between strikes
- Assume full discharge is $5 \cdot RC$

$$5 \cdot RC = 50\ ms$$

$$R \leq 14.3\ M\Omega$$



Test Setup



Submerged in high dielectric liquid, prevent arcing

2x 1-MΩ resistors

3x 2.2-nF (2-kV) capacitors

Test Summary

Setup Details				Pre-Test			Post-Test			
Strike Voltage	**Unit #**	**ESD Capacitance (S2-PGND)**	**Device State**	**IDD**	**RON**	**ROFF**	**IDD**	**RON**	**ROFF**	**Result**
±15kV (1 strike at each polarity)	1	733pF (3x 2.2nF in series)	Powered ON and OFF	8.91mA	121.4ohms	OL	8.91mA	119.9ohms	OL	**PASS**
+15kV	2	No Capacitance	Powered OFF	8.97mA	124ohms	OL	14.1mA	S1-SM: 60.8ohms SM-S2: 13.25kohms	S1-SM: OL SM-S2: 389kohms	**FAIL**
5kV-6.5kV (baseline)	3	No Capacitance	Powered OFF	9.0mA	125ohms	OL	17.27mA	S1-SM: 60ohms SM-S1: 60ohms SM-S2: 1.58Mohms S2-SM: OL	S1-SM: OL SM-S1: OL SM-S2: 1.58Mohms S2-SM: OL	**FAIL** at 6.5kV
+11kV	4	333-pF (3x 1-nF in series)	Powered OFF	8.91-mA	119-Ω	OL	19-mA		SM-S2: 335-kΩ	**FAIL**
±15kV (50 strikes, 50-ms interval)	5, 6, 7	733-pF (3x 2.2-nF in series) 2-MΩ (2x 1-MΩ in series)	Powered ON and OFF	8.77-mA	118.9-Ω	OL	8.77-mA	118.9-Ω	OL	**PASS**

Confirms failure when voltage ≥ 5.5-kV