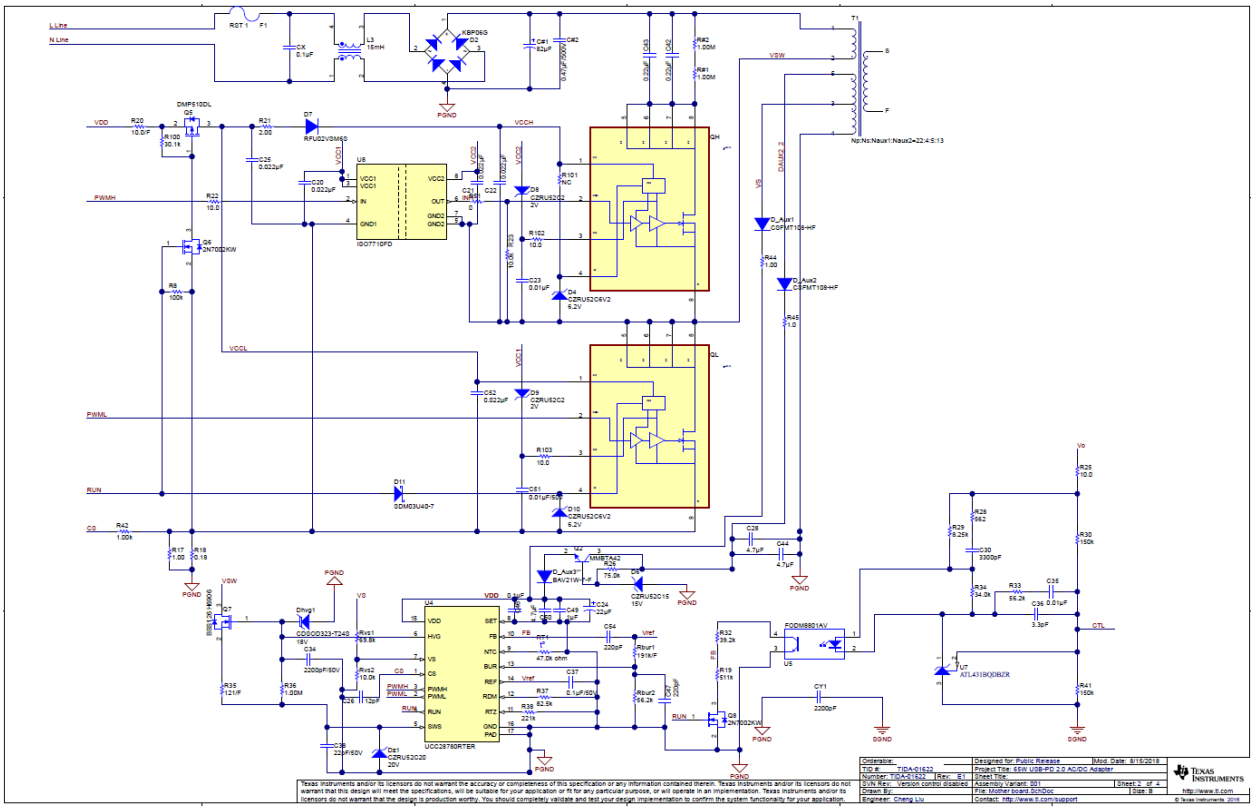
Hello Eleven,

I was not sure, but are you talking about the UCC28780 65W USB reference design? http://www.ti.com/tool/TIDA-01622 However, I can use this 65 W design to show how the OCP, PCL and OCP protections work.



I am going to evaluate the TI reference design to see where the PCL limit occurs.

CS INPUT						
$V_{CST(MAX)}$	Maximum CS threshold voltage	V_{CS} increasing	765	800	825	mV

Evaluate power level based on User's Guide

$Vcst\_max := 0.825V$

$R17 := 1ohm$

$R18 := 0.18ohm$

$$Rcs := \frac{R17 \cdot R18}{R17 + R18}$$

$Rcs = 0.153\,\Omega$ Current Sense Resistance

$$Ipk := \frac{Vcst\_max}{Rcs} = 5.408\,A$$

$Nps := 5.5$ Transformer turns ratio used in the UCC28780 65W reference design

Transformer should be set based on volt second balance. The following is an estimate of how the transformer turns ratio could be set.

$Vinmin := 72V$ $Vout := 20V$

$Vrdson := 0.20V$ Estimate of synchronous rectifier Rdson voltage drop on secondary and primary FET.

$$Nps = \frac{(Vinmin - Vrdson) \cdot Dmax}{(Vout + Vrdson)(1 - Dmax)}$$

Dmax can be calculated based on Nps and estimates for

$$Dmax := \frac{Nps \cdot Vout + Nps \cdot Vrdson}{Vinmin - Vrdson + Nps \cdot Vout + Nps \cdot Vrdson} = 0.607$$

Based on conservation of energy, Nps and Dmax the maximum output power during PCL can be calculated. For this design I estimated that it can deliver 116.7 W for 160 ms.

$$\frac{Vin}{Vout} = Nps = \frac{Iout}{Iin}$$

$$Iin := \frac{Ipk \cdot Dmax}{2}$$

$$Iout := \frac{Ipk \cdot Nps \cdot (1 - Dmax)}{2} = 5.839\,A$$

$Pout\_max := Iout \cdot Vout = 116.772\,W$

Calculate OPP trip point at 72 V input to the flyback converter

First you need to calculate the IVSL current at 72 V input.

$Npa := 4.4$ The primary to aux turns ratio.

$Rvs1 := 69.8 \cdot 10^{3} ohm$

$$Ivsl\_72V := \frac{Vinmin}{Nps \cdot Rvs1} = 1.875 \times 10^{-4} A$$

This design uses a Ropp of zero ohms, so figure 5 from the data sheet can be used calculate the VCST(OPP) trip point at the CS pin base on IVSL. At a IVSL = 187.5 uA the CS trip point for VCST(OPP) is 600 mV.

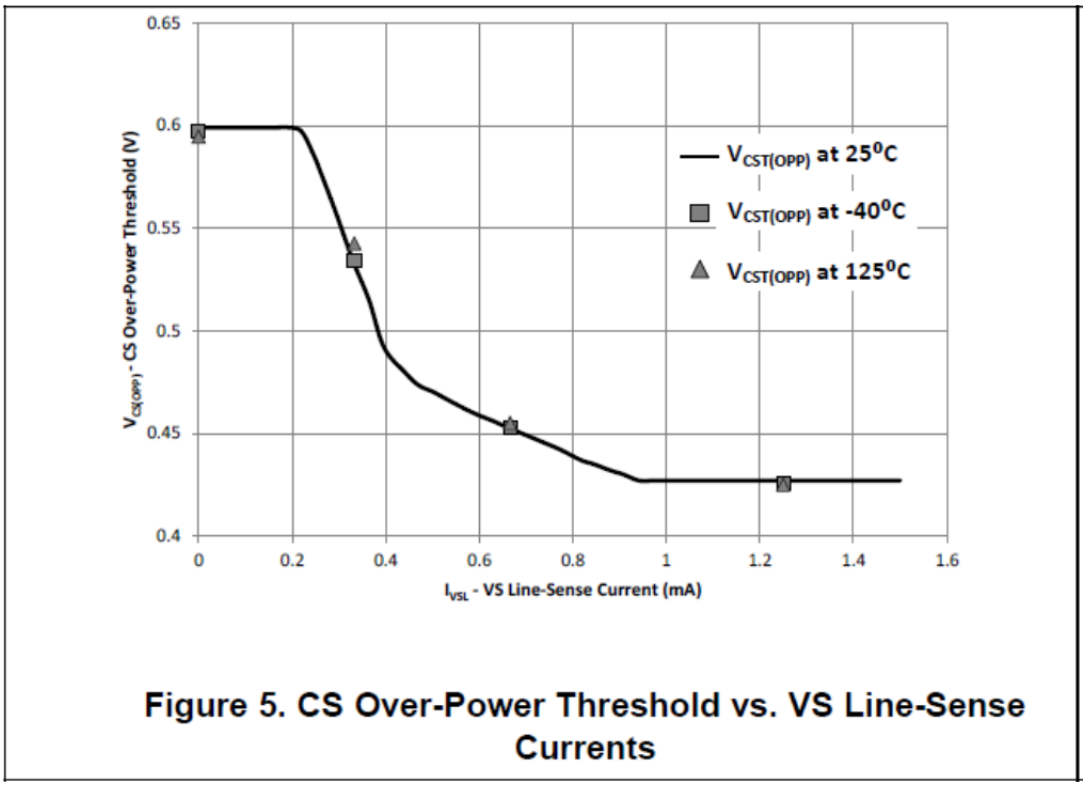


Figure 5. CS Over-Power Threshold vs. VS Line-Sense Currents

Based on a Vcst(opp) of 0.6V the OPP trip point will be roughly 85W.

$Vcst\_opp := 0.6V$

$$Popp := \frac{Vcst\_opp \cdot Nps \cdot (1 - Dmax) \cdot Vout}{Rcs \cdot 2} = 84.925 W$$

So what this means is if the converter is delivering more 85W for a 160 ms or more the converter will initiate a VDD UVLO restart (VVDD(off) to VDD(on)). Please refer to the following figure for details.

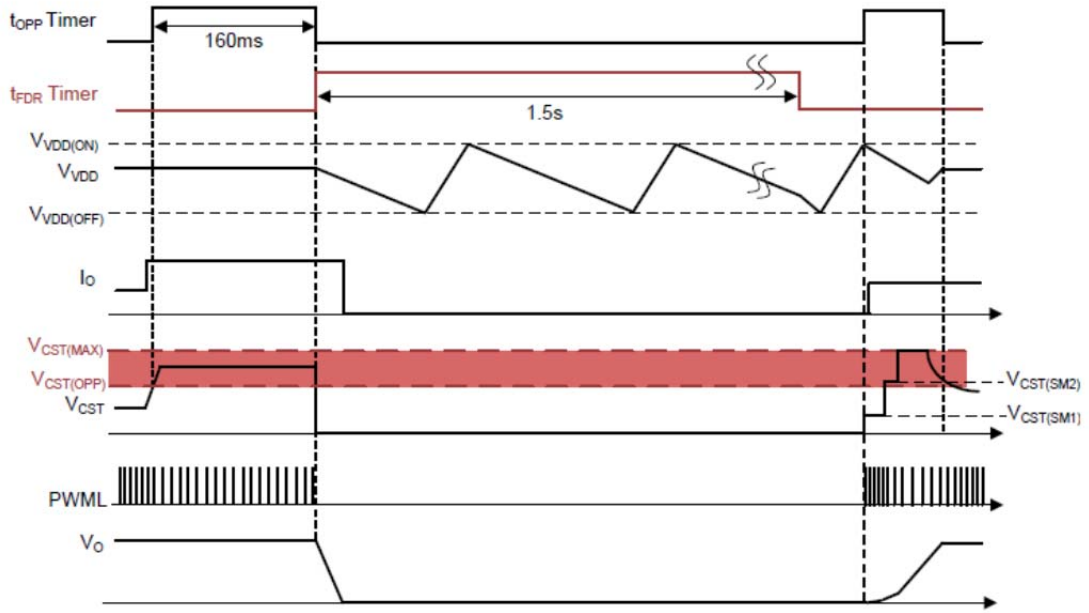


Figure 35. Timing Diagram of OPP

Please note that VCST(OPP) changes with IVLS current and is a delayed over power protection. In this design and may vary with line depending Rvs1 and Npa. Vopp1 = 600 mV and Vopp4 = 425mV in regards to figure 34.

Figure 34 comes from the data sheet and shows the OPP, PCL and OCP trip points.

1.) The first trip point Vcst(opp) needs to see the peak current limit consectutivly trigered for 160 ms before shutting down.
2.) The PCL is a cycle by cycle peak current limit that can be delivered for 160 ms this is more power than OPP.
3.) The OCP will only be seen in the case of transformer saturation or output short circtuit. This will be seen when the CS voltage is above VOCP (1.2V).

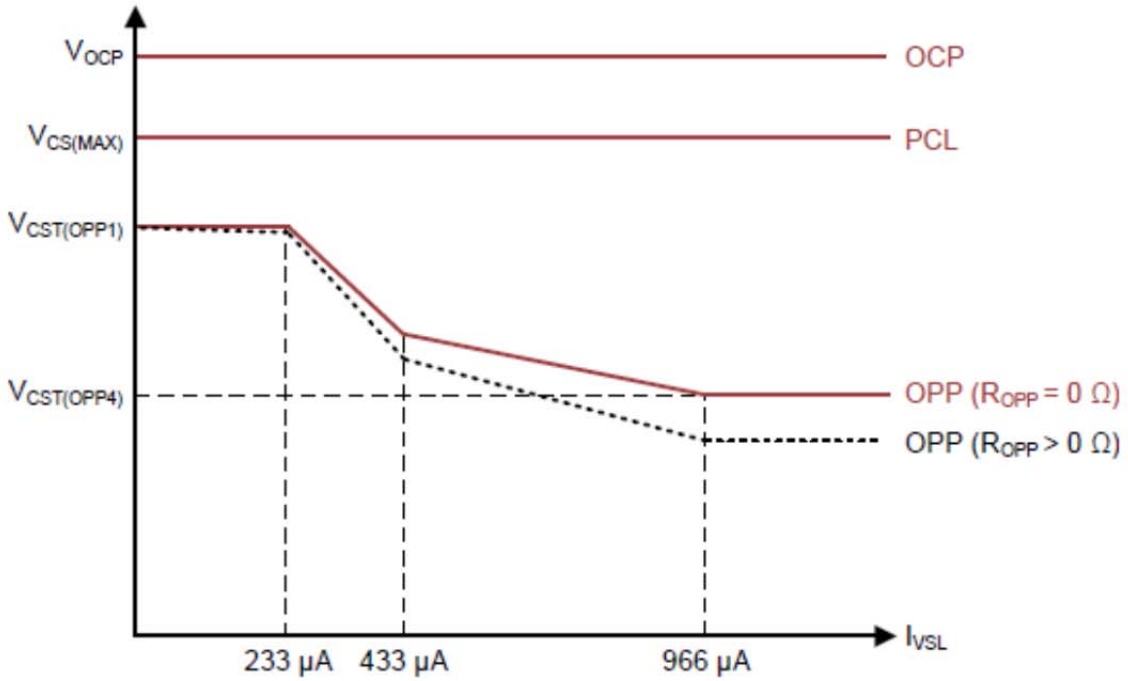


Figure 34. CS-Pin Related Faults

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
PROTECTION						
V_{OVP}	Over-voltage threshold	V_{VS} increasing	4.4	4.5	4.6	V
V_{OCP}	Over-current threshold	V_{CS} increasing	0.97	1.2	1.35	

Regards,

Mike